PoE Powered Device and 24V/1A Active Clamp Forward DC-DC Converter Using the MAX5974C and MAX5969B

MAXREFDES1206

Introduction

The MAXREFDES1206 is a Power over Ethernet (PoE) powered device and active clamp forward converter that delivers up to 1A at 24V from a 39V to 57V supply voltage. It is designed for powered device (PD) systems to comply with the IEEE® 802.3af/at standard in a PoE system. The MAXREFDES1206 illustrates techniques using the active clamp forward topology to generate isolated output. This document explains how the MAX5969B and MAX5974C can be used to design the PD to generate 24V from 39V to 57V input voltage. Table 1 is an overview of the design specification.

Power over Ethernet (PoE) is a technology that allows network cables to deliver power to a powered device (PD) through power-sourcing equipment (PSE) or midspan. It has many advantages over traditional methods of delivering power. PoE allows power and data to be combined, removing the need to alter the AC mains infrastructure. It can be installed by non-electricians. PoE is an intelligent system designed with protection at the forefront, preventing overload, underpowering, and installation errors, while allowing simple scalability and reliability.

The MAX5974C provides control for wide-input-voltage, active-clamped, current-mode PWM, forward converters in Power-over-Ethernet (PoE) powered device (PD) applications. The MAX5974C is highly suitable for universal or telecom input ranges.

Its other features include:

- Programmable Switching Frequency from 100kHz to 600kHz
- Programmable Frequency Dithering for Low-EMI, Spread-Spectrum Operation
- Programmable Dead Time, PWM Soft-Start, Current Slope Compensation
- Programmable Feed-Forward Maximum Duty-Cycle Clamp, 80% Maximum Limit
- Frequency Foldback for High-Efficiency Light-Load Operation
- Internal Bootstrap UVLO with Large Hysteresis
- 100µA (typ) Startup Supply Current
- Fast Cycle-by-Cycle Peak Current-Limit, of 5V and 35ns Typical Propagation Delay
- 115ns Current-Sense Internal Leading-Edge Blanking
- Output Short-Circuit Protection with Hiccup Mode
- Reverse Current Limit to Prevent Transformer Saturation Due to Reverse Current

Hardware Specification

This reference circuit consists of the MAX5969B PD con-troller and an isolated active clamp forward DC-DC converter using the MAX5974C to demonstrate a 24V DC output application. A 1GbE RJ45 magnetic jack is also included as well as two diode bridges to separate data and DC power provided by an endspan or midspan PoE system. The power supply delivers up to 1A at 24V. Table 1 is an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	TYP	MAX
Input Voltage Range	V_{IN}	39V	48V	57V
Switching Frequency	f_{SW}		250kHz	
Maximum Efficiency	η		88%	
Output Voltage	V_{OUT}	23.76V	24V	24.24V
Output Voltage Ripple	ΔV_O		240mV	
Output Current Range	I_{OUT}	0A		1A
Output Power	P_{OUT}	0W		24W

Designed–Built–Tested

This document describes the hardware in Figure 1. It provides a detailed technical guide to design a complete interface for a PD to comply with the IEEE 802.3af/at standard in a PoE, class 4 system, and an isolated active clamp forward DC-DC converter using Maxim's MAX5974C controller. The power supply was built and tested.

MAX5969B PD Interface

A PoE system delivers power and data to an end device (PD) typically through an RJ45 cable power from an endspan (PSE) (Figure 2) or a midspan (Figure 3). The power is separated from the data through diode bridges to deliver a typical 48V for efficient power transfer. This is low enough to be considered a safe voltage, removes the need to rewire AC mains, and saves cost.

The voltage still can damage equipment if not properly delivered although it is safe for humans. This is where MAX5969B classification is required, ensuring the equipment can handle the power delivery. The PSE must perform a signature detection before it can enable power to a connected IP camera or other PD.

Figure 1. MAXREFDES1206 hardware.

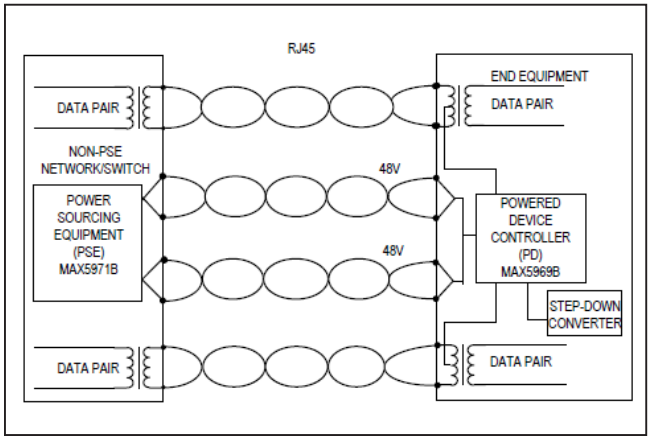

Figure 2. PoE endspan power injector.

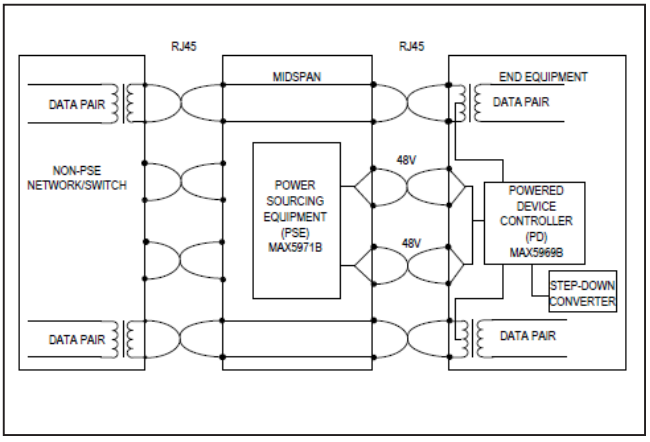

Figure 3. PoE midspan power injector.

Signature Detection

Signature detection uses a lower voltage to detect a characteristic signature of IEEE-compatible PDs (a 24.9kΩ resistance) (Figure 4). The PSE knows that higher voltages can be safely applied once this signature is detected. The PSE applies two voltages on V_{IN} in the range of 1.4V to 10.1V (1V step minimum). It then records the current measurements at the two applied voltages. The PSE then computes the change in current when each voltage is applied (ΔV/ΔI) to ensure the presence of the 24.9kΩ signature resistor.

Classification

The PSE classifies the PD based on the power consumption required in the classification mode. The IEEE 802.3af/at standard defines only Class 0 to 4 and Class 5 for any special requirement.

An external resistor (R_{CLS}) of 30.9Ω connected from the CLS to V_{SS} sets the classification current. The PSE determines the class of a PD by applying a voltage at the PD input and measuring the current sourced from the PSE. The MAX5969A/MAX5969B exhibit a current of 36mA to 44mA when the PSE applies a voltage between 12.6V and 20V.

The PSE uses the classification current information to classify the power requirement of the PD (MAX5969B).

The classification current includes the current drawn by R_{CLS} and the supply current of the MAX5969A/MAX5969B. So, the total current drawn by the PD is within the IEEE 802.3af/at standard figures. The classification current is turned off whenever the device is in power mode (Figure 5).

Power Mode

The final stage after detection and classification of a newly connected PD is to enable power. The 48V supply from the PSE is connected to the PD through the RJ45 cable. Once enabled, the PSE continues to monitor how much current is being delivered to the PD and cuts power to the cable if the power drawn is not within the correct range. This protects the PSE against overload and underpowering, and ensures the PSE is disconnected from the cable if the PD is unplugged or faulted (Figure 6).

The MAX5969B enters power mode when V_{IN} rises above the undervoltage lockout threshold (V_{ON}). Note that V_{ON}/V_{OFF} = 38.6V/31V for the MAX5969B. The MAX5969B turns on the internal n-channel isolation MOSFET to connect GND to RTN when V_{IN} rises above V_{ON}. The open-drain power-good output (PG) remains low for a minimum of t_{DELAY} until the power MOSFET fully turns on to keep the downstream DC-DC converter disabled during inrush. The PGOOD open-drain output is also connected to three small-signal transistors to prevent the DC converters from powering up before the power from the PD is allowable.

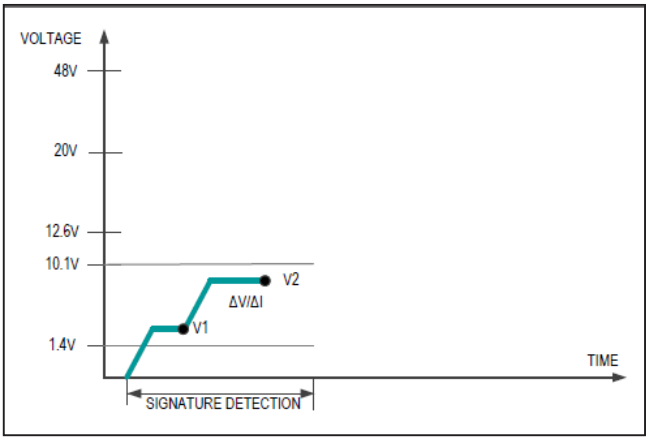

Figure 4. Signature detection.

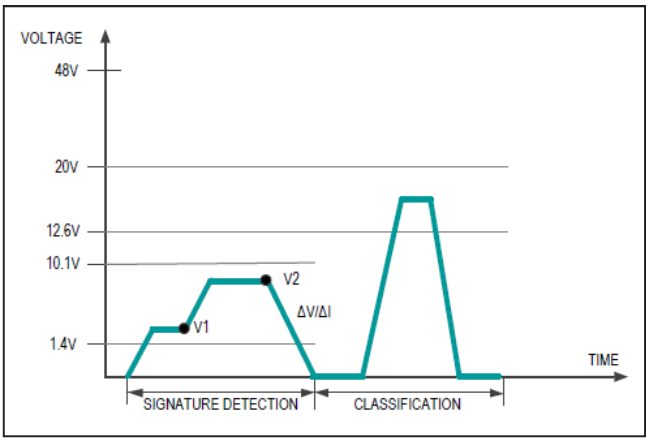

Figure 5. Classification.

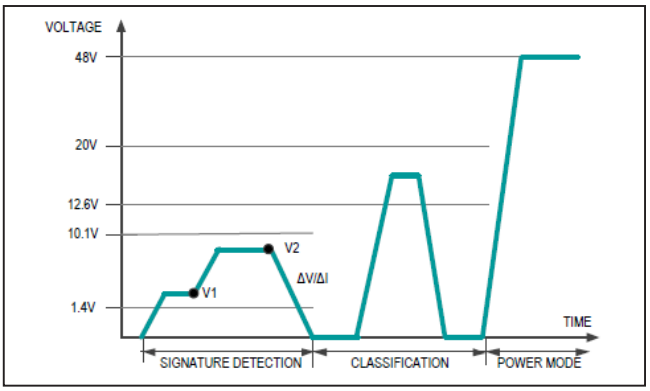

Figure 6. Power enabled.

Design Considerations for MAX5969B

Place the input capacitor, classification resistor, and transient voltage suppressor as close as possible to the MAX5969A/MAX5969B. Use large SMT component pads for power dissipating devices such as the MAX5969A/MAX5969B, and the external diodes. Use short and wide traces for high-power paths.

The MAX5969B enters undervoltage lockout when the input voltage drops below 31V. The isolation MOSFET switches off, disconnecting the 48V from the buck converters, when the input drops below this value. The MAX5969B exits undervoltage lockout when the input exceeds 38.6V, where the isolation MOSFET switches on again, connecting the MAX5974C forward converter.

The Active Clamp Forward Converter

The single-ended forward converter has always been a favorite of designers for single- and multiple-output power supplies in the range from watts to kilowatts. This topology uses a second out-of-phase winding (reset winging) to reset the magnetic flux in the power transformers core when the secondary side freewheeling diode is conducting. The drain-source voltage of the main power switch is limited (excluding ringing due to leakage inductance and parasitic capacitance in the circuit) to two times the input voltage of the power supply if the number of turns on this winding is equal to the number of turns on the main transformer's primary winding. But the maximum duty cycle is also limited to less than 50%. This duty cycle limit can be extended above 50% to improve transformer utilization by increasing the number of turns on the reset winding, but only at the expense of a higher drain-source voltage (increased voltage stress and switching power losses) on the main power switch.

These and other limitations of the forward converter can easily be overcome when the designer fully understands the operation and unique benefits of the ACFC topology.

Figure 7 shows the main components of an ACFC. The active clamp consists of a P-channel MOSFET (Q_{AUX}) and a clamp capacitor (C_{CLAMP}). The difference between the traditional forward converter and the ACFC occurs when the main power MOSFET (Q_{MAIN}) is off. The reset winding and diode of the traditional forward converter clamps the drain-source voltage of QMAIN to approximately twice the power supply input voltage during the first half of the interval when Q_{MAIN} is off. The drain-source voltage of Q_{MAIN} in the ACFC is clamped to an intermediate voltage between V_{IN} and $2V_{IN}$ for the full interval when Q_{MAIN} is off.

The benefits of the ACFC topology go far beyond reducing the voltage stress on the main power MOSFET and increasing the duty cycle limit.

Table 2. Setting the Classification Current.

CLASS	MAXIMUM POWER USED BY PD (W)	R_{CLS} (Ω)	V_{IN}* (V)	CLASS CURRENT SEEN AT V_{IN} (mA)		IEEE 802.3af/at PSE CLASSIFICATION CURRENT SPECIFICATION (mA)	
				MIN	MAX	MIN	MAX
0	0.44 to 12.95	619	12.6 to 20	0	4	0	5
1	0.44 to 3.94	117	12.6 to 20	9	12	8	13
2	3.84 to 6.94	66.5	12.6 to 20	17	20	16	21
3	6.49 to 12.95	43.7	12.6 to 20	26	30	25	31
4	12.95 to 25.5	30.9	12.6 to 20	36	44	35	45
5	>25.5	21.3	12.6 to 20	52	64	-	-

V_{IN} is measured across the MAX5969A/MAX5969B input V_{DD} to V_{SS}.

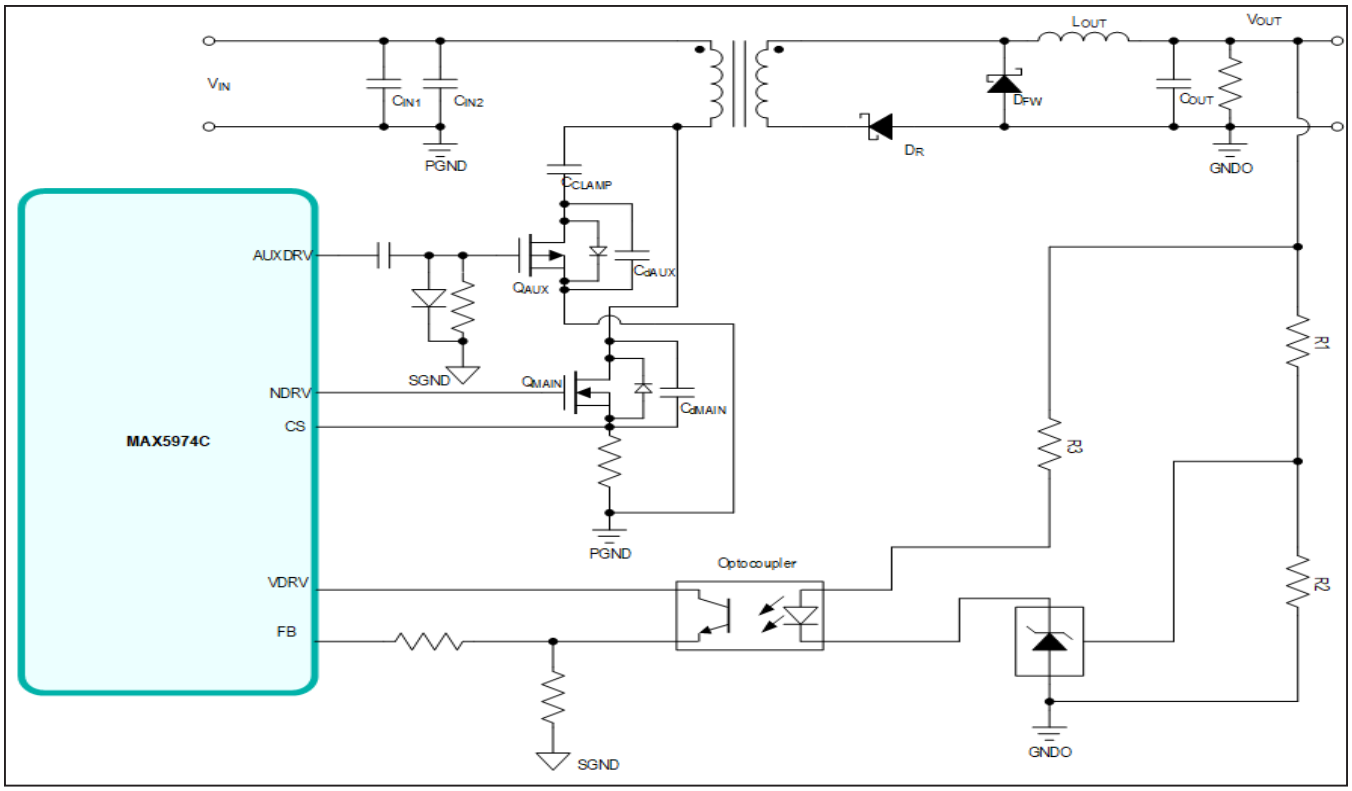

Figure 7. Active clamp forward converter topology.

The ACFC topology provides further benefits like:

- Zero voltage switching (ZVS) for Q_{MAIN} and Q_{AUX} over the full load range by careful design, thus significantly improving power supply efficiency.
- A smaller output inductance due to higher operating duty cycle.
- Operating at higher than 50% duty cycle allows a higher secondary to primary turns ratio on the transformer leading to a lower reflected current from the secondary to primary, and thus a lower peak current in the main power MOSFET.
- Lower EMI due to the ZVS nature of the switching.

Figure 8 shows the main steady-state waveforms of the ACFC. It is very important to understand what is happening during one complete switching cycle of the converter.

Time Interval t_0 to t_1:

Q_{MAIN} turns on at t0, Q_{AUX} remains off. The primary current IP, which is the sum of the transformer magnetizing I_{MAG} and the reflected secondary current I_{SEN}, flows through the primary of the transformer and Q_{MAIN}. I_P ramps up linearly while Q_{MAIN} is on. Current also flows in the secondary side through the rectifying MOSFET Q_R while Q_{MAIN} is on. No current flows through Q_{AUX} during this interval.

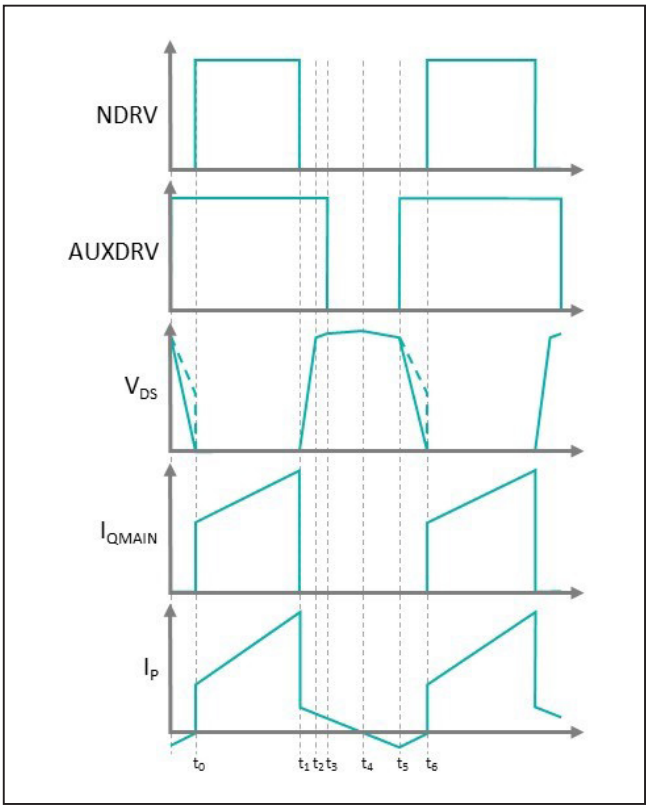

Figure 8. ACFC waveforms.

Time Interval t_1 to t_2:

Q_{MAIN} turns on at t_1. Q_R is now reversed-biased. So, the reflected secondary current component of I_P is zero. I_P is now only the transformer magnetizing current. It decreases towards zero, charging the drain capacitance of Q_{MAIN}, C_{DMAIN}.

Time Interval t_2 to t_3:

The drain voltage of Q_{MAIN} reaches the same voltage level as that voltage across C_{CLAMP} at t_2. The body diode of Q_{AUX} becomes forward-biased and voltage across C_{CLAMP} increases. The rate of increase of the drain voltage of Q_{MAIN} is now much lower since C_{CLAMP} >> C_{DMAIN}.

Time Interval t_3 to t_4:

Q_{AUX} turns on at t_3. Q_{AUX} switches under the ZVS condition, providing it turns on after its body diode starts conducting (at t_2) and before I_P goes negative (at t4). Q_{AUX} must be on before t4. Or, the I_P has no path to go negative at t_4.

Time Interval t_4 to t_5:

I_P is now negative at t_4 and discharges C_{CLAMP} through Q_{AUX}, which is on. The I_P continues to become more negative and the drain voltage of Q_{MAIN} decreases.

Time Interval t_5 to t_6:

Q_{AUX} turns off at t_5 and the voltage across C_{CLAMP} stops decreasing. The only current path now available for the negative I_P to flow is out of C_{DMAIN}. The voltage across C_{DMAIN} decreases until I_P reaches zero. V_{DS} decays to zero by t_6 providing the energy stored in the magnetizing. The leakage inductance at t_5 is greater than the energy stored in C_{DMAIN} at t_5. ZVS occurs if this condition is met. Or, Q_{MAIN} switches on at t_6 at some intermediate voltage between 0 and V_{DSMAX}. IMPORTANT: Reducing L_{MAG} increases the inductive energy stored in LMAG. So, ZVS does not occur if L_{MAG} is too big, as shown by the dash line on the V_{DS} graph.

Design Procedure for the ACFC

Now that the principle of operation of the ACFC is understood, a practical design example can be illustrated. The converter design process can be divided into several stages: power stage design, setup of the MAX5974C ACFC current-mode controller, and the feedback loop. This document is primarily concerned with the power stage design and the feedback loop is intended to complement the information contained in the MAX5974C data sheet on how to set up supervisory and protection functions of the controller.

The following design parameters are used throughout:

- V_{IN} - Input Voltage
- V_{OUT} - Output Voltage
- ΔV_{OUT} - Output Ripple Voltage
- I_{OUT} - Output Current
- $P_{OU}T$ - Output Power
- η - Target Maximum Efficiency
- P_{IN} - Input Power
- f_{SW} - Switching Frequency
- D - Duty Cycle
- N - Primary-Secondary Turns Ratio
- N_P - Turns of Primary Winding
- N_S - Turns of Secondary Winding
- N_{AUX} - Turns of Tertiary Winding

The above symbols are sometimes followed by parenthesis to indicate if minimum or maximum values of the parameters are intended. For example, the minimum input voltage is intended by the symbol $V_{IN(MIN)}$. Or, typical values are intended. Also, there is reference to the schematic in another document through the design procedure.

Step 1: Choosing a Suitable Switching Frequency

The MAX5974C can operate at a switching frequency between 100kHz and 600kHz. A lower switching frequency optimizes the design for efficiency. A higher frequency allows for smaller inductive and capacitive components as well as lower costs. A switching frequency of 250kHz was chosen for this design. R15 sets the switching frequency as:

$$R15 = \frac{8.7 \times 10^9}{f_{SW}} = \frac{8.7 \times 10^9}{250 \times 10^3 Hz} = 34.8k\Omega$$

Step 2: Setting the Maximum Duty Cycle

One advantage of using the MAX5974C for the ACFC is the maximum allowable duty cycle. Transformer saturation can occur if the duty cycle is not clamped at some maximum value, resulting in catastrophic failure. Q_{MAIN} can be subjected to increased voltage stress. A maximum duty cycle of 80% is recommended at switching frequencies up to 400kHz. An initial choice of 62% allows for some design margin.

$$D_{MAX} = 0.62$$

Step 3: Calculating the Transformer Turns Ratio

The transformer turns ratio for the forward converter topology is:

$$n = \frac{V_{IN(MIN)} - V_{MDS(ON)}}{V_{DR(F)} + V_{LOUT} + \frac{V_{OUT}}{D_{MAX}}}$$

where $V_{MDS(ON)}$ is the drain-source voltage of Q_{MAIN} in the on state, $V_{DR(F)}$ is the forward voltage drop of D_R, and V_{LOUT} is the resistive DC voltage drop across the output inductor winding. D_{MAX} occurs at $V_{IN(MIN)}$. Assuming $V_{MDS(ON)}$ = 0.2V, $V_{DR(F)}$ = 0.5V, and V_{LOUT} = 0.2V:

$$n = \frac{N_P}{N_S} = \frac{39V - 0.2V}{0.5V + 0.2V + \frac{24V}{0.62}} = 0.9845$$

Step 4: Calculating the Turns of the Primary Winding N_P, Secondary Winding N_S, Tertiary Winding N_{AUX}

The transformer turns of the primary winding for the forward converter topology is:

$$N_P = \frac{V_{IN(MIN)} \times D_{MAX}}{\Delta B \times Ae \times f_{SW}} \times 10^4$$

where ΔB is the flux density deviation of the transformer, which must be ≤ 2000GS, Ae is the effective magnetic cross-section of the transformer core. EP13 is chosen as the transformer core considering the maximum output power and size of this design. The effective magnetic cross of EP13 is 0.195cm^2. Then,

$$N_P = \frac{39V \times 0.62}{2000GS \times 0.195 \times 10^{-4} m^2 \times 250kHz} \times 10^4 = 24.8T \approx 25T$$

25 turns are used for the primary winding. The secondary turns become:

$$N_S = \frac{N_P}{n} = \frac{25T}{0.9845} = 25.3936T \approx 25T$$

25 turns are used for the secondary winding. Then,

$$n = \frac{N_P}{N_S} = \frac{25T}{25T} = 1$$

The voltage at IN is derived from a tertiary winding of the transformer during normal operation. The tertiary winding turns become:

$$N_{AUX} = N_S \times \frac{V_{AUX}}{V_{OUT}} = 25T \times \frac{12}{24} = 12.5T$$

12 turns are used for the tertiary winding.

Step 5: Calculating D at $V_{IN(MIN)}$, $V_{IN(TYP)}$, and $V_{IN(MAX)}$

Rearranging the expression in Step 3:

$$D = \frac{V_{OUT}}{\left(\frac{V_{IN} - V_{MDS(ON)}}{n}\right) - V_{DR(F)} - V_{LOUT}}$$

and

Step 6: Calculating $V_{MDS(MAX)}$ of Q_{MAIN} at D_{MIN}, D_{TYP}, and D_{MAX}

D_{MIN}	D_{TYP}	D_{MAX}
0.4278	0.51	0.63

V_{MDS} for the forward converter topology is:

$$V_{MDS} = \frac{V_{IN}}{1 - D}$$

Given the D_{MAX} occurs at $V_{IN(MIN)}$, D_{TYP} occurs at $V_{IN(TYP)}$, and D_{MIN} occurs at $V_{IN(MAX)}$:

V_{MDS} at $V_{IN(MAX)}$	V_{MDS} at $V_{IN(TYP)}$	V_{MDS} at $V_{IN(MIN)}$
99.62V	97.96V	105.41V

The critical operating parameters of the converter are now fixed. So, it is possible to continue the design process of calculating and selecting the suitable components for the power train.

Step 7: Calculating and Selecting L_{OUT}

The output inductance is calculated assuming a maximum peak-to-peak output ripple (ΔI_{SEC}), which occurs at the maximum input voltage. The output inductance is:

$$L_{OUT} = \frac{\left(V_{OUT} - V_{DFW(F)}\right) \times \left(1 - D_{MIN}\right)}{I_{OUT} \times \%\Delta I_{SEC} \times f_{SW}}$$

where $V_{DFW(F)}$ is the forward voltage drop of the secondary freewheeling diode, $\%\Delta I_{SEC}$ (0.6, typical) is the ratio of peak-to-peak output inductor current ripple to the average output current at maximum input voltage. Then,

$$L_{OUT} = \frac{(24V - 0.5V) \times (1 - 0.4278)}{1A \times 0.6 \times 250kHz} = 89.64uH$$

where I_{OUT} = 1A and $V_{DFW(F)}$ = 0.5V. A standard ±20% tolerance 100µH inductor is chosen for this design. Finally, choose an output inductor with a DC winding resistance sufficiently low to ensure that V_{LOUT} is less than 0.2V at $I_{O(MAX)}$, because this is the value used for V_{LOUT} in the preceding calculations. Choose an inductor with:

$$R_{LDC} < \frac{V_{LOUT}}{I_{OUT(MAX)}} = \frac{0.2V}{1A} = 0.2\Omega$$

The final inductor value chosen for this design is a 20% tolerance 100µH/2.1A/150mΩ inductor SRR1280A-101M from Bourns.

Step 8: Calculating the Transformer Magnetizing Inductance L_{MAG}, and Secondary and Primary Peak Winding Currents $I_{S(PK)}$ and $I_{P(PK)}$

The physical design of the power transformer is outside the scope of this document. However, it is necessary to calculate the critical parameters of the transformer.

Calculate the minimum output inductor ripple current by rearranging the expression in Step 7 and remembering that minimum ripple occurs at D_{MAX} as follows:

$$\Delta I_{L(MIN)} = \frac{\left(V_{OUT} - V_{DFW(F)}\right) \times \left(1 - D_{MAX}\right)}{L_{OUT(MAX)} \times f_{SW}}$$

$L_{OUT(MAX)}$ for the selected ±20% 100µH inductor is 120µH. So,

$$\Delta I_{L(MIN)} = \frac{\left(24V - 0.5V\right) \times \left(1 - 0.63\right)}{120\mu H \times 250kHz} = 0.29A$$

The maximum magnetizing current referred to the primary side of the transformer must be less than the minimum output inductor ripple current reflected to the primary side of the transformer for the MAX5974C ACFC current-mode controller to function properly. So,

$$I_{MAG(MAX)} < \frac{\Delta I_{L(MIN)}}{n}$$

and

$$I_{MAG(MAX)} < \frac{0.29A}{1} = 0.29A$$

Chose a value for I_{MAG} = 0.25A (85% of $I_{MAG(MAX)}$) to allow for the design margin. The next step is to calculate a minimum magnetizing inductance that ensures that $I_{MAG(MAX)}$ < 0.25A. Use the following expression to calculate $L_{MAG(MIN)}$:

$$L_{MAG(MIN)} = \frac{\left(V_{IN(MAX)} - V_{DS(ON)}\right) \times D_{MIN}}{I_{MAG(MAX)} \times f_{SW}}$$

So,

$$L_{MAG(MIN)} = \frac{\left(57V - 0.2V\right) \times 0.4278}{0.25A \times 250kHz} = 388.78\mu H$$

Choose L_{MAG}= 600µH ± 30% allowing for a ±30% tolerance for the magnetizing inductance. Figure 9 illustrates the output inductor current I_L, the secondary transformer current I_S, primary transformer current I_P, and the current flowing in main power MOSFET I_{QMAIN}.

There is a resonance between the two end points, which makes ZVS possible, although I_P appears linear when both Q_{MAIN} and Q_{AUS} are off (t_1 to t_3 and t_5 to t_6).

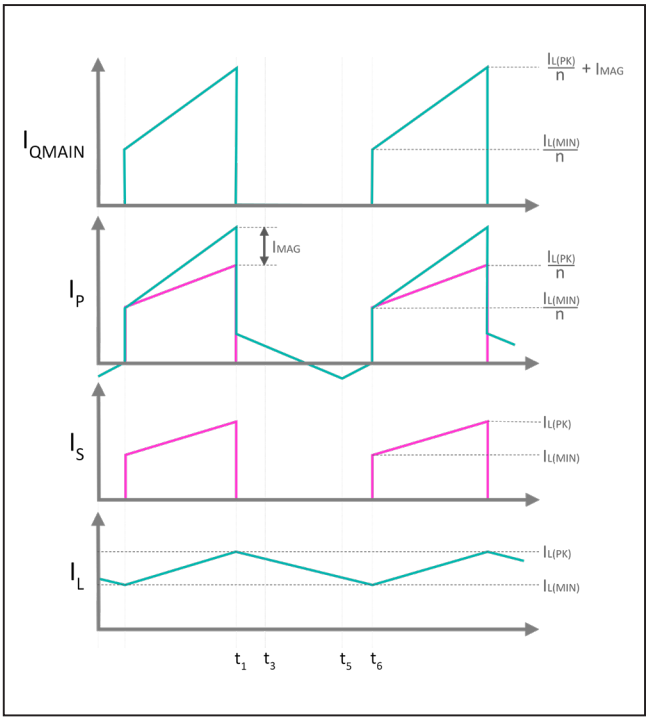

Figure 9. Current waveforms.

The peak current in the secondary winding $I_{S(PK)}$ is equal to the peak current in the output inductor $I_{L(PK)}$. $I_{L(PK)}$ is a maximum at $V_{IN(MAX)}$ and $I_{O(MAX)}$. So,

$$I_{L(PK)} = I_{O(MAX)} + \frac{\left(V_{OUT} - V_{DFW(F)}\right) \times \left(1 - D_{MIN}\right)}{2 \times L_{OUT(MIN)} \times f_{SW}}$$

and

$$I_{S(PK)} = I_{L(PK)}$$

So,

$$I_{S(PK)} = 1A + \frac{(24V - 0.5V) \times (1 - 0.4278)}{2 \times 80\mu H \times 250kHz} = 1.34A$$

The peak current in the primary winding $I_{P(PK)}$ is the peak current in the secondary winding reflected to the primary side of the transformer plus I_{MAG}. So,

$$I_{P(PK)} = \frac{I_{S(PK)}}{n} + I_{MAG}$$

So,

$$I_{P(PK)} = \frac{1.34A}{1} + 0.25A = 1.59A$$

The transformer must not saturate at a magnetizing force of (N_P x $I_{P(PK)}$), where N_P is the number of turns on the primary winding.

Step 9: Calculating the Maximum RMS Currents in the Transformer Secondary and Primary Windings $I_{S(RMS)}$ and $I_{P(RMS)}$

The maximum RMS currents in the transformer primary and secondary windings occur at $V_{IN(MIN)}$ and $I_{OUT(MAX)}$, i.e., at D_{MAX}. First calculate $I_{L(PK)}$ in the output inductor at $V_{IN(MIN)}$ to calculate $I_{S(PK)}$ at $V_{IN(MIN)}$.

Following the process in Step 8, at VIN(MIN):

$$I_{L(PK)} = I_{O(MAX)} + \frac{\left(V_{OUT} - V_{DFW(F)}\right) \times \left(1 - D_{MAX}\right)}{2 \times L_{OUT(MIN)} \times f_{SW}}$$

and

$$I_{S(PK)} = I_{L(PK)}$$

So,

$$I_{S(PK)} = 1A + \frac{(24V - 0.5V) \times (1 - 0.63)}{2 \times 80\mu H \times 250kHz} = 1.22A$$

The current at which the secondary rectifying Diode D_R starts to conduct $I_{S(V)}$ corresponds to $I_{L(MIN)}$.

So,

$$I_{S(V)} = 1A - \frac{(24V - 0.5V) \times (1 - 0.63)}{2 \times 80\mu H \times 250kHz} = 0.78A$$

The maximum RMS current in the secondary winding becomes:

$$I_{S(RMS)} = \sqrt{D_{MAX} \times \frac{I_{S(PK)}^2 + I_{S(PK)} \times I_{S(V)} + I_{S(V)}^2}{3}}$$

So,

$$I_{S(RMS)} = \sqrt{0.63 \times \frac{1.22^2 + 1.22 \times 0.78 + 0.78^2}{3}} = 0.8A$$

Referring to Figure 8, calculate the instantaneous current in Q_{MAIN} at turn-on and turn-off $I_{QM(t\text{-}on)}$ and $I_{QM(t\text{-}off)}$:

$$I_{QM(t-on)} = \frac{I_{SV}}{n} = \frac{0.78A}{1} = 0.78A$$

$$I_{QM(t-off)} = \frac{I_{S(PK)}}{n} + I_{MAG} = \frac{1.22A}{1} + 0.25A = 1.47A$$

The maximum RMS current in Q_{MAIN} is now:

$$I_{QM(RMS)} = \sqrt{0.63 \times \frac{0.78^2 + 0.78 \times 1.47 + 1.47^2}{3}} = 0.91A$$

The transformer primary current I_P in Figure 9 is a more complex waveform than I_{QM}. I_P is a superposition of I_{QM} and I_{QA}, and the resonant currents that flow during the time intervals when both Q_{MAIN} and Q_{AUX} are off. Nevertheless, it is reasonable to use the approximation:

$$I_{P(RMS)} = I_{QM(RMS)}$$

Table 3 details all the critical parameters of the transformer achieved from the above equations/calculations.

Table 3. Critical Parameters of the Transformer.

PARAMETER	SYMBOL	VALUE
Primary Magnetizing Inductance	L_{MAG}	600µH±30%
Primary Peak Current	$I_{P(PK)}$	1.59A
Primary RMS Current	$I_{P(RMS)}$	0.91A
Turns Ratio (N_P/N_S)	n	1
Primary Turns	N_P	25T
Secondary Turns	N_S	25T
Tertiary Turns	N_{AUX}	12T
Secondary Peak Current	$I_{S(PK)}$	1.34A
Secondary RMS Current	$I_{S(RMS)}$	0.8A

A suitable transformer is designed using the parameters in Table 3.

Step 10: Choosing a Suitable MOSFET for Q_{MAIN}

All the necessary parameters to select a suitable Q_M are already calculated.

From Step 6:

$$V_{DS(MAX)} = 105.41V$$

From Step 8:

$$I_{QM(PK)} = I_{P(PK)} = 1.59A$$

and

$$I_{QM(RMS)} = 0.91A$$

The Fairchild part number FDC86244 (allowing for reasonable design margin) was chosen for this design with the following specifications:

Maximum D-S Voltage	150V
Continuous Drain Current	2.3A
D-S Resistance at VGS = 4.5V	144mΩ
Total Gate Charge Qg	6nC

Step 11: Choosing the Suitable Rectifying and Freewheeling Diode for D_R and D_{FW}

Almost all the necessary parameters for selecting a suitable D_R are already calculated. Step 8 was used to calculate $I_{S(PK)}$, the same peak current that flows in D_R.

So,

$$I_{DR(PK)} = I_{S(PK)} = 1.34A$$

Step 9 was used to calculate the maximum RMS current in the transformer secondary winding $I_{S(RMS)}$, the same RMS current that flows in D_R.

So,

$$I_{DR(RMS)} = I_{S(RMS)} = 0.8A$$

The peak reverse voltage seen by D_R is:

$$V_{DR(R)} = \frac{V_{IN(MIN)} \times D_{MAX}}{n \times (1 - D_{MAX})}$$

So,

$$V_{DR(R)} = \frac{39V \times 0.63}{1 \times (1 - 0.63)} = 66.41V$$

For the freewheeling diode D_{FW}:

$$I_{FW(PK)} = I_{S(PK)} = 1.34A$$

The maximum RMS current in the freewheeling diode occurs at $V_{IN(MAX)}$ and is:

$$I_{FW(RMS)} = \sqrt{(1 - D_{MIN}) \times \frac{I_{FW(PK)}^2 + I_{FW(PK)} \times I_{FW(V)} + I_{FW(V)}^2}{3}}$$

where

$$I_{FW(V)} = I_{O(MAX)} - \frac{(V_{OUT} - V_{DFW}) \times (1 - D_{MIN})}{2 \times L_{OUT(MIN)} \times f_{SW}} = 0.664A$$

So,

$$I_{FW(RMS)} = 0.772A$$

Finally, the peak reverse voltage seen by D_{FW} is:

$$V_{DFW(R)} = \frac{(V_{IN(MAX)} - V_{DR(F)})}{n} = \frac{(57V - 0.5V)}{1} = 56.5V$$

A Schottky diode, part number RB068LAM150TF, allowing for a reasonable design margin, was selected for both D_R and D_{FW}.

Step 12: Choosing a Suitable P-Channel MOSFET for the Active Clamp Switch Q_{AUX}

Only a portion of the primary magnetizing current flows in the drain of the active clamp switch during the interval between t_3 and t_5. Assuming the worst case that all the magnetizing current flows in Q_{AUX}, the RMS current flowing in the drain of Q_{AUX} is:

$$I_{MAG(RMS)} = \sqrt{D_{MAX} \times \frac{I_{MAG}^2}{3}} = \sqrt{0.63 \times \frac{0.25^2}{3}} = 0.115A$$

Conduction losses are very low at such a low RMS current. So, choosing a MOSFET with a low gate charge must be the primary consideration, with low $R_{DS(ON)}$ being only a secondary concern. Switching losses are also negligible in addition to conduction losses being very low, because the body diode of Q_{AUX} is conducting before Q_A turns on. The repetitive peak current in Q_{AUX} is the maximum primary magnetizing current:

$$I_{QA(PK)} = I_{MAG} = 0.25A$$

The active clamp switch experiences the same voltage stress as the main power switch. Referring to Step 6, it is:

$$V_{DS(QA)} = V_{DS(QM)} = \frac{V_{IN(MAX)}}{1 - D_{MIN}} = 99.62V$$

The Vishay P-Channel MOSFET, SI1411DH-T1-GE3, allowing for reasonable design margin, was chosen for this design with the following specifications:

Maximum D-S Voltage	150V
Peak Repetitive Drain Current	0.42A
D-S Resistance at VGS =7V	2.05Ω

Step 13: Choosing a Suitable Clamp Capacitor C17

The clamp capacitor (C17) helps in resetting the flux in the transformer core as well absorbing leakage inductance energy. It forms a complex pole-zero pair with the magnetizing inductance (L_{MAG}) of the transformer at a frequency f_R:

$$f_R = \frac{1 - D_{MAX}}{2\pi \times \sqrt{L_{MAG} \times C17}}$$

The value of the clamp capacitor for a 20% voltage ripple is:

$$C17 = \frac{I_{MAG} \times (1 - D_{MIN})^2}{1.6 \times V_{IN(MAX)} \times f_{SW}} = \frac{0.25A \times (1 - 0.4278)^2}{1.6 \times 57V \times 250kHz} = 3.59nF$$

2.2nF is chosen as the clamp capacitor.

The voltage stress on the clamp capacitor is:

$$V_{C17} = \frac{V_{IN}}{1 - D}$$

The C17 must be rated for at least 1.4x the calculated worst-case V_{C12} stress.

Step 14: Calculating and Choosing the Output Capacitor C_{OUT}

The output capacitance value can be calculated based on either steady-state voltage ripple or transient voltage ripple. The output capacitor is usually sized to support a step load of 25% of the rated output current (I_{OUT}) in isolated applications if the design consideration is the transient steady-state voltage ripple. So, the output-voltage deviation is contained to 3% of the rated output voltage. The output capacitance is:

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{2 \times \Delta V_{OUT}}$$

where C_{OUT} is the total capacitance required at the output, I_{STEP} is the load step, $t_{RESPONSE}$ is the response time of the controller, and ΔV_{OUT} is the allowable output voltage deviation during transient.

The response time of the controller $t_{RESPONSE}$ is:

$$t_{RESPONSE} = \frac{0.33}{f_C} + \frac{1}{f_{SW}}$$

The complex pole-zero pair frequency formed due to clamp capacitor and magnetizing inductance of the converter is:

$$f_R = \frac{1 - D_{MAX}}{2\pi \times \sqrt{L_{MAG} \times C17}} = \frac{1 - 0.63}{2\pi \times \sqrt{600\mu H \times 2.2nF}} = 51.28kHz$$

f_C is the target closed-loop crossover frequency:

$$f_C = \frac{f_R}{5} = \frac{51.28kHz}{5} = 10.256kHz$$

So, the response time of the controller $t_{RESPONSE}$ is:

$$t_{RESPONSE} = \frac{0.33}{10.256kHz} + \frac{1}{250kHz} = 36.18\mu s$$

Choose I_{STEP} equal to 25% of output current, I_{STEP} = 0.25A, ΔV_{OUT} = 3% of output voltage, which is equal to 720mV. So, the output capacitance is:

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{2 \times \Delta V_{OUT}} = \frac{0.25A \times 36.18\mu s}{2 \times 0.72V} = 6.28\mu F$$

5 x 4.7µF ceramic capacitors are used in this design to get smaller output voltage ripple. The total ceramic output capacitance is 5 × 4.7µF × 0.8 = 18.8µF considering 20% derating of the ceramic capacitors.

Step 15: Calculating and Choosing the Input Capacitor C_{IN}

Capacitor selection is based on the switching ripple. The maximum average input current drawn from the input power supply at minimum input voltage is:

$$I_{IN(AVG)} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN(MIN)}} = \frac{24V \times 1A}{0.88 \times 39V} = 0.7A$$

The voltage ripple present on the input capacitor is 2% of the minimum input voltage and is:

$$\Delta V_{IN(RIPPLE)} = 0.02 \times V_{IN(MIN)} = 0.02 \times 39V = 0.78V$$

The value of the input ceramic capacitor with the above assumed ripple voltage is:

$$C_{IN} = \frac{I_{IN(AVG)} \times (1 - D_{MAX})}{\Delta V_{IN(RIPPLE)} \times f_{SW}} = \frac{0.7A \times (1 - 0.63)}{0.78V \times 250kHz} = 1.29\mu F$$

2 × 1µF ceramic capacitors and one 33µF electrolytic capacitor are used for the input capacitor in this design.

Step 16: Calculating and Selecting the Peak Current Limit Resistors (R21 and R25)

The current-sense resistor (RCS in the Typical Application Circuits), connected between the source of the n-channel MOSFET and PGND, sets the current limit. The current limit comparator has a voltage trip level (VCS-PEAK) of 400mV. Use the following equation to calculate RCS:

$$R21 + R25 = \frac{400mV}{I_{P(PK)}} = \frac{400mV}{1.59A} = 252m\Omega$$

Two standard 400mΩ current-sense resistors are used in the design. Low-inductance, current-sense resistors must be used for R21 and R25.

Design Resources

Download the complete set of **Design Resources** including the schematics, bill of materials, PCB layout, and test files.

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/20	Initial release	—