Single-Output SEPIC Converter Using MAX16990

MAXREFDES1204

Introduction

The MAXREFDES1204 is a single-output SEPIC converter reference design developed using the MAX16990 controller. This reference design is rated to operate over a wide input voltage range from 6V to 18V. The design can deliver an output power of 24W at 12V. It is targeted for automotive applications.

Main features include the following:

- Very High Efficiency > 90% for Load > 25%
- Very Low Line and Load Regulation < 0.02%
- Output Voltage Ripple < 0.7% at Nominal V_{IN}
- Overshoot < 2.6% for 50% Step Load
- Continuous Conduction Mode (CCM) Operation
- Internal Soft-Start

Hardware Specification

A single-output SEPIC converter using the MAX16990 is demonstrated for a 6V to 18V input voltage range application. The output is preset to +12V using feedback resistors. The power supply delivers up to a 2A max load current. Table 1 shows an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	TYP	MAX
Input Voltage	V_{IN}	6V	12V	18V
Load Current	I_L	1A	1.5A	2A
Output Voltage	V_{OUT}	—	12V	—
Frequency	f_{SW}	—	400kHz	—
Maximum Efficiency	η	—	90%	—
Output Power	P_{OUT}	12W	18W	24W

Designed–Built–Tested

This document describes the hardware shown in Figure 1. It provides a detailed, systematic technical guide to designing a SEPIC converter using Maxim's MAX16990 current-mode controller. The power supply uses uncoupled inductors and has been built and tested, details of which follow later in this document.

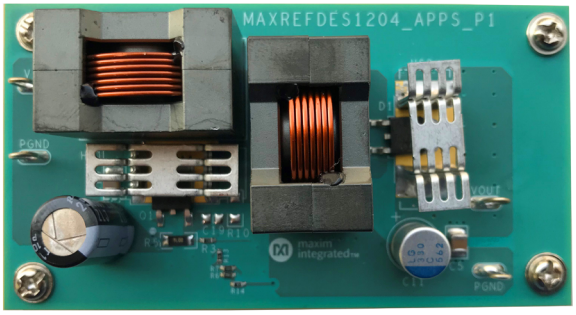

Figure 1. MAXREFDES1204 hardware.

Quick Start

Required Equipment

- DC Power Supply
- DC Electronic Load
- Multimeter
- Oscilloscope

Procedure

The reference design is fully assembled and tested. Follow these steps to verify board operation:

1) Connect a 24V supply to the input.
2) Configure the 24V supply to 12V and turn on.
3) Observe the output voltage using a multimeter. It should show 12V.
4) Connect a DC electronic load at the output and load up to 2A. Observe the output voltage regulation and output ripple.

SEPIC Principle

The single-ended primary inductor converter (SEPIC) is a type of DC-DC voltage converter (regulator) that can step-up (boost) or step-down (buck) an input voltage. A conventional buck/boost converter can do this too, but the SEPIC converter achieves this without reversing the polarity of the output. Other advantages of this topology are discussed later in this document.

The SEPIC converter architecture is originally based on the buck/boost converter, but with the addition of an extra inductor and capacitor. The series capacitor (C_S) prevents any DC current component flowing from input to output. However, the anode of the diode (D1) must connect to a known potential to operate. This is created by connecting the D1 anode to ground through an inductor (L_2).

SEPIC Operation

It is known that the average voltage across any inductor is zero. This principle can be used for inductors L_1 and L_2 of the SEPIC configuration to evaluate the magnitude of the steady-state DC voltage present across the coupling capacitor (C_S). From Figure 2 we can see that one end of inductor L_1 is connected to input voltage (V_{IN}) while the other end is connected to junction X, which consists of a switching MOSFET, SW1, and C_S (i.e., voltage on the drain of the switching MOSFET). The average voltage across L_1 can be zero only when the average voltage at this junction X is equal to V_{IN}. Similarly, one end of L_2 is connected to ground (GND) while the other end is connected to junction Y, which consists of C_S and D1. The average voltage across L_2 can be zero only when the average voltage at junction Y is also equal to zero (GND). From this analysis, we can say that the value of the DC voltage developed across the coupling capacitor ($V_{CS(AVG)}$) is:

$$V_{CS(AVG)} = V_X - V_Y$$
$$= V_{IN} - GND$$
$$= V_{IN}$$

In the light of the above discussion, we can conclude that, under steady-state condition coupling, C_S develops an average voltage equal to V_{IN} across it. Therefore, for any SEPIC design, the series coupling capacitor must have a voltage rating to endure the maximum input voltage. A SEPIC is said to be operating in CCM if the current through L_1 never falls to zero. In this document, we discuss only the CCM operation of SEPIC converter. Next, we will discuss how the SEPIC circuit behaves during the switching period on- and off-times.

When Switch Is On

When the switch is closed (on), the magnetic energy stored in both inductors (L_1 and L_2) increases. The input current (I_{IN}) builds up a field in L_1. Capacitor C_S discharges, building up a field in L_2. The diode is reverse-biased, as shown in Figure 3, so only the output capacitor (C_{OUT}) supplies current to the load.

The voltage expression for the input voltage loop can be written as follows:

$$V_{IN} = V_{L1} + V_{Q1}$$

as $V_{Q1} = 0$ (assuming negligible switch voltage drop):

$$V_{L1} = +V_{IN}$$

Similarly, the voltage expression for the middle loop can be written as:

$$V_{Q1} = V_{CS} + V_{L2}$$
$$V_{CS} + V_{L2} = 0$$
$$V_{CS} = -V_{L2}$$

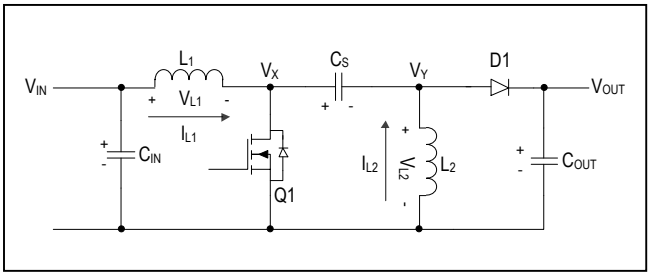

Figure 2. SEPIC circuit diagram.

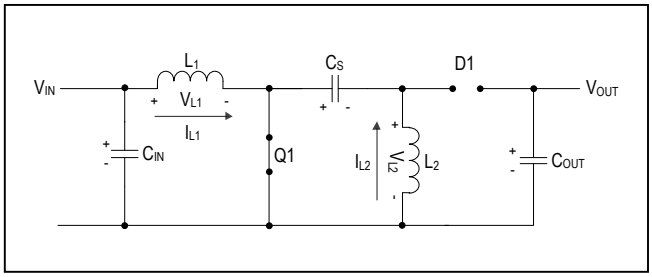

Figure 3. SEPIC circuit diagram when the switch is on.

It is evaluated already that the average voltage across C_S is equal to the input voltage. Substituting this in the above equation yields the voltage across L_2 during the on-time of the switch:

$$V_{L2} = -V_{IN}$$

Thus, during the on-time, the voltage across L_1 is equal to V_{IN}, whereas the voltage across L_2 is $-V_{IN}$ (shown in Figure 5). The current in L_1 has a slope of $+V_{IN}/L_1$ while the current in L_2 has a slope of $-V_{IN}/L_2$. Finally, because the switch is on, the drain voltage (V_D) of the switching MOSFET is at 0V.

Current flow in different nodes of the circuit can be evaluated using Kirchoff's Current Law (KCL) expressions as shown below:

$$I_{L1} - I_{Q1} - I_{CS} = 0$$

Rearranging the above expression yields the current in L_1 as follows:

$$I_{L1} = I_{Q1} + I_{CS}$$

Because the diode is reverse-biased, the current in C_S can be written as:

$$I_{CS} = -I_{L2}$$

$$I_{D1} = 0 \text{ (diode reverse-biased)}$$

The output capacitor C2 provides current to the load.

$$I_{LOAD} = I_{COUT}$$

When Switch Is Off

When the switch is open (off), the magnetic energy stored in L_1 charges C_S and supplies current to the load. The diode is forward-biased, as shown in Figure 4, and the current from L_2 continues in a negative direction and supplies the load. In the off cycle, C_S is charged so that it can recharge L_2 during the on cycle.

The input voltage loop equation can be written as follows:

$$V_{L1} + V_{CS} + V_{L2} = V_{IN}$$

Assuming negligible forward voltage drop of the diode, V_{OUT} is clamped across L_2. Therefore, during the off-time, the voltage across L_2 can be written as:

$$V_{L2} = V_{OUT}$$

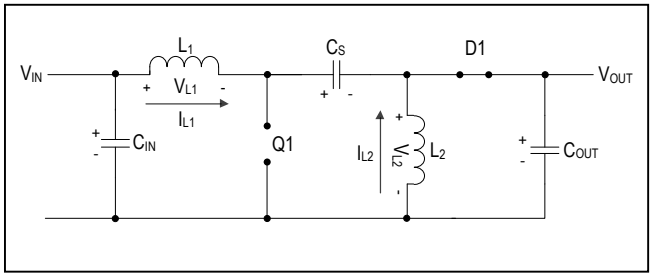

Figure 4. SEPIC circuit diagram when the switch is off.

The voltage across L_1 can be calculated by substituting values of V_{L2} and V_{CS} in the previous expression:

$$V_{L1} = V_{IN} - (V_{IN} + V_{OUT})$$
$$= -V_{OUT}$$

Thus, during the off-time, the voltage across L_1 is equal to $-V_{OUT}$, whereas the voltage across L_2 is $+V_{OUT}$. The current in L_1 has a slope of $-V_{OUT}/L_1$ while the current in L_2 has a slope of $+V_{OUT}/L_2$. See Figure 5 for inductor Turn ON and Turn OFF waveforms.

When the MOSFET switch is off, the total voltage drop over the drain voltage (V_D) of the switching MOSFET can be written as follows:

$$V_{DS} = V_{CS} + V_{DIODE} + V_{OUT}$$

Assuming negligible diode drop, the voltage stress on the drain of the MOSFET can be written as:

$$V_D = V_{IN} + V_{OUT}$$

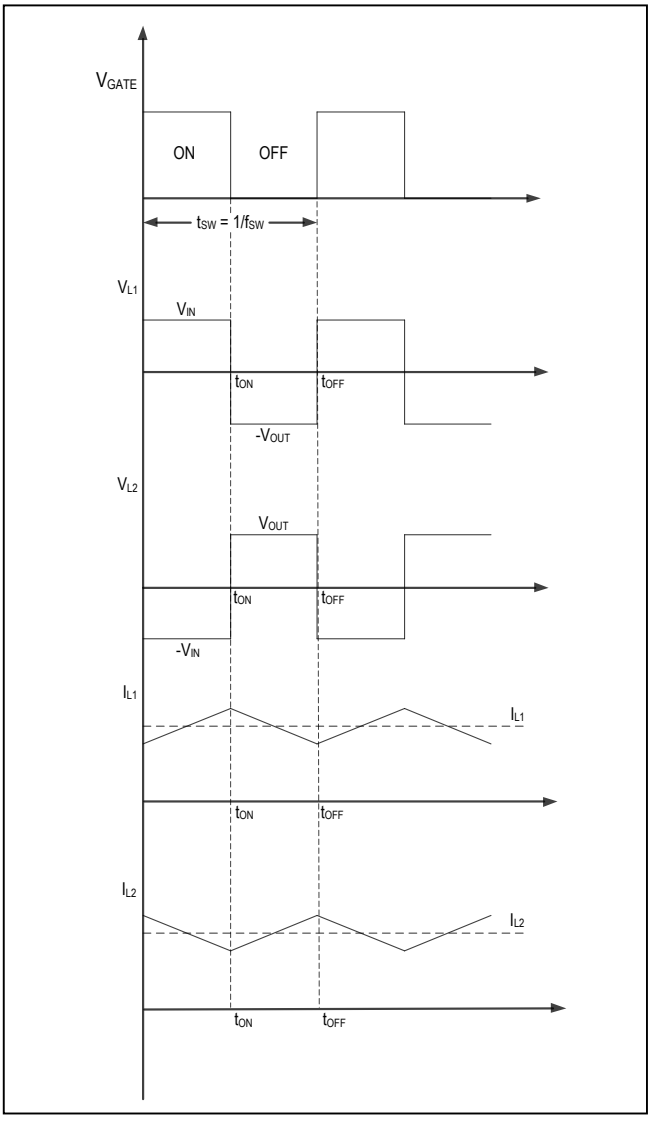

Figure 5. SEPIC inductor waveforms.

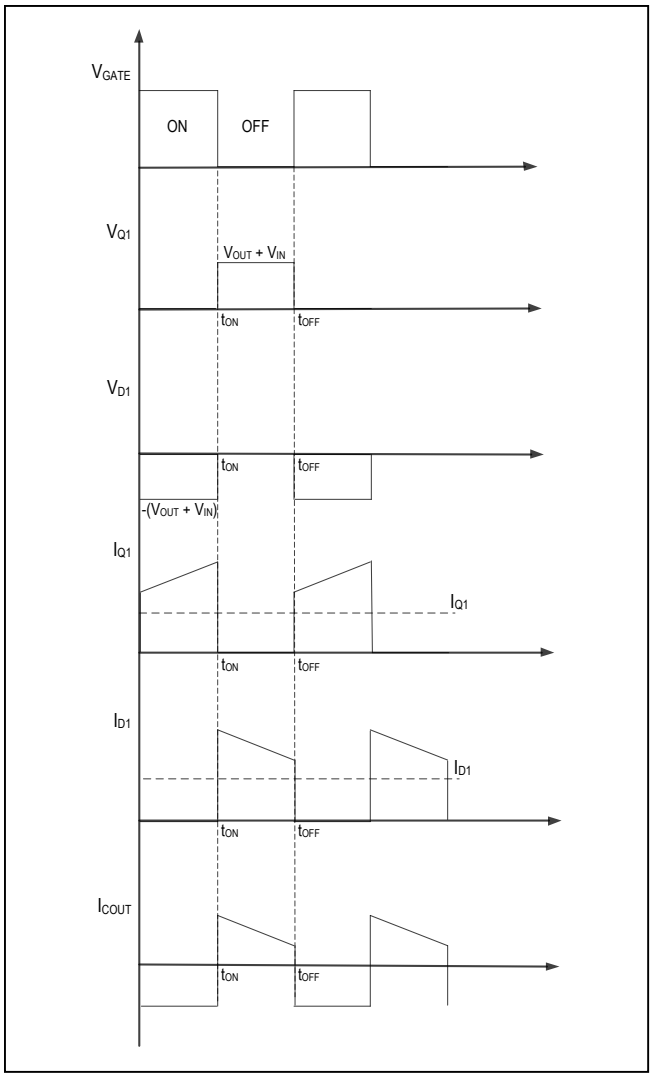

Figure 6. SEPIC switches and output capacitor waveforms.

Thus, the selected MOSFET must be able to endure the voltage stress equivalent to sum of the input and output voltages, as seen in Figure 6.

Current flowing in different nodes of the circuit can be evaluated using the KCL expressions as follows:

$$I_{IN} = I_{CS}$$

$$I_{CS} = I_{D1} - I_{L2}$$

$$I_{D1} = I_{LOAD} + I_{COUT}$$

The inductor volt-second balance expressions can be used to evaluate the voltage gain of the SEPIC converter. The volt-second balance can be used either for L_1 or L_2, and both give the same value of the voltage gain.

For L_1 it can be written as:

$$V_{IN} \times t_{ON} = V_{OUT} \times t_{OFF}$$

$$V_{IN} \times \frac{t_{ON}}{t_{SW}} = V_{OUT} \times \frac{t_{OFF}}{t_{SW}}$$

$$V_{IN} \times D = V_{OUT} \times (1 - D)$$

where D is the duty cycle of the switching period:

$$\frac{V_{IN}}{V_{OUT}} = \frac{D}{1 - D}$$

SEPIC configuration is very useful in automotive/battery applications where output voltage requirements can be less than, greater than, or equal to the input voltage of the battery.

Design Procedure for SEPIC Converter Using MAX16990

This document is primarily concerned with the design of the power stage and the feedback loop, and is intended to complement the information contained in the **MAX16990** data sheet. For details on how to set up supervisory and protection functions of the controller, see the MAX16990 data sheet. All equations used in design calculation are based on the equations from Maxim **Application Note 5740**.

The switching frequency is determined by the operating range of the controller used in our design. The MAX16990 has a 100kHz to 1MHz frequency range. For this design, we have selected a switching frequency (f_{SW}) of 400kHz.

The design is optimized for 12V output.

Step 1: Calculations of Inductor Current Range

Suppose an initial design efficiency of 90% and calculate the input current range that is equivalent to the primary inductor (L_1) current operating range. The minimum average inductor current (I_{INAVG_MIN}) can be calculated as follows:

$$I_{INAVG\_MIN} = I_{L1AVG\_MIN} = \frac{V_{OUT} \times I_{OUTMIN}}{V_{INMAX} \times \eta}$$

$$= \frac{12V \times 1A}{6V \times 0.9} = 0.741A$$

Similarly, the maximum average inductor current can be calculated as follows:

$$I_{INAVG\_MAX} = I_{L1AVG\_MAX} = \frac{V_{OUT} \times I_{OUTMAX}}{V_{INMIN} \times \eta}$$

$$= \frac{12V \times 2A}{6V \times 0.9} = 4.444A$$

The average current range of the secondary inductor (L_2) is equal to the minimum and maximum output current:

$$I_{L2AVG\_MIN} = I_{OUT\_MIN} = 1A$$

$$I_{L2AVG\_MAX} = I_{OUT\_MAX} = 2A$$

Step 2: Duty-Cycle Range Calculation

Next, we evaluate the duty-cycle range to calculate the D_{MIN} and D_{MAX} at which the regulator operates. This can be determined with the following two equations:

$$D_{MIN} = \frac{V_{OUT}}{V_{INMAX} + V_{OUT}} = \frac{12V}{18V + 12V} = 0.4$$

$$D_{MAX} = \frac{V_{OUT}}{V_{INMIN} + V_{OUT}} = \frac{12V}{6V + 12V} = 0.667$$

We make a more accurate estimate of the duty-cycle range later. This calculation is to ensure that the estimated duty-cycle range is within the specification of the MAX16990 (4% to 93%).

Step 3: Inductor Selection

The minimum required values for L_1 and L_2 can be calculated from the expressions below:

$$L_1 = \frac{V_{OUT} \times (1 - D_{MIN})}{2 \times f_{SW} \times I_{INAVG\_MIN}} = \frac{12V \times (1 - 0.4)}{2 \times 400k\Omega \times 0.741A} = 12.14\mu H$$

$$L_2 = \frac{V_{OUT} \times (1 - D_{MIN})}{2 \times f_{SW} \times I_{OUT\_MIN}} = \frac{12V \times (1 - 0.4)}{2 \times 400k\Omega \times 1A} = 9\mu H$$

We must select a commercial value that is always higher than the critical inductance. This guarantees CCM operation throughout the application range. Hence, we select the following values for L_1 and L_2:

$$L_1 = L_2 = 15\mu H$$

Inductor ripple current ratio (LIR) is another parameter to remember when choosing proper inductors. It is defined as the ratio of the peak-to-peak inductor current (I_{L_PK-PK}) to the average input current (I_{L_AVG}):

$$LIR = \frac{I_{L\_PK-PK}}{I_{L\_AVG}}$$

The relationship between the inductors (L_1 and L_2) and LIR is shown in the following equations:

$$LIR_{L1} = \frac{V_{OUT} \times (1 - D_{MAX})}{L_1 \times f_{SW} \times I_{INAVG\_MAX}} = \frac{12V \times (1 - 0.667)}{15\mu F \times 400k\Omega \times 4.444A} = 0.149$$

$$LIR_{L2} = \frac{V_{OUT} \times (1 - D_{MAX})}{L_2 \times f_{SW} \times I_{OUT\_MAX}} = \frac{12V \times (1 - 0.667)}{15\mu F \times 400k\Omega \times 2A} = 0.333$$

This results in the inductors' peak currents of:

$$I_{L1\_PK} = I_{INAVG\_MAX} \times \left[1 + \frac{LIR_{L1}}{2}\right] = 4.444A \times \left[1 + \frac{0.149}{2}\right] = 4.775A$$

$$I_{L2\_PK} = I_{OUT\_MAX} \times \left[1 + \frac{LIR_{L2}}{2}\right] = 2A \times \left[1 + \frac{0.333}{2}\right] = 2.333A$$

Based on the calculated specs for the inductors, the Coilcraft® VER2923-153KL was selected.

Step 4: MOSFET and Diode Selection

The next step is to calculate the MOSFET and diode. This selection requires MOSFET and diode rating calculations. The peak drain current that flows into the MOSFET (I_{MOSFET_PK}) is the sum of inductor peak currents, which is also the same as the diode peak current (I_{DIODE_PK}).

$$I_{MOSFET\_PK} = I_{DIODE\_PK} = I_{L1\_PK} + I_{L2\_PK} = I_{DIODE\_PK} = 4.775A + 2.333A = 7.108A$$

$$I_{MOSFET\_VALLEY} = I_{L1\_VALLEY} + I_{L2\_VALLEY} = 4.112A + 1.667A = 5.788A$$

$$I_{MOSFET\_RMS} = \sqrt{\frac{D_{MAX} \times \left[I_{MOSFET\_PK}^2 + I_{MOSFET\_VALLEY}^2 + (I_{MOSFET\_PK} \times I_{MOSFET\_VALLEY})\right]}{3}} = 5.353A$$

$$V_{DS\_MAX} = V_{INMAX} + V_{OUTMAX} = 18V + 12V = 30V$$

$$V_{D\_MAX} = (V_{INMAX} + V_{OUTMAX}) = 30V$$

Based on this information, the Infineon® IPD30N10S3L nMOS rated for a drain current of 30A was selected. The typical $R_{DS(ON)}$ of this transistor is 32.2mΩ with a V_{GS} = 5V, which is the drain-source voltage provided by the MAX16990. The rated drain-source voltage for this device is 100V, which is higher than the maximum drain-source voltage calculated by the V_{DMAX} expression. The STM FERD20H100S 100V, 20A diode was selected.

Step 5: Series Capacitor Selection

The series capacitor is charged at a DC voltage equal to the input voltage. It must carry the primary inductor current during the off-time and the secondary inductor

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current during the on-time. This makes this capacitor selection challenging, even somewhat tricky.

As the first requirement, the voltage rating of the series capacitor must be higher than the maximum input voltage (V_{INMAX}).

The RMS current flowing through the capacitor (I_{CS_RMS}) is given by the following equation:

$$I_{CS\_RMS} = I_{OUTMAX} \times \sqrt{\frac{D_{MAX}}{1-D_{MAX}}}$$
$$= 2A \times \sqrt{\frac{0.686}{1-0.686}} = 2.958A$$

The ripple across the series capacitor is determined by the capacitor value and its equivalent series resistance (ESR). Assuming a 1% voltage ripple across the series capacitor due to the ESR, the series capacitor ESR must be lower than:

$$ESR_{CS} < MIN\left[\frac{0.01 \times V_{INMIN}}{I_{L1\_PK}}, \frac{0.01 \times V_{INMIN}}{I_{L2\_PK}}\right]$$
$$< MIN\left[\frac{0.01 \times 6V}{4.7737A}, \frac{0.01 \times 6V}{2.3297A}\right]$$
$$< [0.0125, 0.0257]$$

Finally, the minimum required value of series capacitor can be calculated as follows:

$$C_S = \frac{I_{OUTMAX} \times D_{MAX}}{0.05 \times V_{INMIN} \times f_{SW}}$$
$$= \frac{2A \times 0.686}{0.05 \times 6V \times 400k\Omega} = 11.5\mu F$$

Step 6: Output Capacitor Selection

Selecting the correct output capacitor (C_{OUT}) and its related ESR is very important for minimizing output voltage ripple (V_{OUT_RIPPLE}). Assume that V_{OUT_RIPPLE} is equally distributed between the voltage drop (which is due to the capacitor discharging during off-time) and the ESR voltage drop. The minimum capacitance and the maximum ESR for C_{OUT} can be calculated as follows:

$$C_{OUT} > \frac{I_{OUTMAX} \times D_{MAX}}{0.5 \times V_{OUT\_RIPPLE} \times f_{SW}}$$
$$> \frac{2A \times 0.686}{0.5 \times 0.12V \times 400k\Omega} = 57.5\mu F$$

$$I_{C_{OUT}\_RMS} = I_{OUTMAX} \times \sqrt{\frac{D_{MAX}}{1-D_{MAX}}}$$
$$= 2A \times \sqrt{\frac{0.686}{1-0.686}} = 2.958A$$

$$ESR_{C_{OUT}} < \frac{0.5 \times V_{OUT\_RIPPLE}}{I_{L1\_PK} + I_{L2\_PK} - I_{OUTMAX}}$$
$$< \frac{0.5 \times 0.12V}{4.7737A + 2.3297A - 2A} = 0.0117\Omega$$

Step 7: Input Capacitor Selection

The input current to a boost converter is almost continuous, and the RMS ripple current at the input capacitor is low. Calculate the minimum input capacitor value:

$$C_{IN} = \frac{\Delta I_{L1} \times D_{MAX}}{4 \times f_{SW} \times \Delta V_{IN}}$$
$$= \frac{0.662 \times 0.667}{4 \times 400k\Omega \times 0.12} = 2.3\mu F$$

Step 8: Sense Resistor Calculation

Because I_{MOSFET_PK} has been calculated, it is possible to select the sense resistor (R_{SENSE}). The MAX16990 triggers the current limit when the voltage drop on the ISNS pin reaches 212mV (min). This voltage is due to the drop on R_{SENSE} and the drop on the slope resistor (R_{SLOPE}), which is used for slope compensation. It is recommended to leave 100mV of headroom for slope compensation. Therefore, R_{SENSE} should generate a voltage drop of 112mV at the current-limit threshold. In the following equation, R_{SENSE} is calculated with a current-limit threshold that is 20% higher than I_{MOSFET_PK}.

$$R_{SENSE} = \frac{0.112}{1.2 \times I_{MOSFET\_PK}}$$
$$= \frac{0.112}{1.2 \times 7.103A} = 13m\Omega$$

Step 9: Type II Voltage Compensation and Slope Compensation

Using the electronic calculator from **Application Note 5740**, it is now possible to extrapolate the following component values for compensation. The compensation network is designed for worst-case 6V input voltage and 2A output current.

For a 12V output, we obtained a 2kHz crossover frequency with a phase margin of approximately 60° by selecting the following components for Type II voltage compensation and slope compensation:

R_{SLOPE} = 1.3kΩ

C_{COMP} = 16nF

R_{COMP} = 10kΩ

C_{2COMP} = 680pF

Design Resources

Download the complete set of **Design Resources** including the schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/19	Initial release	—