32-Channel Industrial Digital I/O Module
MAXREFDES1165

Overview

The MAXREFDES1165 is a complete, 32-channel industrial digital I/O module comprising 16 digital inputs (DIs) and 16 digital outputs (DOs) that is built and tested in an industrial form factor to meet transient immunity standards such as IEC 61000-4.

The MAXREFDES1165 is a proven design that provides the hardware and software necessary to demonstrate the MAX22190 octal industrial digital input device with diagnostic features, and the MAX14915 octal industrial digital output with high-side switches. In this reference design, two MAX22190s are configured in daisy-chain mode, and two MAX14915s are configured in addressable SPI mode. Galvanic isolation is provided by the MAX14483 and MAX12930 to isolate the data from the logic (SPI master) and field (24V) sides.

The MAXREFDES1165 has a 12-pin Pmod™-compatible connector (CNT1) for external SPI communication. For testing purposes, the reference design uses Maxim's USB2PMB2# adapter board that receives commands from a PC through the USB port and translates them into an SPI interface. Alternatively, the user can connect the reference design board to any Pmod-compatible board, such as an FPGA or microcontroller system, and write their own software for controlling the MAX22190 and MAX14915.

Other features include the following:

- 32 Digital I/Os: 16 Inputs and 16 Outputs
- High Integration Reduces BOM Count and PCB Space
- Fault Tolerant with Built-In Diagnostics
- Robust Design to Meet IEC 61000-4

Hardware Specification

The MAXREFDES1165 features 16 digital inputs (MAX22190) and 16 digital outputs (MAX14915), and it supports isolated SPI data. Both the MAX22190 and MAX14915 communicate with the host controller utilizing the same isolated SPI bus with separate chip-select ($\overline{CS}$) signals. Each MAX22190 translates eight industrial inputs to an SPI compatible output. Each MAX14915 provides power to the external loads in accordance with the command received from the host controller. In addition, the host controller receives all available diagnostics information. The MAX14483 and MAX12930 are used together to provide data signal isolation for SPI, as well as a Pmod-compatible connector for SPI communication with the host. The system is powered by 24V DC.

Designed–Built–Tested

This reference design describes the hardware shown in **Figure 1**. It provides a detailed, systematic technical guide to design an industrial digital I/O module with 16 digital inputs and 16 digital outputs. The reference design has been built and tested, details of which will follow later in this document.

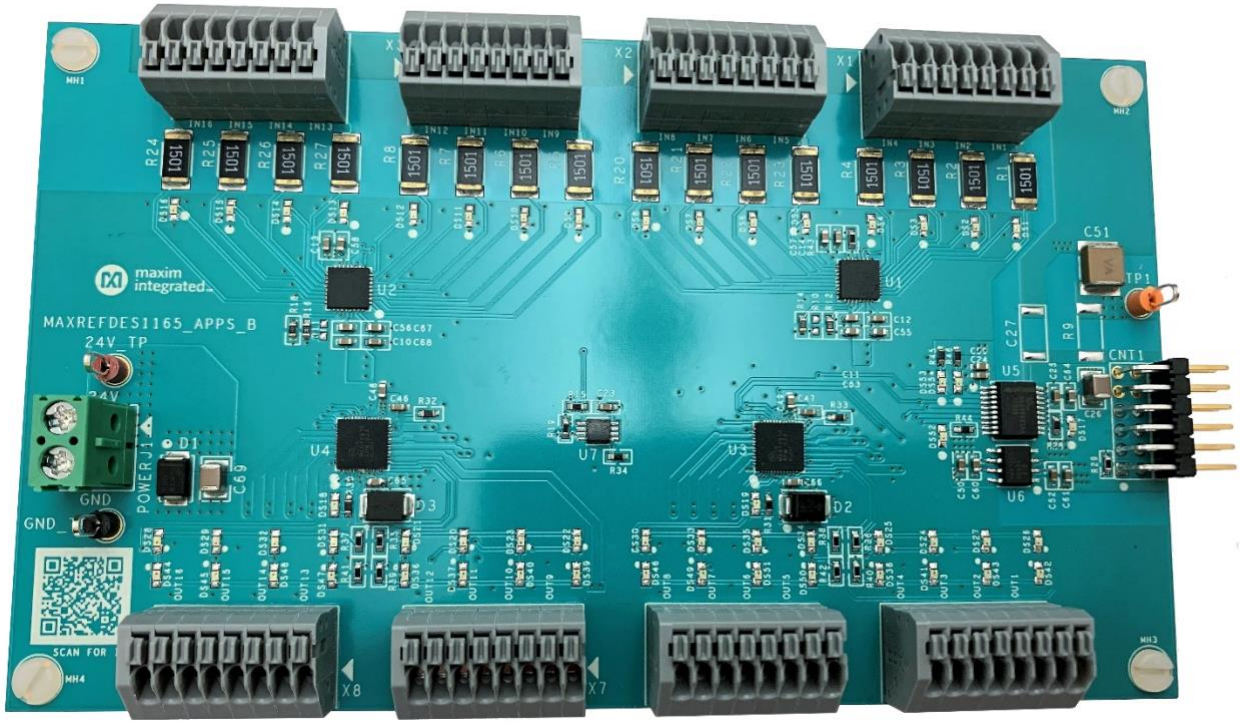

Figure 1. MAXREFDES1165 hardware.

Introduction

Advanced factory automation solutions, such as Industry 4.0, require an increasing number of digital sensors and actuators, which are typically controlled using a digital I/O module within a programmable logic controller (PLC). As a leading provider of industrial digital I/O ICs, Maxim also provides complete reference design solutions to help our customers improve their time to market. These proven designs demonstrate the device's optimal electrical performance and cover all of the hardware requirements needed for compliance with transient immunity standards such as IEC 61000-4.

The MAXREFDES1165 reference design consists of two MAX22190 octal industrial digital input with diagnostics devices and two MAX14915 octal digital output devices, with the MAX14883 and MAX12930 as the galvanic isolation devices between the field side and logic side. **Figure 2** shows the system block diagram.

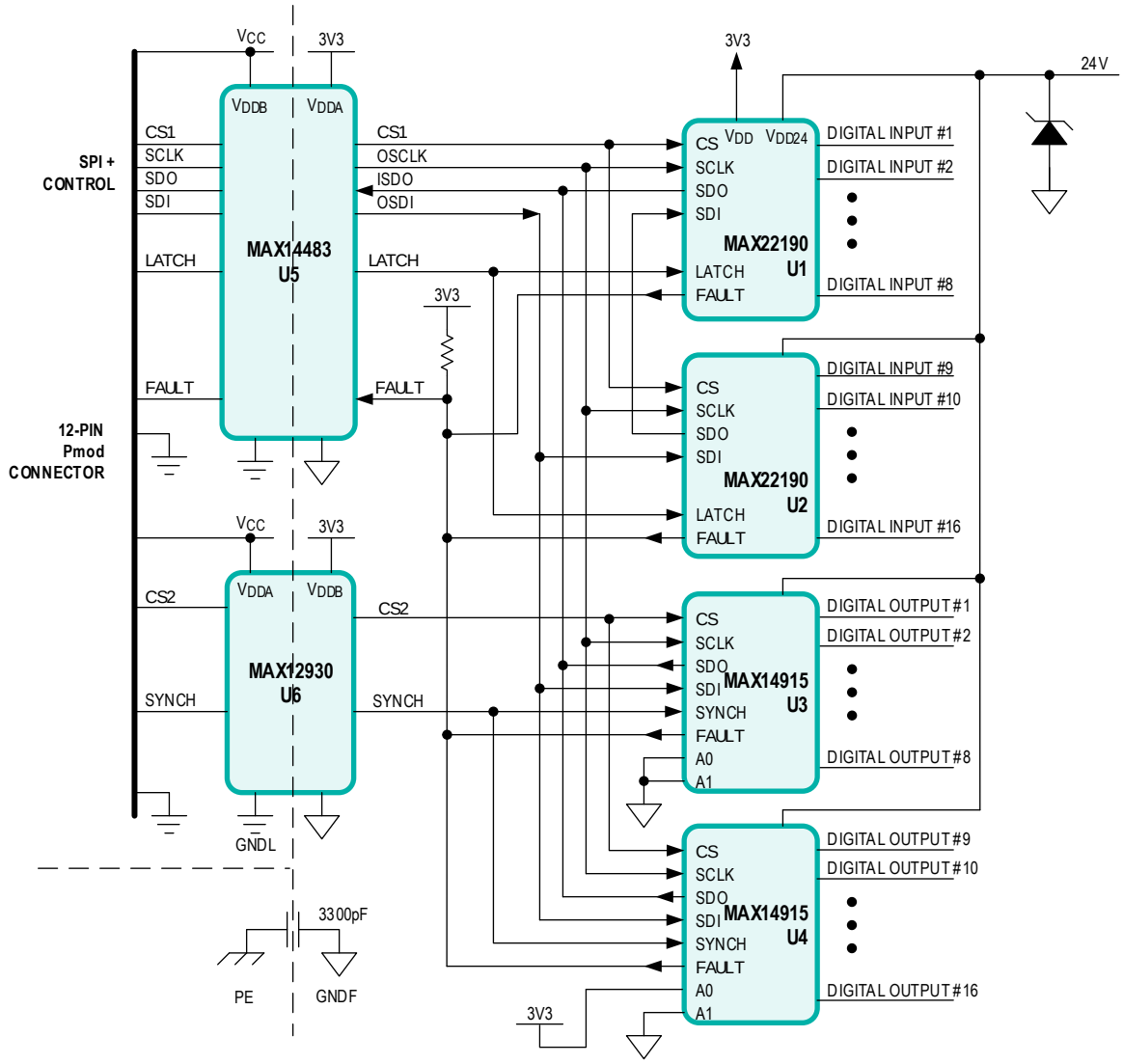

Figure 2. MAXREFDES1165 block diagram.

Detailed Description

Hardware

This section discusses the design components of the MAXREFDES1165. **Figure 2** shows the main hardware blocks.

Power Supply

The system is powered by a 24V field power supply. The 24V DC can come from an AC-DC module connected to the POWERJ1 terminal block on the board. Alternatively, +24V can be supplied from a bench power supply and connected to the 24V_TP and GND_TP test points. It is important to ensure that the power supply has enough capability to support any digital output load current being switched. Each MAX14915 channel is specified to deliver up to 700mA continuous current, so potentially the 24V supply current can be as high as 11.2A with 16 channels driving their loads simultaneously.

The MAX22190 (U1) uses its integrated LDO to generate +3.3V to power logic interfaces on the field side of the galvanic isolators (U5 and U6). The Pmod connector CNT1 supplies a 1.8V to 5.5V supply (V_{CC}) which powers the other (logic) side of the galvanic isolators.

Digital Inputs

The MAXREFDES1165 implements a 16-channel digital input using two MAX22190s. The MAX22190 senses the digital input state (on = logic 1 or off = logic 0) of each channel and serializes this to data bytes in the MAX22190 registers. All inputs are simultaneously latched by the assertion of either LATCH or CS, and the data is made available in a serialized format through the SPI interface. To support 16 channels, two MAX22190s are daisy-chained and communicate with a single SPI master. In this design, the SPI interface is configured as SPI Mode 2 (M1 = 1, M0 = 0), which indicates that SPI frame length is 24 bits for each device including CRC check code. The full SPI interface details and timing diagrams are included in the MAX22190 data sheet.

In this design, the MAX22190 is configured for Type 1 and Type 3 inputs with a 1.5kΩ input resistor and 7.5kΩ current-setting resistor at each REFDI pin (R13 and R17). The MAX22190 can also be configured for Type 2 inputs by connecting two channels in parallel and changing the REFDI resistor to 5.2kΩ and the input resistors to 1kΩ. Refer to the MAX22190 IC data sheet for details. The data sheet explains how to select the current sinking value by choosing the REFDI resistor value and the input resistor value to ensure that the current at the on and off trip points, as well as the voltage at the trip points, satisfy the requirements of IEC 61131-2 for Type 1 and Type 3 inputs, or for Type 2 inputs. Each input drives a LED (DS1–DS16) to provide an indication of each input channel state, powering the LED from the input signal without increasing overall power dissipation.

Each input channel (IN1–IN16) has a programmable filter, and the input data may be filtered to reduce noise or it may be read directly for more rapid response. Bit FBP in the corresponding FLT_ register is used to bypass the filter or to enable the filter. Some digital input devices use an input capacitor on each digital input channel to reduce the input noise. However, for the MAX22190, it is not recommended to populate the input capacitors for general use due to its integrated surge protection structures. Instead it is recommended to use the internal programmable digital filter to filter the input glitches. Refer to the MAX22190 data sheet and register tables for details.

Each input channel also includes a second threshold comparator that can be individually enabled to verify the integrity of field wiring. The comparator senses the presence of the small input current produced by a device, such as a two-wire proximity sensor in its open state, or the current from an open switch with a diagnostic resistor placed across it. The wire-break current threshold is set to 100µA by placing a resistor (R14 or R18 = 24kΩ) between the REFWB pin and GND for each MAX22190 device.

The MAX22190 has extensive built-in diagnostic features for die temperature, field supply, and input wiring. The FAULT pin is an open-drain output that can be wire ORed with other open-drain outputs and used to notify the host processor of a fault. When enabled, the FAULT pin goes low to indicate that one or more of the flags in the FAULT1 register have been set and all fault status bits can be read through the SPI interface. Additional diagnostics that assert the FAULT pin include the REFDI and REFWB resistor status, SPI CRC check, and power-on reset conditions. Refer to the MAX22190 data sheet for a full description of all these diagnostic features.

Digital Outputs

Two MAX14915s implement 16 digital output channels (OUT1–OUT16). The MAX14915 has eight high-side switches, which are specified to deliver up to 700mA (min) continuous current. The MAX14915 devices are configured to operate in addressed SPI mode to allow access to 16 output channels through a single SPI interface and a shared CS signal (CS2). Daisy-chain mode does not provide access to many of the MAX14915 key features, such as extensive diagnostics and configurability. Addressed SPI offers the advantage of direct chip access and access to the global diagnostics in the same SPI cycle. Refer to the Serial Interface section in the MAX14915 data sheet for details.

In this design, CRC error detection is enabled by setting the CRCEN input high. A CRC frame check sequence (FCS) is sent along with each serial transaction. The FAULT pin is an open-drain output that transitions to active low when a fault condition is detected. The source of faults and how to mask or read them is covered in detail in the MAX14915 data sheet.

The SYNCH pin can be used to enable synchronous update of all outputs. On the rising edge of the SYNCH logic input, all OUT_ switches change to the new state previously programmed into the SetOUT register. If SYNCH is held high, the outputs change state immediately when the SetOUT register is written to.

A 4x4 LED crossbar matrix integrated within the MAX14915 drives 16 LEDs to indicate the per-channel output status and fault conditions.

Galvanic Isolation

The MAX14483 is a 6-channel, 3.75kV$_{RMS}$ digital galvanic isolator and is used to provide data signal isolation for the SPI interface, including FAULT and LATCH control signals for the MAX22190s. The MAX12930 is a 2-channel, 3kV$_{RMS}$ digital galvanic isolator and is used to provide isolation for the SYNCH and CS2 signals that control the MAX14915s.

For this design, the IFAULT input of the MAX14483 is wire-ORed from all four FAULT signals of the four ICs (MAX22190/MAX14915). The OFAULT output of the MAX14483 is used to notify the host processor of a fault. The four READY signals from the MAX22190s and MAX14915s are also ORed together through U7 (SN74LVC2G32) to the IRDY input of the MAX14483 isolator. The logic-side ready signal SAA notifies the user that the field side is ready for operation by turning on the DS17 LED.

Pmod Connector

The Pmod-compatible connector (CNT1) is used to communicate with the SPI host. See the Pmod connector pinout in **Figure 3**. The user can interface to this connector with a USB2PMB2# adapter or any FPGA or microcontroller board equipped with a Pmod-compatible connector.

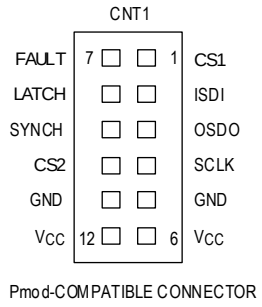

Figure 3. MAXREFDES1165 Pmod pinout.

Design Verification Testing

Load Testing

The MAXREFDES1165 was tested in Maxim's laboratory at an ambient temperature of +25°C (unless otherwise noted) for common industrial applications that use digital I/Os. The test methodology and results are presented in this section.

Test Equipment Used

- MAXREFDES1165 and USB2PMB2# Adapter
- MAXREFDES1165 GUI
- B&K Precision® 8540 DC Electronic Load
- Fluke® Precision Temperature Calibrator
- Inductive and Incandescent Lamp Loads
- 24V, 15A Supply
- Oscilloscope

Digital Output Continuous Load Test

The MAX14915 has eight high-side switches specified to deliver up to 700mA continuous current. In this test, all 16 outputs were loaded to 700mA, as shown in **Figure 4**. The test was run at room temperature and a FLIR image (**Figures 5a and 5b**) was taken to show the heat signature from the power dissipation for each IC (U3 and U4). In addition, the individual IC case temperatures were measure with a Fluke precision temperature calibrator. From an ambient temperature of +24.1°C, U3 temperature only increased to +33.3°C and U4 temperature increased to +33.2°C, which closely matched the calculated case temperature based on given specifications for on-resistance, load current, and package thermal characteristics θ_{JA} and θ_{JC}.

In addition, an ammeter was used to measure the current for each output channel, and driver on-resistance R_{OUT_HS} was calculated and compared to the MAX14915 data sheet specification (**Table 1**).

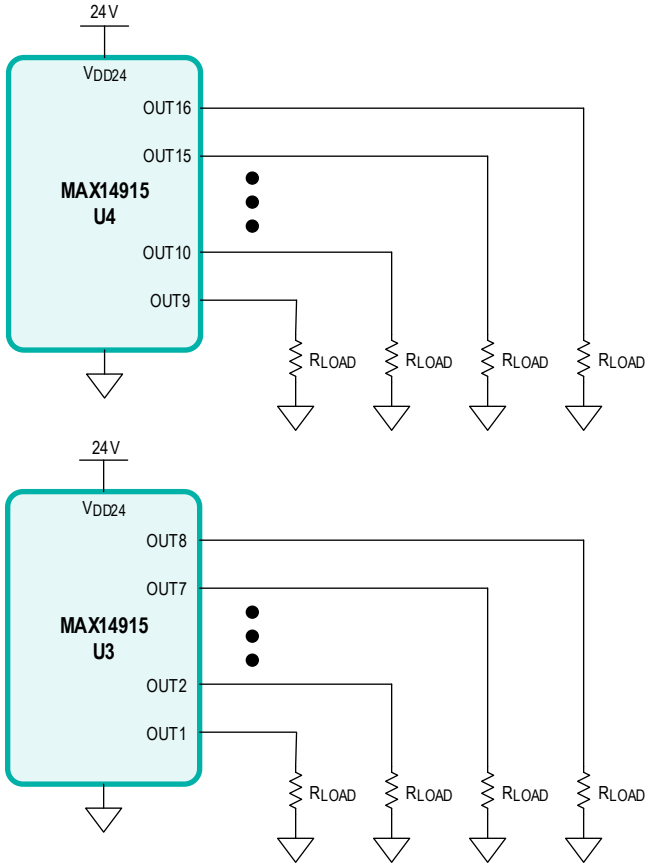

Figure 4. Digital output continuous load test.

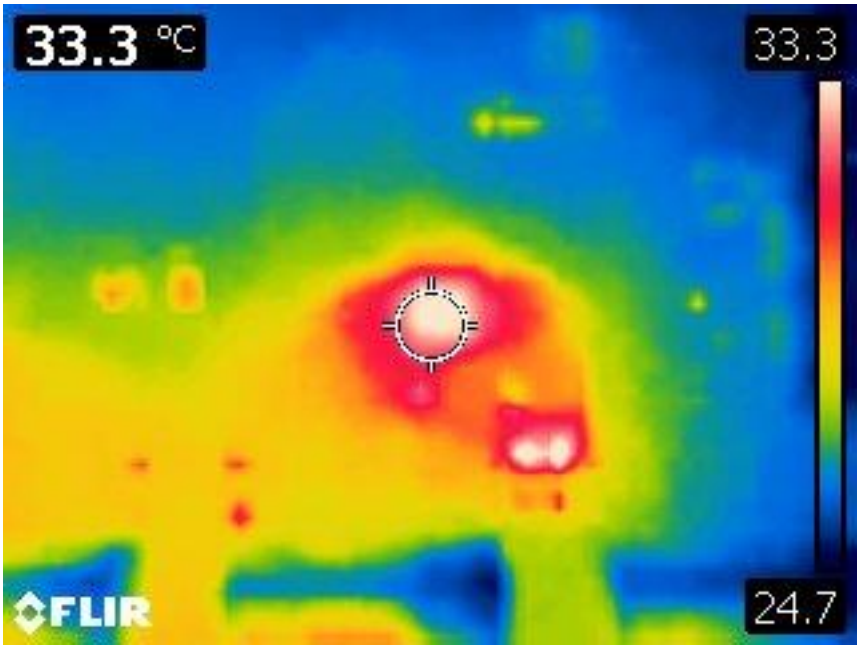

Figure 5a. MAXREFDES1165 (U3) digital output continuous load thermal performance.

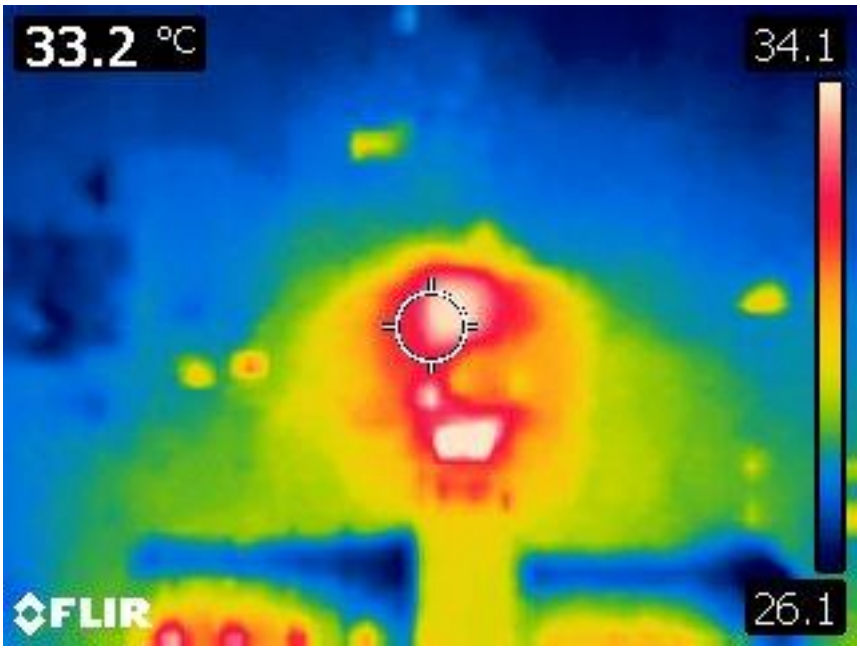

Figure 5b. MAXREFDES1165 (U4) digital output continuous load thermal performance.

Table 1. Per Channel On-Resistance

DEVICE	SPECIFICATION	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
U3	I (mA)	699	699	699	699	699	699	699	699
	R_{OUT_HS} (mΩ)	114.6	114.4	114.6	114.6	114.6	114.4	114.6	114.2
U4	I (mA)	699	699	699	699	699	699	699	699
	R_{OUT_HS} (mΩ)	114.6	114.4	114.6	114.6	114.4	114.6	114.4	114.4

Summary: The MAX14915 output driver on-resistance was within data sheet limits, and the board ran for over 24 hours without overheating with no register faults observed.

Switching an Inductive Load with Fast Demagnetization

A DC reactor with an inductance of 1.5H and a resistance of 26.7Ω was connected to output channel 1, as shown in **Figure 6**, and this output was switched on and off at 1Hz frequency. An oscilloscope with a current probe was used to monitor the output voltage and current with the result shown in **Figure 7**.

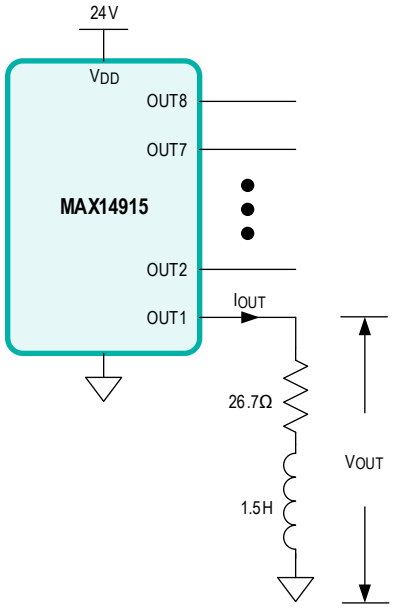

Figure 6. MAXREFDES1165 switching inductive load setup.

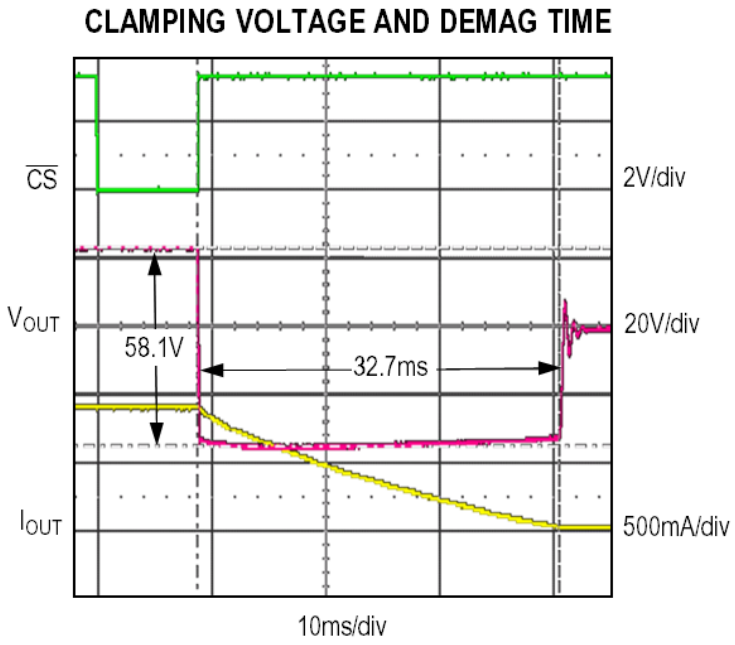

Figure 7. MAXREFDES1165 switching inductive load with fast demagnetization.

Figure 7 shows the clamping voltage and demagnetization. The green waveform represents CS signal, magenta represents output voltage, and yellow represents output current. The OUT_Clamp voltage (V_{CLAMP}) was measured at 58V and demagnetization time at 32ms.

The theoretical demagnetization time is calculated at 30ms using the following equation and 24V for V_{DD} and 58V for V_{CLAMP}:

$$t_{DEMAG} = \frac{L}{R_{LOAD}} \times \ln\left(1 + \frac{V_{DD}}{V_{CLAMP} - V_{DD}}\right)$$

Summary: The fast demagnetization circuitry within MAX14915 allowed it to switch off inductive loads fast. The high clamp voltage due to Maxim's proprietary process technology allows the MAX14915 to quickly discharge (demagnetize) an inductive load.

Incandescent Lamp Load Turn-On

A 24V/6W incandescent lamp load (two 12V/3W bulbs in series) was connected to output 1 of the MAX14915, as shown in in **Figure 8**. The cold (room temperature) filament resistance was measured at 13Ω in total using a simple DMM.

An oscilloscope with a current probe was used to monitor the output voltage and current, as well as CS2 and FAULT signals, with the result shown in **Figure 9**.

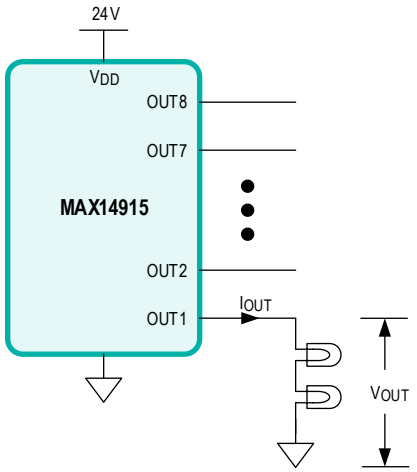

Figure 8. MAXREFDES1165 incandescent lamp load setup.

Incandescent lamps initially draw high currents while their filament is cold, and this turn-on current reduces as the filament heats up. The MAX14915 automatically detects the presence of lamp loads. The MAX14915 monitors the load voltage to determine if it is an incandescent lamp and, if a lamp load is detected, the overtemperature and overload warnings are disabled for a duration of 200ms. The lamp load detection is transparent to the user and is not signaled.

Figure 9 shows a green trace for the FAULT signal, aqua represents CS, magenta represents output voltage, and yellow represents output current. When the output driver is initially turned on, its output current tries to reach 2A (approximated from 24V/13Ω) but is current limited around 1A, and the voltage across the load is measured at 12.4V. The MAX14915 detects the load as a lamp and masks the overcurrent and overtemperature faults for the initial 200ms. After 5ms, the output voltage has reached 24V and, as the filament temperature increases (along with its resistance), the output current decreases over time to normal operating level of approximately 0.25A (6W/24V).

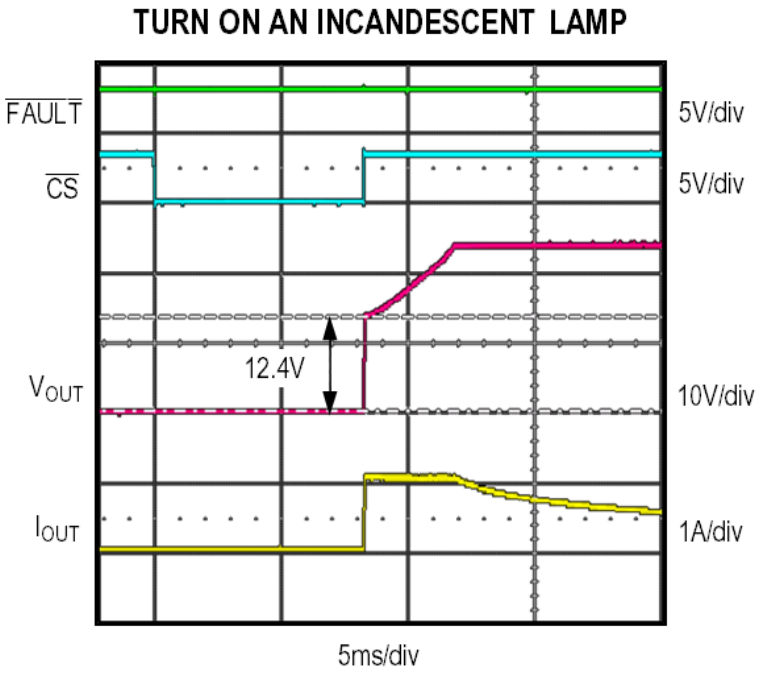

Figure 9. MAXREFDES1165 incandescent lamp load turn-on waveforms.

Summary: The MAX14915 detects a lamp load and masks the FAULT signal during the initial turn-on when the current is limited and the device could overheat.

Digital Output Active Current Limiting

Each high-side switch features active current limiting. When the load current exceeds 1A (typ), the load current is limited by the high-side switch. If the load impedance tries to draw higher current, the voltage across the high-side FET switch increases and the temperature of the FET increases in accordance with the FET's power dissipation. When an OUT_ channel shows an overcurrent, the CL_ bit is set in the CurrLimF register.

For this test, a DC load was connected to one output channel, leaving the other seven channels open. The load was varied to provide the graph in **Figure 10** showing output current vs. load resistance.

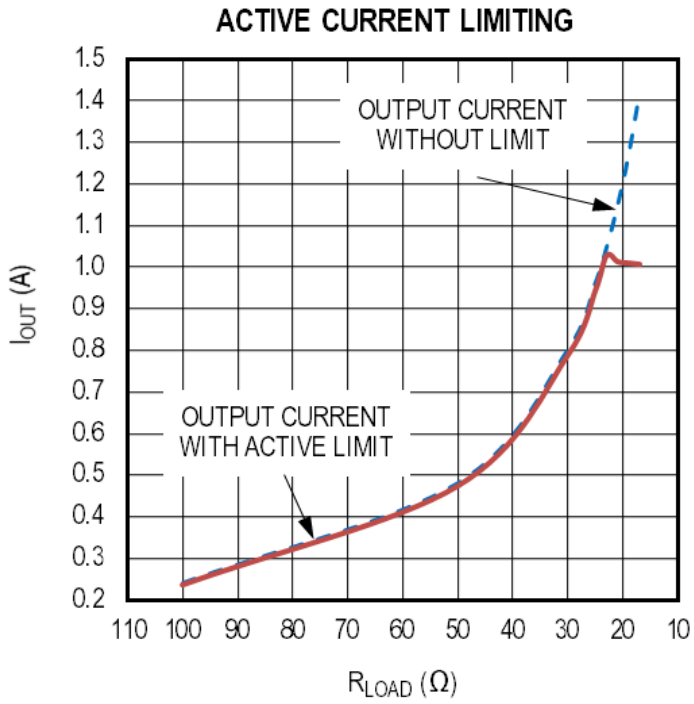

Figure 10. MAX14915 active current limiting.

Summary: The MAX14915 load current is actively limited by the high-side switch when it exceeds the limit of 1A (typ). The red line shows the load current is limited when the load resistance drops below 23Ω. The blue dotted line shows an ideal I-R curve in which the load current continues to increase as load resistance decreases.

Digital Output Per-Channel Thermal Shutdown Protection

Outputs 1–7 are connected to resistive loads so each channel draws approximately 700mA (i.e., below the current-limit region) and are switched on/off at a rate of 100Hz. Output 8 was shorted to GND as shown in **Figure 11**, and the output waveforms are shown in **Figure 12**.

Each high-side switch features active current limiting. When an OUT_ channel shows an overcurrent, the CL_ bit is set in the CurrLimF register and the FAULT output goes low – note overcurrent fault is enabled by default. For this test we set CurrLimM bit = 0 to mask or disable the overcurrent interrupt, thereby ensuring that if the FAULT output is pulled low it is due to the channel thermal overload (and ThrmShut bit is also set).

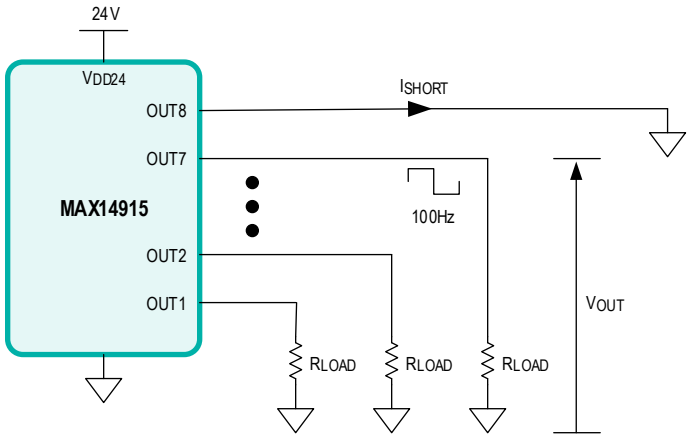

Figure 11. MAXREFDES1165 per channel thermal shutdown protection setup.

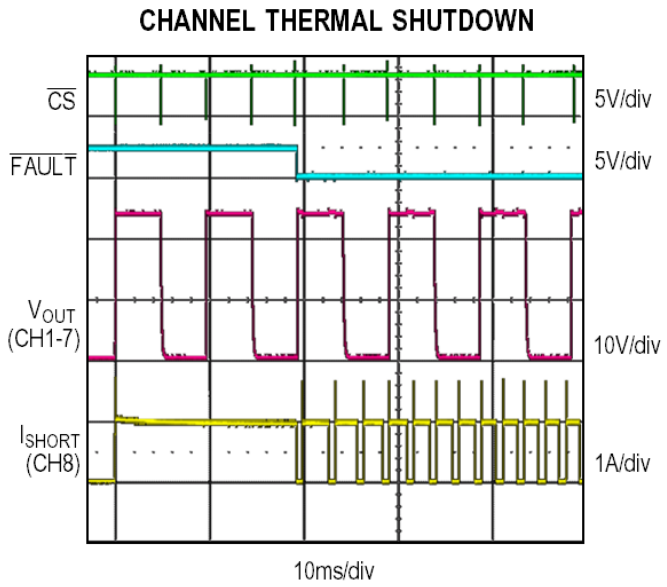

Figure 12. MAXREFDES1165 per channel thermal shutdown protection.

Summary: The output current waveform for channel 8 shows how, after the short circuit is detected, the output current is limited to approximately 1A. As the output switch heats up, channel thermal shutdown takes place, as indicated by the FAULT output being asserted low and bit OVL8 in OvlChF register is set. Channel 8 automatically switches between on and off states (thermal cycling) to prevent overheat damaging the device. Note that the FAULT output stays low until the fault condition is removed and the fault bits cleared. Despite this overload condition on channel 8, the other channels operate normally, toggling at 100Hz.

Digital Output IC Thermal Shutdown Protection

Outputs 1–8 were connected to 1kΩ resistive loads and the ambient temperature was gradually increased. During this time, the fault bits ThErr and ThrmShutd were monitored, as well as the internal voltage regulator output, V_A.

The results are shown in **Table 2**.

Table 2. IC Thermal Shutdown

TEMPERATURE	OUT 1-8	FAULT BITS (ThErr and ThrmShutd)	INTERNAL REGULATOR, V_A
<140°C	Normal operation	0	Normal operation
140°C	Normal operation	0	Normal operation
150°C	All outputs shut down (thermal overload)	1	Normal operation
160°C	All outputs shut down (thermal overload)	1	Shutdown

Summary: When the MAX14915 chip temperature rises above the thermal shutdown threshold of 150°C, the chip enters shutdown protection and all overloaded OUT switches are kept off until the chip temperature drops below +140°C. The ThrmShut bit and FAULT output are set.

Transient Immunity Testing

The MAXREFDES1165 was tested in Maxim's laboratory for common industrial transient immunity standards, and the test methodology and results are presented in this section.

Performance Criteria for Immunity Tests

The results of immunity test are typically classified into four categories as listed in **Table 3**. The end-application requirements and its ability to tolerate transient noise will determine whether the system sees the performance criteria as a failure or not.

Table 3. Performance Criteria for Immunity Test

CRITERIA	DESCRIPTION
Performance Criteria A	Normal operation with no performance degradation
Performance Criteria B	Temporary performance degradation which is self-recoverable (data loss, data error)
Performance Criteria C	Temporary performance degradation which requires intervention (device reset or power cycle)
Performance Criteria D	Loss of function which is not recoverable (device damage)

IC and Board-Level Protection

Maxim ICs are designed to survive transient immunity events using a combination of integrated functionality and external (board-level) components. All Maxim ICs are designed to support robust ESD performance and some interface devices, such as the MAX14873E RS-485 transceiver, have ±35kV ESD (HBM) specification. However, for higher energy ESD and surge pulses, such as described in IEC 61000-4-2 and IEC 61000-4-5, external transient voltage suppression (TVS) diodes are typically used to meet ESD and surge transient immunity. These diodes have extremely fast response times in order to respond to the 1ns rise time of the ESD pulse and excellent power dissipation capability to withstand ten of amps of surge current. The TVS diode clamps the incoming transients to a safe level to avoid damage to the semiconductor device.

In order to achieve high electrical fast transient (EFT) performance, some devices such as digital isolators are designed to provide a high common-mode transient immunity (CMTI) performance, which improves EFT tolerance. For more robust systems with line-to-PE surge protection, a Y-capacitor between field ground (GNDF) and protective earth (PE) can be used. Maxim's digital output devices such as the MAX14915 are protected by their internal clamping diodes and feature integrated line-to-ground and line-to-line surge protection, which only requires a TVS diode on V_{DD}. Maxim's digital input devices such as the MAX22190 achieve high Contact and Air-Gap ESD performance with a single external series resistor, which also achieves surge immunity.

A simplified schematic of the external protection devices used on the MAXREFDES1165 is shown in **Figure 13**.

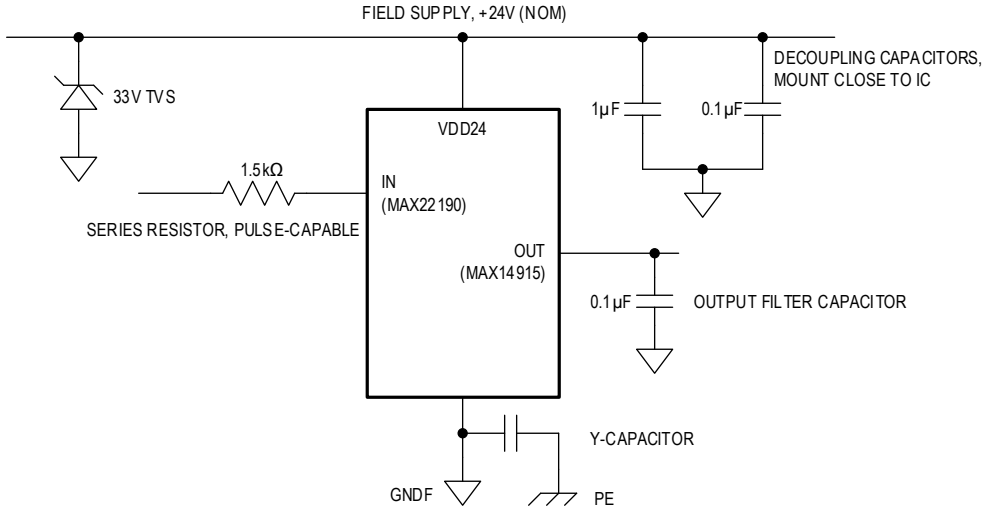

Figure 13. MAXREFDES1165 simplified schematic for transient immunity.

IEC 61000-4-2 Electrostatic Discharge

ESD results from electrical charge buildup, and different generators for this charge are found in industrial applications. This standard covers surges with a duration of tens of nanoseconds and is more stressful than other, lower energy ESD standards such as Human Body Model (HBM) or Machine Model (MM), both of which are tested as standard for all Maxim products and listed in the individual IC data sheets.

Contact Discharge method: The charged electrode of the test generator is held in contact with the EUT, and the discharge is actuated by the discharge switch within the generator.

Air-Gap Discharge method: The charged electrode of the generator is brought close to the EUT, and the discharge is actuated by a spark to the EUT.

An ESD test generator is used with a "sharp point" to make direct connection to the EUT (pin) for Contact ESD testing. A "round tip" is added to the generator for Air-Gap ESD testing.

Table 4. ESD Test Procedure

Output Voltage	Up to ±8kV (nominal) for Contact Discharge Up to ±15kV (nominal) for Air-Gap Discharge
Polarity of the output voltage	Positive and negative
Holding time	At least 5 seconds
Number of applications	Ten (10) consecutive ESD discharges for each polarity

Figure 14 shows the IEC 61000-4-4 model, and **Figure 15** shows the current waveform for IEC 61000-4-2 Contact Discharge test.

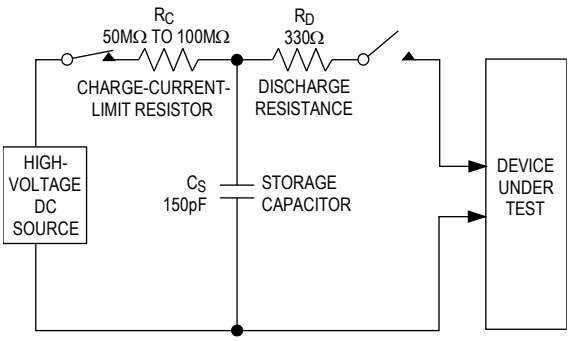

Figure 14. IEC 61000-4-2 ESD test circuit.

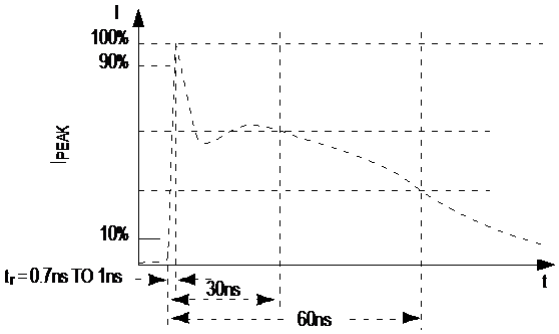

Figure 15. IEC 61000-4-2 Contact Discharge test waveforms.

IEC 61000-4-4 EFT/Burst Testing

EFTs are commonly found in industrial applications and occur from the arcing of contacts in switches and relays, as well as when large inductive loads (such as motors) are connected and disconnected.

An EFT/surge generator with an output voltage range of up to ±4kV with a 50Ω load is used to generate the voltage waveforms defined by the IEC specification. A capacitive coupling clamp provides the ability to couple the fast transients (bursts) from the EFT generator to the input, output, or power pins of the EUT without any galvanic connection to the EUT. The bench test setup is shown in **Figure 16**, and the waveform is shown in **Figure 17**.

Table 5. EFT Test Procedure

Test Voltage	Up to ±4kV
Polarity of the Output Voltage	Positive and negative
Repetition Frequency	5kHz, 100kHz
Burst Duration/Repetition Time	15ms/300ms at 5kHz 0.75ms/300ms at 100kHz
Test Duration	60 seconds

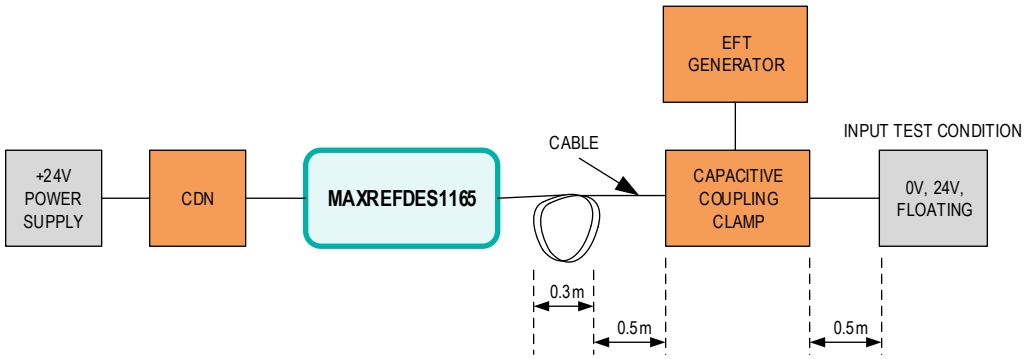

Figure 16. EFT/burst waveform test bench setup.

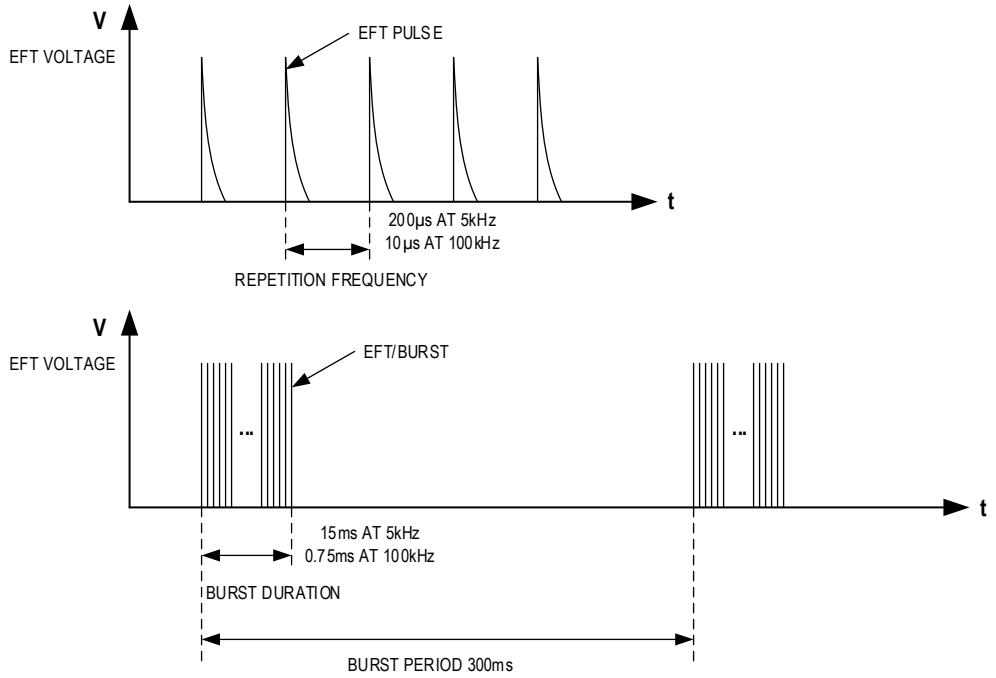

Figure 17. IEC 61000-4-4 EFT/burst waveform.

IEC 61000-4-5 Surge Testing

Severe transients or surges occur during events such as lightning strikes or switching of power systems and loads or during short-circuit fault conditions. This IEC standard specifies six classes of test levels, which depend on the end-equipment installation conditions. The class determines the protection with corresponding voltage levels. In addition, this defines the coupling mode (line-to-line or line-to-ground) and the source impedance (Zs) required. The class that most closely fits the applications using products such as Maxim's digital I/O ICs are Class 3 for asymmetrical operated circuits/lines with suggested test levels of ±2kV for line-to-line and ±1kV for line-to-ground. Refer to the IEC 61000-4-5 standard for further details.

The standard recommends a source impedance of 42Ω and, because the surge generator has an internal impedance of 2Ω, an external 40Ω resistor is used in series with the generator, as shown in the simplified schematic in **Figure 18**.

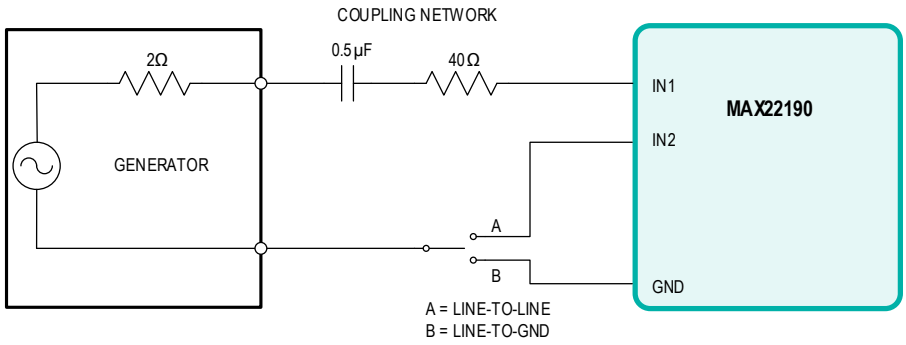

Figure 18. IEC 61000-4-5 surge test methods.

Table 6. Surge Test Procedure

Test Voltage	Up to ±2kV
Polarity of the Output Voltage	Positive and negative
Waveform Parameters	Front time: 1.2µs Time to half-value: 50µs
Signal Applied	Port-to-port

	Port-to-ground
Repetition Rate	Ten (10) surges, 10s interval for both polarities

Surge testing is performed in accordance with the IEC 61000-4-5 specification, and a typical setup is shown in **Figure 19**. The 1.2/50µs combination wave generator is used for testing the digital I/O products, and the waveform is shown in **Figure 20**. Surge transients with a total source impedance of 42Ω are performed for all 16 DIs and 16 DOs. Ten surge pulses of both positive and negative polarities are applied for each test condition. The pulses are applied with a 10s interval (0.1Hz). For the MAX22190, the input ports are tested when floating, or held low (0V) or held high (24V). For the MAX14915, the output ports are tested with the output switch on (+24V) and off (0V) with a load connected and also with output floating. After each surge test, the GUI reads the status of the EUT (through the SPI interface) to see if the surge transient caused any damage, changed any register contents, or caused a device reset.

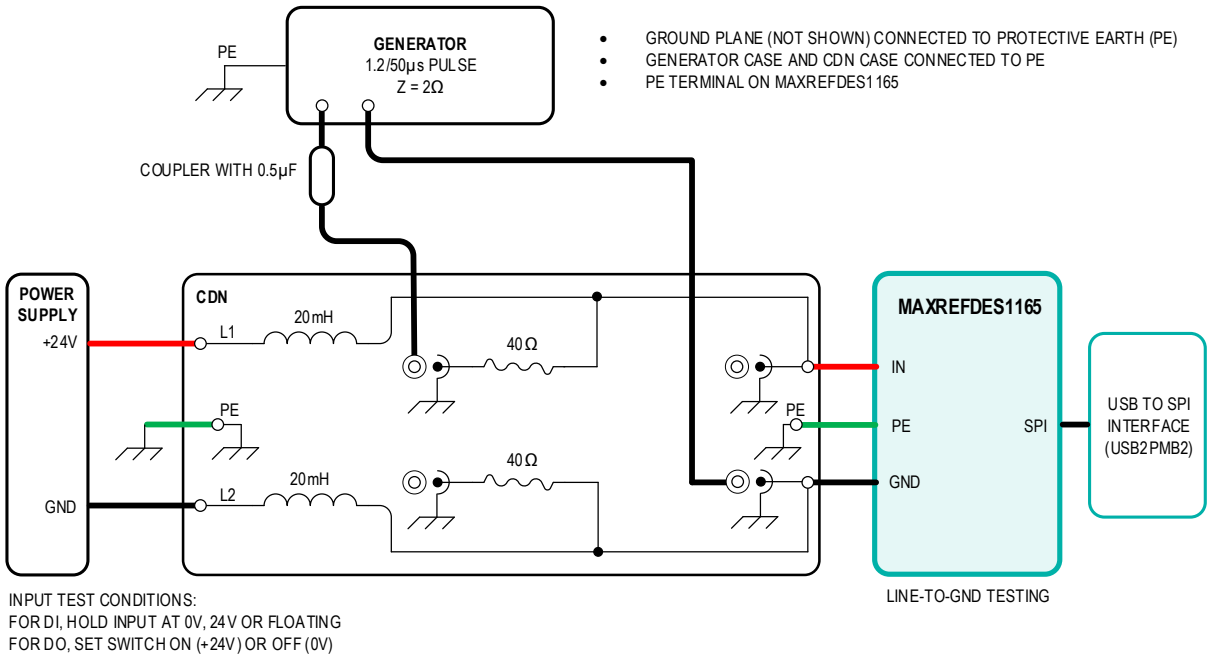

Figure 19. Surge test bench setup.

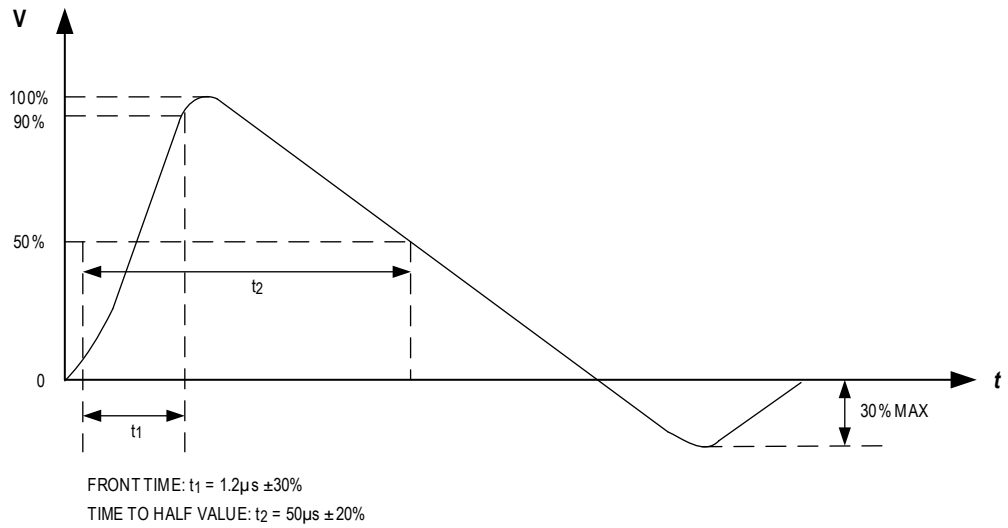

Figure 20. IEC 61000-4-5 1.2/50µs surge voltage waveform.

Transient Immunity Testing Bench Setup

The equipment used for testing the MAXREFDES1165 is listed in **Table 7**, and a picture of the testing bench setup is shown in **Figure 21**.

Table 7. Equipment Used for Transient Immunity Tests

EQUIPMENT	DESCRIPTION	TEST(S)
MAXREFDES1165	Equipment under test (EUT)	All
ESD Test Generator	Teseq® NSG 438 with Air-Gap Discharge Tip 403-826	Contact ESD and Air-Gap ESD
EFT/Surge Generator	Haefely® Technology ECOMPACT4 and Teseq NSG 3040A	EFT and Surge
Signal and Data Line Coupling Network	Teseq CDN 117	Surge
Coupler with 0.5µF Capacitor	INA 174A	Surge
Capacitive Coupling Clamp	Teseq CDN 3425	EFT

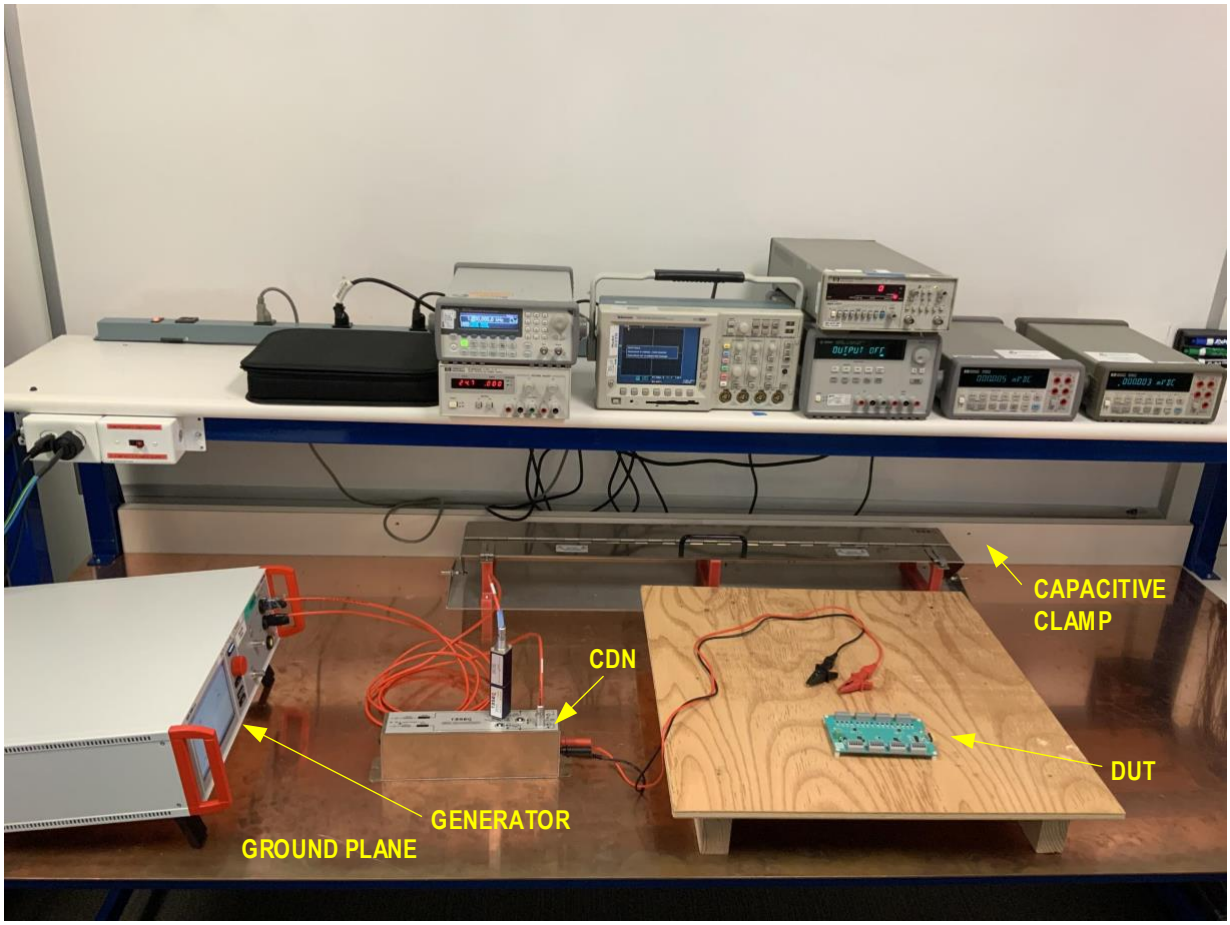

Figure 21. MAXREFDES1165 transient immunity testing bench setup.

Transient Immunity Test Results

Tables 8–10 include details of specific test conditions and results for each test. For input tests with the MAX22190, the input was either tied low (0V), tied high (+24V), or left floating. For output tests with the MAX14915, the output switch

was set to on or off with a 1kΩ load connected to ground. When the MAX14915 output was 'floating', the output switch was set to off, but with no load connected.

The MAXREFDES1165 meets performance Criteria B for all of the IEC61000-4 immunity tests.

Table 8. ESD Test Conditions and Results

DUT		MAX22190 (DIGITAL INPUT)			MAX14915 (DIGITAL OUTPUT)		
I/O		IN1 – IN16 (U1, U2)			OUT1 – OUT16 (U3, U4)		
TEST CONDITIONS		FLOATING	0V	24V	FLOATING, SWITCH OFF	1kΩ LOAD, SWITCH OFF (0V)	1kΩ LOAD, SWITCH ON (24V)
Line-to-GND	Contact	±8kV, Criteria B	±8kV, Criteria B	±8kV, Criteria B	±7kV, Criteria B	±7kV, Criteria B	±7kV, Criteria B
	Airgap	±15kV, Criteria B	±15kV, Criteria B	±15kV, Criteria B	±30kV, Criteria B	±30kV, Criteria B	±30kV, Criteria B

Table 9. EFT/Burst Test Conditions and Results

DUT		MAX22190 (DIGITAL INPUT)			MAX14915 (DIGITAL OUTPUT)		
I/O		IN1 – IN16 (U1, U2)			OUT1 – OUT16 (U3, U4)		
TEST CONDITIONS		FLOATING	0V	24V	FLOATING, SWITCH OFF	1kΩ LOAD, SWITCH OFF (0V)	1kΩ LOAD, SWITCH ON (24V)
Line-to-GND	5kHz	±4kV, Criteria B	±4kV, Criteria B	±4kV, Criteria B	±4kV, Criteria B	±4kV, Criteria B	±4kV, Criteria B
	100kHz	±4kV, Criteria B	±4kV, Criteria B	±4kV, Criteria B	±4kV, Criteria B	±4kV, Criteria B	±4kV, Criteria B

Table 10. Surge Test Conditions and Results

DUT		MAX22190 (DIGITAL INPUT)			MAX14915 (DIGITAL OUTPUT)		
I/O		IN1 – IN16 (U1, U2)			OUT1 – OUT16 (U3, U4)		
TEST CONDITIONS		FLOATING	0V	24V	FLOATING, SWITCH OFF	1kΩ LOAD, SWITCH OFF (0V)	1kΩ LOAD, SWITCH ON (24V)
Line-to-GND	±1kV	Criteria B	Criteria B	Criteria B	Criteria B	Criteria B	Criteria B
Line-to-Line	±2kV	Criteria B	N/A	N/A	Criteria B	N/A	N/A

Design Resources

Download the complete set of Design Resources including schematics, bill of materials, and PCB layout.

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