

Introduction

The MAX17681/MAX17681A is a high-voltage, high-efficiency, iso-buck DC-DC converter designed to provide isolated power up to 5W. The device operates over a wide 4.5V to 42V input and uses primary-side feedback to regulate the output voltage. The MAX17681/MAX17681A uses peak-current-mode control. Low-resistance, on-chip MOSFETs ensure high efficiency at full load while simplifying the PCB layout. The MAX17681/MAX17681A devices generate a well-regulated primary side voltage, which is then scaled by a suitable transformer turns ratio to derive isolated secondary output rails. While both the MAX17681 and MAX17681A support primary side overcurrent protection, the MAX17681A is an enhanced design that also supports robust secondary-side overcurrent protection. The MAX17681/MAX17681A is available in a compact 10-pin (3mm × 2mm) TDFN package.

Simulation models are available.

- Reduces External Components and Total Cost
 - No Optocoupler
 - Synchronous Primary Operation
 - All-Ceramic Capacitors, Compact Layout
- Reduces Number of DC-DC Regulators to Stock
 - Wide 4.5V to 42V Input
 - 0.9V to 0.96 × V_{IN} Primary Output Voltage
 - Delivers Up to 5W Output Power
- Reduces Power Dissipation
 - Peak Efficiency > 90%
 - 0.9μA (typ) Shutdown Current
- Operates Reliably in Adverse Industrial Environments
 - Peak and Sink Current-Limit Protection
 - Robust Secondary-Side Output Overcurrent Protection (MAX17681A)
 - ±1.7% Feedback Accuracy
 - Programmable EN/UVLO Threshold
 - Adjustable Soft-Start
 - Overtemperature Protection
 - -40°C to +125°C Operation

Hardware Specification

An iso-buck DC-DC converter using the MAX17681A is demonstrated for ±15V DC or ±12V DC output applications. The power supply delivers up to 100mA at ±15V or 50mA at ±12V. Table 1 provides an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	MAX
Input Voltage	V _{IN}	17V	32V
Switching Frequency	f _{SW}	200kHz	
Peak Efficiency	η	89%	
Duty Cycle	D	27.1%	60%
Output Voltage 1	V _{OUT1}	14.4V	17.3V
Output Current 1	I _{OUT1}	0A	100mA
Output Voltage 2	V _{OUT2}	-16.6V	-14.2V
Output Current 2	I _{OUT2}	0A	100mA
Output Voltage Ripple 1	ΔV _{OUT1} or ΔV _{OUT2}	220mV	
Output Power 1	P _{OUT1} , P _{OUT2}	3W	
Output Voltage 3	V _{OUT3}	11.88V	12.12V
Output Current 3	I _{OUT3}	0A	50mA
Output Voltage 4	V _{OUT4}	-12.12V	-11.88V
Output Current 4	I _{OUT4}	0A	50mA
Output Voltage Ripple 2	ΔV _{OUT3} or ΔV _{OUT4}	20mV	
Output Power 2	P _{OUT3} , P _{OUT4}	1.2W	

Designed–Built–Tested

This reference design describes the hardware shown in Figure 1. It provides a detailed systematic technical guide to design an iso-buck converter using Maxim's MAX17681A current mode controller. The power supply has been built and tested, details of which follow later in this document.

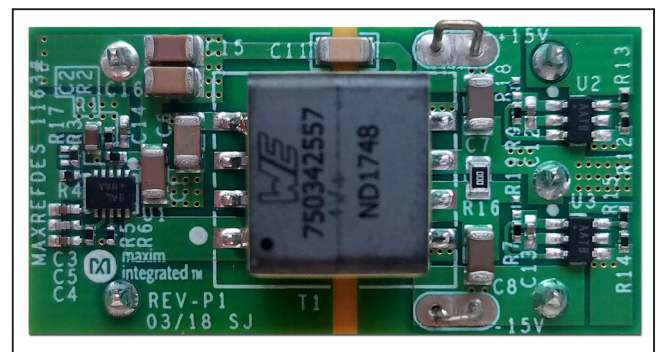


Figure 1. MAXREFDES1163 hardware.

Detailed Description of the Hardware

The MAX17651 ultra-low quiescent current, high-voltage linear regulator is ideal for use in industrial and battery-operated systems. The device operates from a 4V to 60V input voltage, delivers up to 100mA of load current, and consumes only 8 μ A of quiescent current at no load. The device consumes only 0.9 μ A current when in shut-down. Output voltage is adjustable in the 0.6V to 58V voltage range. Feedback voltage accuracy is $\pm 2\%$ over temperature.

This reference design is derived from the MAX17681AEVKITA. The three main differences between MAXREFDES1163 and the MAX17681AEVKITA are as follows:

- The board size of the MAXREFDES1163 is 20mm \times 40mm, which is approximately one-quarter the size of the MAX17681AEVKITA.
- The pin distances of the MAXREFDES1163 are consistent with Distributed-power Open Standards Alliance (DOSA) open standards for DC/DC brick power supplies.

- The reference design has two transformer options, one is from Würth Elektronik® and the other is from the transformer vendor HanRun Electronics®.

With the above three features, customers can reduce the whole solution size and cost. Customers can also mount this reference design on system boards.

Iso-Buck Converter

The iso-buck has a synchronous-buck-converter-based topology, useful for generating isolated outputs at low power levels without using an optocoupler. Figure 2 shows the basic circuit of an iso-buck converter, comprising a half-bridge transformer driver and secondary side filter.

Figure 3 shows the equivalent circuit when the high-side switch (Q_{HS}) is on. During this time, the primary current ramps up and stores energy in the transformer magnetizing inductance (L_{PRI}) and the primary capacitor (C_{PRI}). The secondary side diode is reverse-biased, and the load current is supplied by the secondary-side filter capacitor (C_{OUT}).

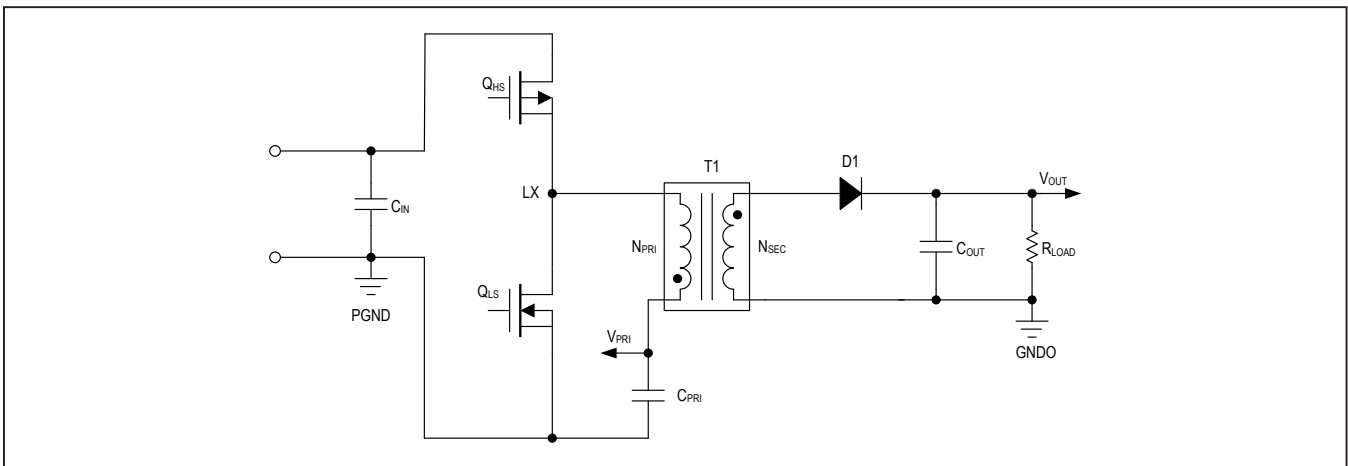


Figure 2. Iso-buck topology.

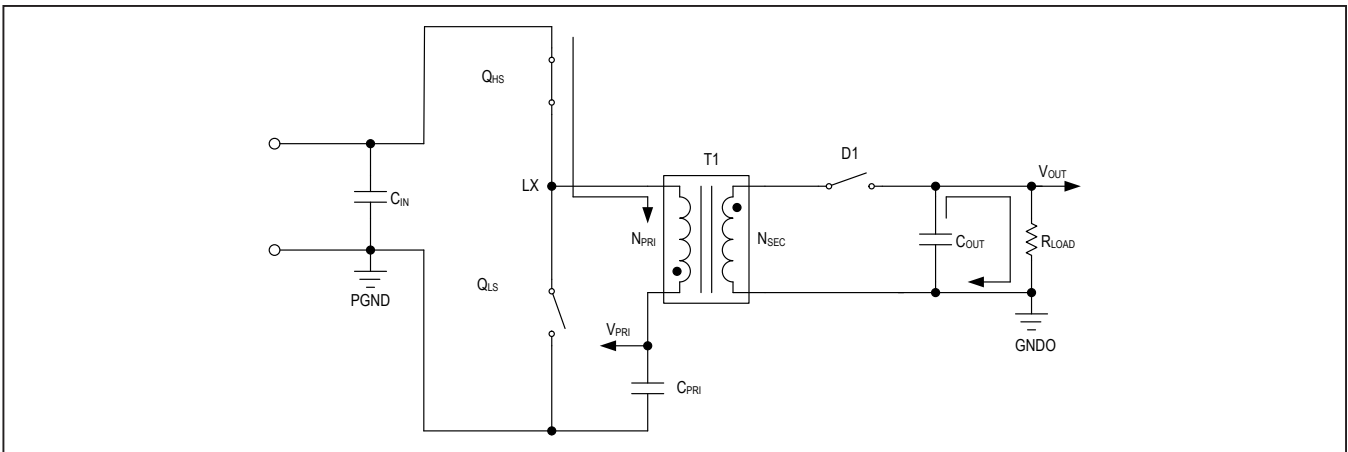


Figure 3. On-period equivalent circuit.

HanRun Electronics is a registered trademark of Hanrun Electronics Co., Ltd.

Würth Elektronik is a registered trademark and registered service mark of Würth Elektronik GmbH & Co.

Figure 4 shows the equivalent circuit when the low-side switch (Q_{LS}) is on. During this time, the secondary diode gets forward-biased. The primary current ramps down and releases stored energy in the transformer magnetizing inductance and the primary capacitor to the load.

Operating waveforms of the converter are shown in Figure 5. Neglecting diode drop V_D , transformer resistances, and leakage inductance, the output voltage V_{OUT} is proportional to the primary output voltage C_{PRI} and is regulated by the MAX17681/MAX17681A control loop.

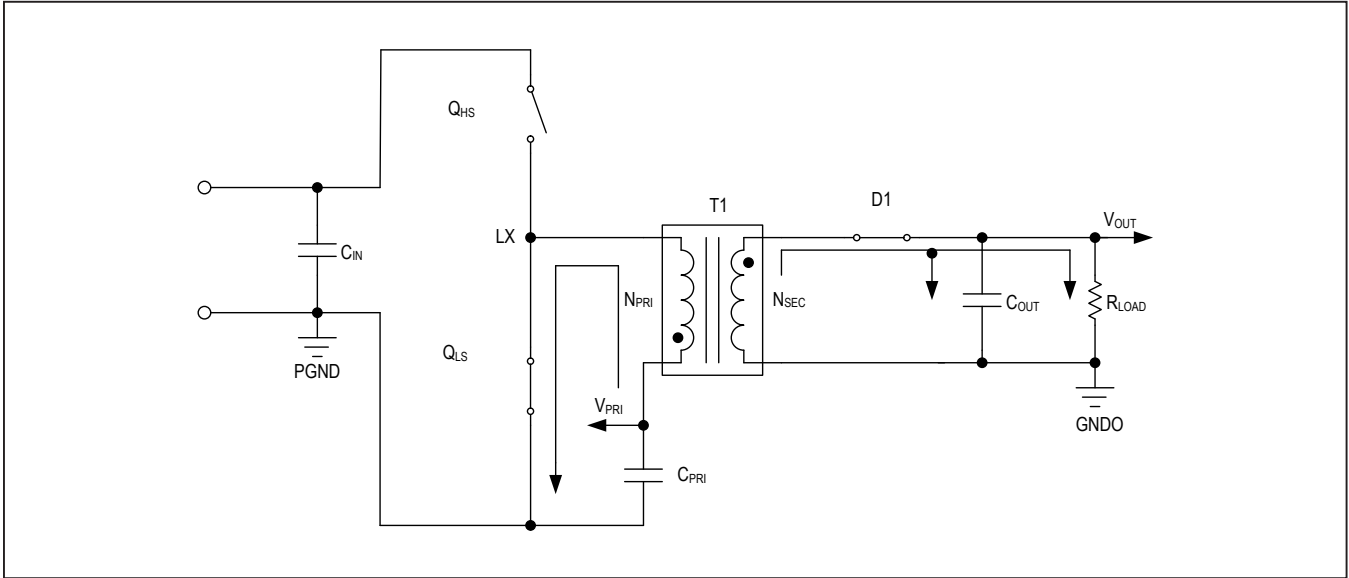


Figure 4. Off-period equivalent circuit.

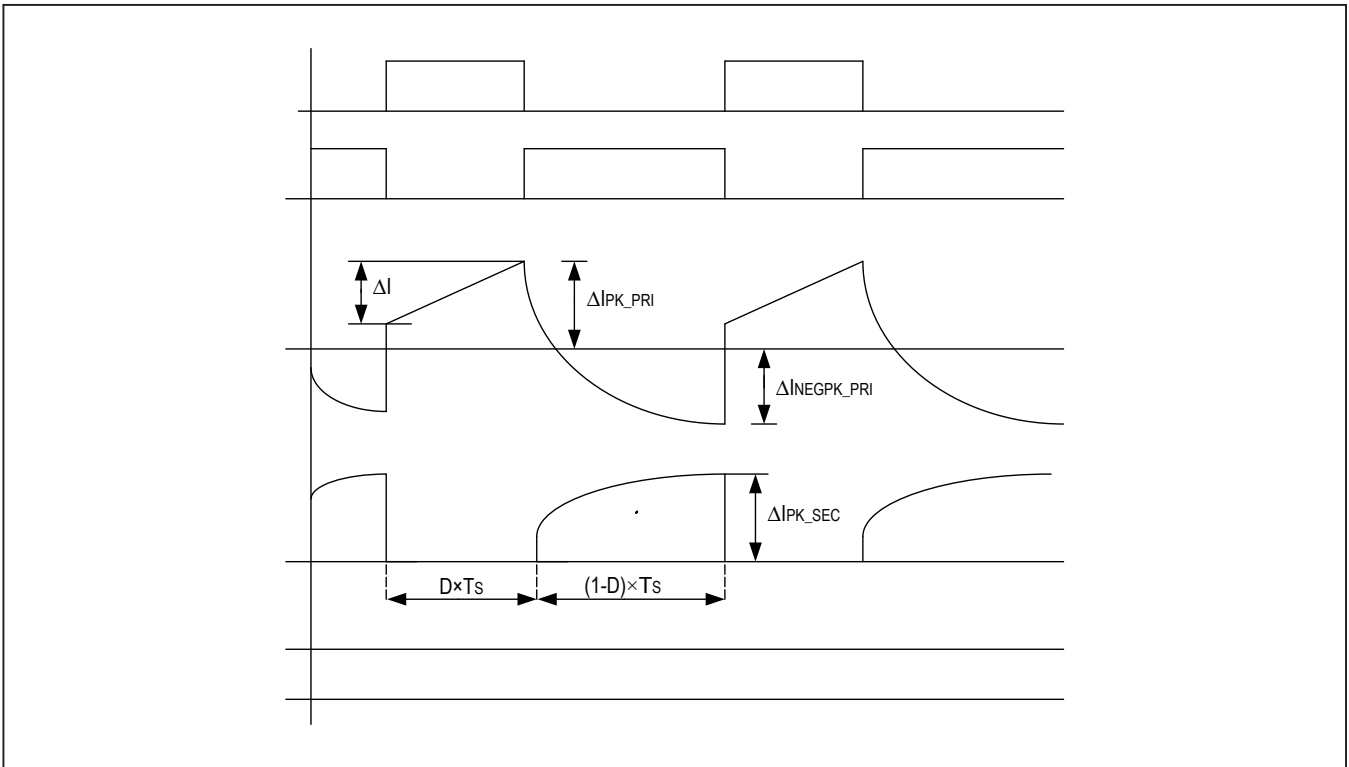


Figure 5. Iso-buck operating waveforms.

Design Procedure for the Iso-Buck Converter

Now that the principle of operation of the iso-buck is understood, a practical design example can be illustrated. The converter design process can be divided into different stages, such as power stage design and setup of the MAX17681 iso-buck peak current mode controller. This document is primarily concerned with the power stage design, and the other circuit is intended to complement the information contained in the MAX17681 data sheet for details on how to set up the protection functions of the controller. Because the $\pm 12\text{V}/50\text{mA}$ is the output of the linear regulator MAX17651, which is very easy to design, it is not illustrated in this document.

The following design parameters are used throughout:

V_{IN}	= Input Voltage
V_{INU}	= Input Under-Voltage Lockout Level
t_{SS}	= Soft Start Time
V_O	= Output Voltage
ΔI	= Primary Ripple Current
I_O	= Output Current
f_{SW}	= Switching Frequency
D_{MAX}	= Maximum Duty Cycle
K	= Secondary to Primary Turns Ratio
V_{PRI}	= Primary Voltage
I_{PK_PRI}	= Primary Peak Current
I_{PRI_RMS}	= Primary RMS Current
I_{PK_SEC}	= Secondary Peak Current
I_{PRI_RMS}	= Secondary RMS Current

The above symbols are sometimes followed by parentheses to indicate whether minimum or maximum values of the parameters are intended, for example: minimum input voltage is intended by the symbol $V_{IN(MIN)}$. Otherwise typical values are intended. In addition, through the design procedure reference is made to the schematic in another document.

Step 1: Primary Output Voltage Selection

Primary output voltage is regulated by the MAX17681/MAX17681A control loop. The primary output voltage can be calculated by using the following equation:

$$V_{PRI} = D_{MAX} \times V_{IN(MIN)}$$

where D_{MAX} is the maximum duty cycle of the converter and $V_{IN(MIN)}$ is the minimum input voltage. Maximum duty cycle should be in the range of 0.4 to 0.6 for ideal iso-buck operation. In this design we use 0.45 as the maximum duty cycle, so

$$V_{PRI} = 0.5 \times 17 = 8.5\text{V}$$

Step 2: Adjusting the Primary Output Voltage

The primary output voltage is set with a resistor-divider from the primary output to FB to GND (see Figure 6). Choose R2 in the range of 10k to 49.9k and calculate R1 using the equation:

$$R1 = R2 \times \left(\frac{V_{PRI}}{0.9} - 1 \right)$$

Choose R2 = 10.5k, so:

$$R1 = 10.5 \times \left(\frac{8.5}{0.9} - 1 \right) = 88.67\text{k}$$

Choose R1 = 90.9k, so $V_{PRI} = 8.69\text{V}$

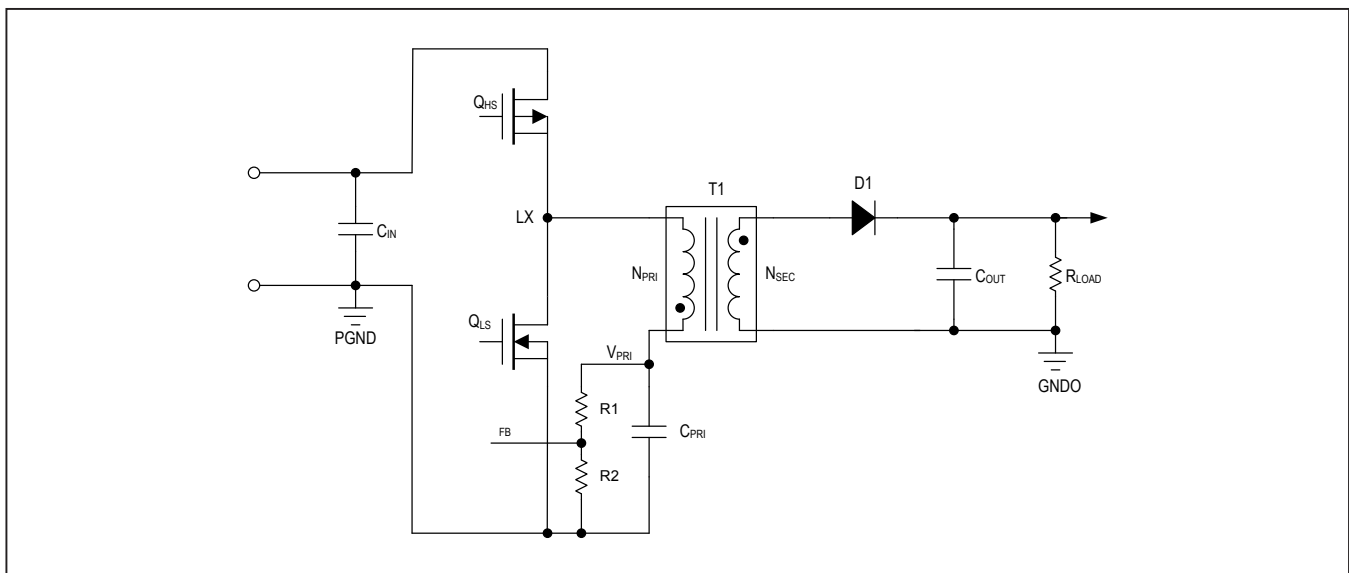


Figure 6. Adjusting the primary output voltage.

Step 3: Transformer Turns Ratio Selection

Neglecting the diode drop V_D , transformer resistances, and leakage inductance, the iso-buck output voltage V_{OUT} is proportional to the primary output voltage V_{PRI} . The turns ratio (K) is given by the following equation:

$$K = \frac{N_{SEC}}{N_{PRI}} = \frac{V_{OUT} + V_D}{V_{PRI}}$$

The turns ratio can be adjusted to match the readily available off-the-shelf transformer turns ratio by adjusting the primary output voltage. There are four output voltages in this design so four secondary coils are needed. Use K1 as the turns ratio of the +15V output voltage and the primary output voltage, and use K2 as the turns ratio of the -15V output voltage and the primary output voltage.

$$K1 = \frac{N_{SEC1}}{N_{PRI}} = \frac{V_{OUT1} + V_D}{V_{PRI}} = \frac{15 + 0.5}{8.69} = 1.78$$

$$K2 = \frac{N_{SEC2}}{N_{PRI}} = \frac{V_{OUT2} + V_D}{V_{PRI}} = \frac{15 + 0.5}{8.69} = 1.78$$

Choose $K1 = 2$ and $K2 = 2$.

Step 4: Primary Inductance Selection

The primary inductance value determines the ripple current in the transformer. The required primary inductance is given by the equation:

$$L_{PRI} = 7 \times V_{PRI} = 7 \times 8.69 = 60.83\mu\text{H}$$

where L_{PRI} is the primary inductance in μH and V_{PRI} is the primary output voltage. The primary ripple current can be calculated using the following equation:

$$\Delta I = \frac{V_{PRI} \times \left(1 - \frac{V_{PRI}}{V_{IN}}\right)}{f_{SW} \times L_{PRI}} = \frac{8.69 \times \left(1 - \frac{8.69}{17}\right)}{200 \times 10^3 \times 50 \times 10^{-6}} = 0.35\text{A}$$

where L_{PRI} is the primary inductance in H, f_{SW} is the switching frequency in Hz, V_{PRI} is the primary output voltage, V_{IN} is the input voltage.

Step 5: Winding Peak and RMS Currents Calculation

The winding peak and RMS current ratings should be specified for selecting the iso-buck transformer. Primary and secondary winding peak currents are given by the following equations:

$$I_{PK_PRI} = \sum_{i=1}^n I_{O_i} \times K_i + \frac{\Delta I}{2} = 0.1 \times 2 + 0.1 \times 2 + \frac{0.35}{2} = 0.575\text{A}$$

$$I_{PK_SEC1} = \frac{2 \times I_{O1}}{1-D} = \frac{2 \times 0.1}{1-0.5} = 0.4\text{A}$$

$$I_{PK_SEC2} = \frac{2 \times I_{O2}}{1-D} = \frac{2 \times 0.1}{1-0.5} = 0.4\text{A}$$

Where n is the total number of isolated outputs, i is the individual isolated output, I_O is the secondary load current, K is the secondary turns ratio, D is the duty cycle, and ΔI is the primary ripple current. Primary RMS current is the sum of the high-side and low-side switch RMS currents.

The high-side switch RMS current is given by the following equation:

$$I_{HS_RMS} = \sqrt{D \times \left(\left(\sum_{i=1}^n I_{O_i} \times K_i \right)^2 + \frac{\Delta I^2}{12} \right)} = \sqrt{0.5 \times \left((0.1 \times 4)^2 + \frac{0.35^2}{12} \right)} = 0.29\text{A}$$

The low-side switch RMS current is given by the following equation:

$$I_{LS_RMS} = \sqrt{1-D} \times \left\{ \left(\left(\sum_{i=1}^n I_{O_i} \times K_i \right)^2 + \frac{\Delta I^2}{12} + \frac{4 \times \left(\sum_{i=1}^n I_{O_i} \times K_i \right)^2}{3 \times (1-D)} \right) \times \left(\frac{3D-1}{2 \times (1-D)} + \frac{\Delta I}{4 \times \left(\sum_{i=1}^n I_{O_i} \times K_i \right)} \right) \right\}$$

$$I_{LS_RMS} = \sqrt{1-0.5} \times \left\{ \left((0.1 \times 4)^2 + \frac{0.35^2}{12} + \frac{4 \times (0.1 \times 4)^2}{3 \times (1-0.5)} \right) \times \left(\frac{1.5-1}{2 \times (1-0.5)} + \frac{0.35}{4 \times (0.1 \times 4)} \right) \right\} = 0.46\text{A}$$

The primary winding RMS current is given by the following equation:

$$I_{PRI_RMS} = \sqrt{I_{HS_RMS}^2 + I_{LS_RMS}^2} = \sqrt{0.29^2 + 0.46^2} = 0.55A$$

The secondary winding RMS current is given by the following equation:

$$I_{SEC_RMS} = 2 \times I_O \times \sqrt{\frac{1}{3 \times (1-D)}} = 2 \times 0.1 \times \sqrt{\frac{1}{3 \times 0.5}} = 0.163A$$

Step 6: Leakage Inductance

Transformer leakage inductance (L_{LEAK}) plays a key role in determining the output voltage regulation. For better output voltage regulation, leakage inductance should be reduced to less than 1% of the primary inductance value. Higher leakage inductance also limits the amount of power delivered to the output.

Step 7: Primary Output Capacitor Selection

X7R ceramic output capacitors are preferred, due to their stability over temperature in industrial applications. The minimum required output capacitance is given by the following equation:

$$C_{PRI} = \frac{\left(\sum_{i=1}^n I_{O_i} \times K_i\right) \times D}{f_{SW} \times 0.01 \times V_{PRI}} = \frac{(0.1 \times 4) \times 0.5}{200 \times 10^3 \times 0.01 \times 8.69} = 11.5\mu F$$

Step 8: Secondary Output Capacitor Selection

A secondary side capacitor supplies load current when the high-side switch is on. The required output capacitance to support 1% steady state ripple is given by the following equation:

$$C_{OUT1} = \frac{I_{O1} \times D}{f_{SW} \times 0.01 \times V_{OUT1}} = \frac{0.1 \times 0.5}{200 \times 10^3 \times 0.01 \times 15} = 1.67\mu F$$

$$C_{OUT2} = \frac{I_{O2} \times D}{f_{SW} \times 0.01 \times V_{OUT2}} = \frac{0.1 \times 0.5}{200 \times 10^3 \times 0.01 \times 15} = 1.67\mu F$$

Dielectric materials used in ceramic capacitors exhibit capacitance loss due to DC bias levels and should be appropriately derated to ensure the required output capacitance is obtained in the application.

Step 9: Input Capacitor Selection

Ceramic input capacitors are recommended for the IC. The input capacitor reduces peak current drawn from the power source and reduces noise and voltage ripple on the input caused by the switching circuitry. In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the input ceramic capacitor to provide necessary damping for potential oscillations caused by the longer input power path and input ceramic capacitor. The required input capacitance can be calculated using the following equation:

$$C_{IN} = \frac{\left(\sum_{i=1}^n I_{O_i} \times K_i\right) \times D \times (1-D)}{f_{SW} \times \Delta V_{IN}} = \frac{0.1 \times 4 \times 0.5 \times 0.5}{200 \times 10^3 \times 0.02 \times 17} = 1.47\mu F$$

ΔV_{IN} is the input voltage ripple, normally 2% of the minimum input voltage, D_{MAX} is the maximum duty cycle, and f_{SW} is the switching frequency of operation.

Step 10: Secondary Diode Selection

A secondary rectifier diode should be rated to carry peak secondary current and to withstand reverse voltage when the high-side switch is on. A Schottky diode with less forward-voltage drop should be selected for better output voltage regulation. The peak current rating of the diode is given by the following equation:

$$I_{PK_DIODE} = \frac{2 \times I_O}{1-D} = \frac{2 \times 0.1}{0.5} = 0.4A$$

The peak reverse voltage rating of the diode is given by the following equations:

$$V_{DIODE1} = (V_{IN_MAX} - V_{PRI}) \times K1 + V_{O1} = (32 - 8.69) \times 2 + 15 = 62V$$

$$V_{DIODE2} = (V_{IN_MAX} - V_{PRI}) \times K2 + V_{O2} = (32 - 8.69) \times 2 + 15 = 62V$$

Step 11: Soft-Start Capacitor Selection

The MAX17681/MAX17681A implements an adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to GND programs the soft-start period. The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$C_{SS} = 5.55 \times t_{SS}$$

where t_{SS} is in milliseconds and C_{SS} is in nanofarads.

Step 12: Input Under-Voltage Lockout Level Setting

The device offers an adjustable input under-voltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from V_{IN} to GND (see Figure 7). Connect the center node of the divider to EN/UVLO. Choose R1 to be 3.3M Ω max and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.218}{V_{INU}}$$

where V_{INU} is the voltage at which the device is required to turn on. Choose $R1 = 3.01\text{M}\Omega$, $V_{INU} = 14\text{V}$, so $R2 = 261\text{k}\Omega$.

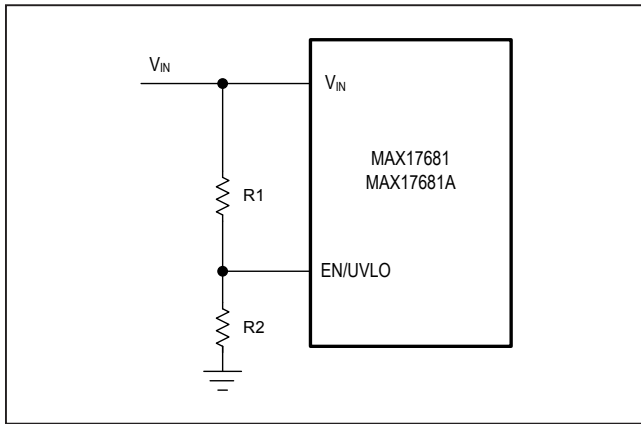


Figure 7. Adjusting EN/UVLO network.

Design Resources

Download the complete set of [Design Resources](#) including the schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/18	Initial release	—

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