

Introduction

The MAXREFDES1131 provides the internal core voltage (V_{CCINT}) for Xilinx Ultrascale+ FPGAs. This reference design targets FPGAs with a -2L speed grade that require 0.72V for V_{CCINT} from a 12V intermediary bus. The converter supports a maximum load of 12A at a 400kHz switching frequency. The MAXREFDES1131 is centered around the MAX20730 step-down regulator, which is configured for standalone operation. However, the PMBus™ interface allows for monitoring and control of various converter parameters. All circuitry for the PMBus interface is provided and the MAXPOWERTOOL002# can be used to communicate with the MAXREFDES1131.

The MAXREFDES1131 uses the MAX20730 synchronous step-down regulator. The internal MOSFETs and control loop compensation allow for a compact design with minimal external resources. Additionally, the differential sense lines allow for accurate sensing of the CPU core voltage when located remotely from the MAX20730 IC. The loop gain is selectable to allow design flexibility between stability and output capacitance. A programmable soft-start limits inrush currents during startup. The MAX20730 also offers protections such as input UVLO, output overvoltage/undervoltage alerts, output overvoltage protection, over-temperature, and current limiting. Moreover, the PMBus interface allows additional parameters to be monitored such as input voltage, output voltage, output current, and temperature. For a full list of PMBus commands, see [Application Note 6042](#).

Other features include the following:

- PMBus Interface
- Soft-Start
- Protections
 - Output Undervoltage/Overvoltage Alert
 - Current Limit and Short-Circuit Protection
 - Input UVLO at 3.9V
 - Overtemperature Protection

Hardware Specification

A synchronous buck converter design using the MAX20730 is demonstrated for a 0.72V/12A output. [Table 1](#) provides an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX
Input Voltage	V_{IN}	—	11.4V	12V	12.6V
Output Voltage	V_{OUT}	—	0.698V	0.72V	0.742V
Load	I_{OUT}	—	—	—	12A
Frequency	f_{SW}	—	—	400kHz	—
Peak Efficiency	η	—	—	84%	—
Output Voltage	V_{OUT}	—	0.698V	0.72V	0.742V
Overshoot	V_{OS}	$I_{STEP} = 6A$	—	—	36mV
Undershoot	V_{US}	$I_{STEP} = 6A$	—	—	36mV
Output Ripple	V_{RIPPLE}	—	—	—	14.4mV

Designed–Built–Tested

The power supply has been built and tested. This document describes the design of the hardware shown in [Figure 1](#).

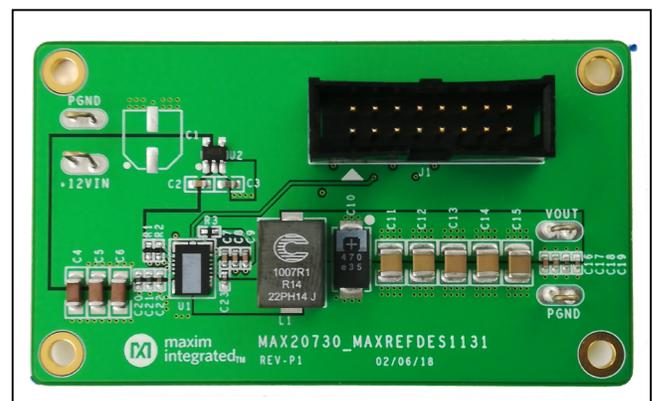


Figure 1. MAXREFDES1131 hardware.

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Synchronous Buck

In recent low-voltage, high-current power converters, the synchronous buck converters are more efficient than conventional buck converters because the synchronous buck converters use a low-side MOSFET rather than a conventional catch diode. As a result, the power dissipated in the low-side MOSFET is minimized. The low-side MOSFET is always driven opposite to the high-side MOSFET. In other words, whenever one of these switches is on, the other is off. In steady-state conditions, the complementary switching of the high-side and low-side MOSFETs regulates the output to its set value.

Figure 2 illustrates the basic operation of a synchronous buck converter. The switching period begins with S1 turning on while S2 is off, which creates a conduction path from V_{IN} to the load. While S1 is on, the magnetic field within the inductor charges up. S1 is on for as long as the control algorithm dictates. When S1 has been on for the time commanded by the controller, S1 turns off in a break-before-make scheme that ensures S1 and S2 are never on at the same time. While both S1 and S2 are off, current flows through the body diode in the low-side switch.

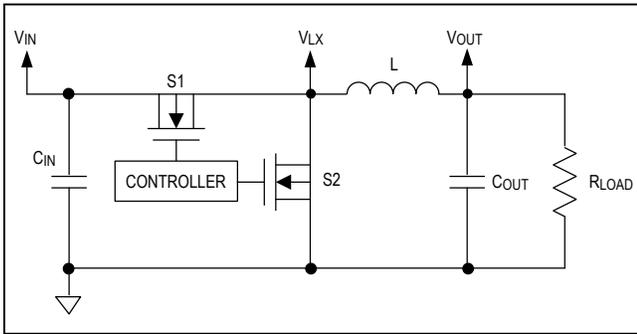


Figure 2. Synchronous buck converter topology.

This is because the stored energy in the inductor must be discharged, and the low-side MOSFETs body diode acts as a free-wheeling diode. The period where both S1 and S2 are off is known as dead time. After the dead time, S2 is turned on, and the inductor discharges through the on-resistance of S2 for the remainder of the switching period. Discharging the inductor through the low on-resistance of the low-side MOSFET significantly reduces conduction losses when compared to a conventional buck converter that uses a diode in place of the low-side MOSFET. The control algorithm uses these three states to regulate the output based on feedback signals from the converter.

PWM Valley Current-Mode Control

The MAX20730 is a synchronous buck regulator that uses a pulse-width-modulation (PWM), valley current-mode control scheme. PWM control allows for regulation of the output voltage by modulating the high-side switch on-time (i.e., S1 in Figure 2), while maintaining a constant switching frequency. The control algorithm uses the output voltage as feedback to determine the high-side switch on-time. Typical waveforms for the output voltage (V_{OUT}), inductor current (I_L), and switch-node (V_X) are shown in Figure 3.

Moreover, the MAX20730 also monitors the inductor current through the low-side switch. While the low-side switch is on, the V_X node is connected to ground, and the inductor is in a discharging state. The inductor reaches its minimum current at the end of the low-side switch on-time, which is known as the valley of the inductor current. The valley current-mode control limits the valley current of the inductor based on the device's overcurrent protection (OCP) setting and limits the amount of energy that is delivered to the load, which provides an inherent form of output current limiting. For more details on valley current protection, see [Application Note 6498](#).

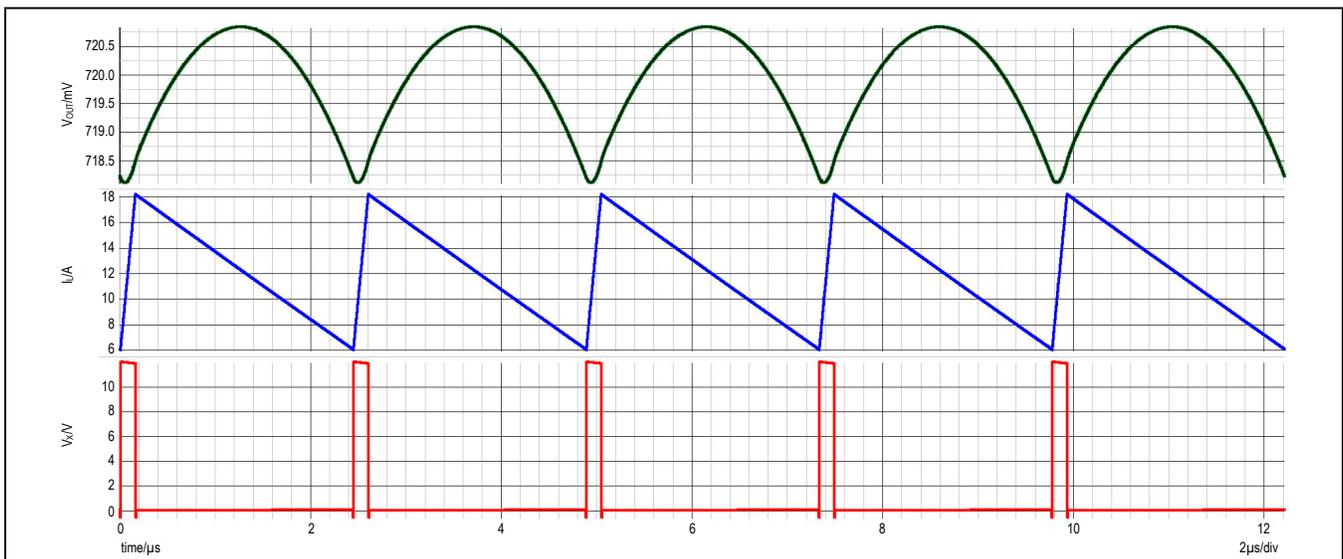


Figure 3. Synchronous buck waveforms showing output voltage (V_{OUT}), inductor current (I_L), and the switch-node (V_X).

Design Procedure for the MAXREFDES1131

The design procedure provides a step-by-step process for power supply designers to select components. The component designators refer to the MAXREFDES1131 schematic. The MAX20730 uses V_{DDH} and V_{IN} interchangeably to reference the input voltage. This document uses V_{IN} to describe the input voltage, and the reader should acknowledge that $V_{IN} = V_{DDH}$, per the MAX20730 data sheet. All other terms and variables are from the MAX20730 data sheet.

Step 1: Boot Voltage, Soft-Start, and PMBus Slave Address

The boot voltage, soft-start, and PMBus slave address are programmed through the PGMA pin.

The boot voltage is programmed using a capacitor from PGMA to GND, as shown in the PGMA Pin C_SELA Capacitor Values table in the MAX20730 data sheet. The output voltage cannot be less than the boot voltage, so we must select the boot voltage to be less than the desired output voltage (i.e., $V_{OUT} = 0.72V$). The capacitor on PGMA is left open to provide a 0.6484V boot voltage.

$$C27 = \text{Open}$$

The soft-start time and PMBus slave address are programmed through a resistor from PGMA to GND. It is expected that the MAXREFDES1131 requires a high output capacitance due to the low switching frequency and required low output voltage ripple. During startup, the output capacitors are discharged and appear as a short to the input. Large inrush currents are drawn from the supply during startup due to the bulk output capacitance. To minimize current draw during startup, we select the longest startup time of 3ms. The PMBus slave address is not a concern for this design, so a 9.09k Ω resistor (R8) is used to set the 3ms soft-start and to provide a slave address of 0x54. See the PGMA Pin R_SELA Values table in the MAX20730 data sheet for more information.

$$R8 = 9.09\Omega \pm 1\%$$

Step 2: Output Voltage

The output voltage is programmed using a resistor-divider from V_{OUT} to PGND. The MAX20730 uses differential sense lines to measure the feedback voltage. The differential sense lines accurately measure the output voltage at the point of load to minimize the effect of PCB parasitic impedances on the feedback signal. The MAXREFDES1131 uses external feedback resistors to set the output voltage, so the differential sense lines must be connected to the low-side resistor in the resistor-divider network. However, the differential sense lines must still be routed to the point of load. Use the layout for this design as reference when designing the PCB layout.

The voltage across the low-side resistor is regulated to V_{BOOT} upon startup but can be adjusted using the internal

DAC. Per the MAX20730 data sheet recommendations, where $V_{REF} = V_{BOOT} = 0.6484V$ upon startup and R_{PAR} is approximately 1k Ω , calculate the feedback resistor-divider values as follows:

$$R1 = \frac{V_{OUT} \times R_{PAR}}{V_{REF}} = \frac{0.72V \times 1k\Omega}{0.6484V} \approx 1.11k\Omega$$
$$R2 = \frac{R1 \times R_{PAR}}{R1 - R_{PAR}} = \frac{1.11k\Omega \times 1k\Omega}{1.11k\Omega - 1k\Omega} \approx 10.09k\Omega$$

The feedback resistors must have at least 1% tolerance, so resistors are chosen based on available values from the standard E96 series of resistors. For this design, we select $R1 = 1.27k\Omega$ and $R2 = 11.5k\Omega$ because this combination of standard E96 resistors yields the lowest error in output voltage.

Step 3: Switching Frequency

The switching frequency is hardware-selectable or overridden through the PMBus. This design does not require any PMBus programming, so the switching frequency is set by placing a resistor from PGMB to GND. The switching frequency is chosen for high efficiency, so we select the lowest possible switching frequency of 400kHz. We must also ensure the minimum on-time is not violated based on the required duty cycle and set switching frequency. The absolute minimum on-time of the MAX20730 converter is 50ns. A 400kHz switching frequency with 12V input and 0.72V output results in 150ns of on-time, as shown by the following equation:

$$t_{H_ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} = \frac{0.72V}{12V \times 400kHz} = 150ns$$

The operating on-time is much greater than the 50ns minimum, so there is no concern for a minimum on-time violation. The 400kHz switching frequency is set by leaving the capacitor open on the PGMB pin. See the MAX20730 data sheet for the PGMB Pin C_SELB Capacitor Values table.

$$C26 = \text{Open}$$

Step 4: Average Input Current

The average input current of the converter must be less than 6A. The following equation is used to calculate the average input current and ensure it does not violate the 6A limit:

$$I_{VIN(MAX)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} = \frac{0.72V \times 12A}{12V \times 0.87} \approx 0.83A$$

For a 400kHz switching frequency, see the MAX20730 data sheet for the typical system efficiency. For $V_{IN} = 12V$, $V_{OUT} = 0.72V$, and 12A max output current, the efficiency is around 87%. This gives an approximate figure for the maximum average input current and ensures it is less than the 6A limit.

Step 5: Inductor and Valley OCP Limit

The inductor is chosen based on the inductor current ripple. The ratio between the peak-to-peak and the average inductor current is known as the inductor current ratio (i.e., LIR). The recommended LIR is between 25% to 50% of the full rated load for the MAX20730 (i.e., $I_{OUT(MAX)} = 25A$). A higher LIR results in less output capacitance and greater efficiency, but also a slow transient response and a physically larger inductor. In contrast, a lower LIR has better transient performance and a smaller inductor, but requires greater output capacitance to maintain a low ripple and generally results in lower efficiency. To obtain a fast transient response, the LIR is selected to be 50% of the full rated load.

$$L1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times LIR \times I_{OUT(MAX)} \times f_{SW}} = \frac{0.72V \times (12V - 0.72V)}{12V \times 0.5 \times 25A \times 400kHz} \approx 135nH$$

The peak current flowing through the inductor must also be calculated to ensure the inductor core does not saturate. To determine the peak inductor current, we first need to determine the valley OCP limit setting. The valley OCP limit is chosen based on the inductor current ripple and the desired output current limit. Calculate the ripple current based on the high-side switch on-time (t_{H_ON}) as follows:

$$I_{OUTRIPPLE} = \frac{t_{H_ON} \times (V_{IN} - V_{OUT})}{L1} = \frac{150ns \times (12V - 0.72V)}{135nH} \approx 12.5A$$

$$I_{VALLEY} = I_{OUT} - \frac{I_{OUTRIPPLE}}{2} = 12A - \frac{12.5A}{2} \approx 5.75A$$

We must select a valley OCP limit above the minimum calculated (5.75A) to ensure that the OCP limit does not trip at full load. Choose the OCP setting 0, which provides a typical valley threshold of 13A. Moreover, use a 1.8mΩ transimpedance gain, which allows a compromise between required output capacitance and loop stability. For more information on R_{GAIN} selection, see the Control-Loop Stability section in the MAX20730 data sheet.

Using the known positive valley current limit (i.e., I_{OCP}) and inductor current ripple, calculate the absolute peak inductor current. The valley OCP limit has some tolerance, so the maximum positive valley current for the OCP setting 0 is used in the calculation.

$$I_{PEAK} = I_{VALLEY(MAX)} + I_{OUTRIPPLE} = 16.7A + 12.5A \approx 29.2A$$

The chosen inductor is found in the Recommended Inductors table in the MAX20730 data sheet. The FP1007 family of inductors from Eaton/Cooper provide a small

size for the required inductance. The FP1007R1-R14-R is chosen for the 140nH inductance and 72A saturation current, which is well above the expected peak current. Additionally, the FP1007R1-R14-R provides the lowest DCR and height from the list of recommended inductors shown in Table 9 of the MAX20730 data sheet. This ultimately results in a higher efficiency by using a smaller inductor.

Step 6: Output Capacitance

The output capacitors are chosen based on the desired peak-to-peak voltage ripple on the output. The peak-to-peak ripple is chosen to be 2% of the output voltage for a peak-to-peak ripple of 14.4mV. The output capacitors' cumulative capacitance, ESR, and ESL contribute to the output voltage ripple. To simplify the design, the ESL component is assumed to be minimal since the switching frequency is relatively low. The output capacitance and ESR are each assumed to contribute to 50% to the ripple voltage. These voltage ripples are out of phase, but combining them provides a conservative estimate of the output voltage ripple. For the selected inductance, the inductor current ripple is recalculated to determine the output capacitance.

$$I_{OUTRIPPLE} = \frac{t_{H_ON} \times (V_{IN} - V_{OUT})}{L1} = \frac{150ns \times (12V - 0.72V)}{140nH} \approx 12.09A$$

$$ESR = 50\% \times \frac{V_{P-P}}{I_{OUTRIPPLE}} = 50\% \times \frac{14.4mV}{12.09A} \approx 0.6m\Omega$$

$$C_{OUT(MIN)} = \frac{I_{OUTRIPPLE}}{8 \times f_{SW} \times 50\% \times V_{P-P}} = \frac{12.09A}{8 \times 400kHz \times 50\% \times 14.4mV} \approx 525\mu F$$

Another aspect of output capacitor selection is the overshoot and undershoot that occurs during a transient loading event. If the slew rate of the load current greatly exceeds the slew rate of the inductor, the output capacitors must deliver charge during a loading event or absorb charge during an unloading event. This causes the output voltage to momentarily sag during loading or soar during an unloading event. The design must ensure there is no more than 5% overshoot/undershoot for a quick transient load that exceeds the slew rate of the inductor based on a 6A step load. Determine the minimum capacitance for both loading and unloading events by using the following equations:

Output Voltage Sag:

$$C_{OUT(MIN)} = \frac{L1 \times \left(I_{STEP} + \frac{I_{OUTRIPPLE}}{2} \right)^2}{2 \times V_{SAG} \times (V_{IN} - V_{OUT})} = \frac{140nH \times \left(6A + \frac{12.09A}{2} \right)^2}{2 \times 36mV \times (12V - 0.72V)} \approx 25\mu F$$

Output Voltage Soar:

$$C_{OUT(MIN)} = \frac{L1 \times \left(I_{STEP} + \frac{I_{OUTRIPPLE}}{2} \right)^2}{2 \times V_{SAG} \times V_{OUT}} + \frac{I_{STEP} \times t_{H_ON}}{V_{SOAR}} =$$

$$\frac{140nH \times \left(6A + \frac{12.09A}{2} \right)^2}{2 \times 36mV \times 0.72V} + \frac{6A \times 150ns}{36mV} \approx 416\mu F$$

Lastly, we must consider the effects of the control loop response time. The control loop takes time to respond to changes in the output voltage. This response time results in some error in the output voltage during loading and unloading events. The magnitude of the error voltage is dependent on both the magnitude of the step load and the loop gain. The effective loop gain is calculated below based on the R_{GAIN} setting and feedback divider ratio.

$$K_{DIV} = \frac{R2}{R1 + R2} = \frac{11.5k\Omega}{1.27k\Omega + 11.5k\Omega} \approx 0.901$$

$$R_{GAIN_EFF} = \frac{R_{GAIN}}{K_{DIV}} = \frac{1.8m\Omega}{0.901} \approx 2m\Omega$$

Using the effective loop gain, we then calculate the error produced based on a 6A step from 50% to 100% load. The error produced is 20mV, which is below the 5% overshoot/undershoot specification.

$$V_{OUT_ERROR} = I_{STEP} \times R_{GAIN_EFF} = 6A \times 2m\Omega = 12mV$$

With a cumulative capacitance greater than 416 μ F and a total ESR less than 0.6m Ω , the desired output voltage ripple and overshoot/undershoot can be achieved. To achieve the 416 μ F output capacitance and low ESR, multiple capacitors are placed in parallel. A 470 μ F/2.5V conductive polymer tantalum capacitor is used for the bulk capacitance. Ten 100 μ F/6.3V ceramic capacitors are additionally placed in parallel to supply the remaining capacitance and reduce the overall ESR. Furthermore, four 10 μ F/6.3V, two 1 μ F/25V, and two 0.1 μ F/16V ceramic capacitors in an 0402 size are placed in parallel to maintain low ESL. The combined capacitance is approximately 1512 μ F, and the effective ESR is approximately 0.23m Ω .

Step 7: Input Capacitance

The input capacitor is chosen based on the desired input voltage ripple. The input voltage ripple is typically between 2% to 3% of the input voltage. However, this design has a 1% ripple for a total output voltage ripple of 120mV. Calculate the input capacitance as shown in the following equation.

$$C_{IN} = \frac{I_{MAX} \times V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times V_{IN}^2 \times V_{IN-PP}} =$$

$$\frac{12A \times 0.72V \times (12V - 0.72V)}{400kHz \times 12V^2 \times 0.12V} \approx 14\mu F$$

The input capacitors provide current to the buck converter during switching transitions. Calculate the expected RMS current through the input capacitors to determine the RMS current rating the capacitors need to support by using the following equation:

$$I_{CIN_RMS} = \frac{I_{LOAD} \times \sqrt{V_{OUT} \times (V_{DDH} - V_{OUT})}}{V_{DDH}} =$$

$$\frac{12A \times \sqrt{0.72V \times (12V - 0.72V)}}{12V} \approx 2.85A$$

To achieve the required input capacitance and RMS current rating, multiple ceramic capacitors are placed in parallel. The selected bulk input capacitor is the TDK® C3216X5R1E476M160AC. The nominal capacitance for this capacitor is 47 μ F. However, with a 12V DC bias, the input capacitor diminishes in capacitance by approximately 87% (see the C3216X5R1E476M characteristic data sheet as reference). In addition, the capacitor has a \pm 20% tolerance. With both capacitor DC bias and tolerance derating in mind, the minimum expected capacitance is approximately 4.89 μ F (i.e., $C_{IN} = 47\mu F \times 13\% \times 80\% = 4.89\mu F$). A total of five C3216X5R1E476M capacitors are used on the input. Assuming each capacitor shares the RMS current equally, the RMS current per capacitor is 0.95A. Per the C3216X5R1E476M data sheet, this raises the capacitor temperature about 2°C, so heating in the components is minimal.

In addition, one 0.1 μ F and two 1 μ F capacitors are placed in parallel with the bulk capacitance to support any high-frequency currents. These capacitors are placed closest to the IC pins to minimize the parasitic impedance between the capacitors and IC.

The position for a 120 μ F aluminum electrolytic capacitor is added to the schematic in case long wires are used during testing. Long wires add inductance between a sourcing power supply and the MAXREFDES1131, which may show more ripple on the input voltage than expected in a practical application. The bulk capacitor acts as a low-impedance path for the high-frequency ripple and ensures the input voltage ripple does not affect any test measurements.

Step 8: BST Capacitor

The BST capacitor supplies charge to the high-side MOSFET gate during switching. The high-side switch is internal, so the gate driver requirements are fixed. Use the 0.22 μ F ceramic capacitor recommended by the data sheet. The maximum voltage across the BST capacitor is the same as the input voltage, so a 16V-rated capacitor is chosen based on the 12V input requirement.

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Step 9: V_{CC}, STAT, and OE

Capacitors are required at the V_{CC} pin to stabilize the internal LDO. These capacitors are placed as close as possible to the device. Three 10µF X5R ceramic capacitors are recommended for the V_{CC} pin.

The STAT pin is an open-drain alert that requires a pullup resistor to the V_{CC} rail. The recommended value for the pullup resistor is 20kΩ.

The OE pin enables the output when raised above the rising threshold voltage. The rising threshold voltage is precise to allow the sequencing of multiple regulators. However, this pin is pulled to V_{CC} through a 20kΩ resistor to allow the output voltage to start up when the input voltage is applied.

Step 10: SDA, SCL, and SMALERT

The SDA, SCL, and SMALERT are open-drain pins that require pullup resistors for PMBus communication. The PMBus interface is designed to be compatible with the MAXPOWERTOOL002#, which uses 3.3V logic. The 3.3V rail is provided by the MAX1615 high-voltage LDO from the 12V input. The SDA, SCL and SMALERT pins are tied to the 3.3V rail using 10kΩ resistors.

MAXPOWERTOOL002# GUI Description

The MAXREFDES1131 provides hardware connections to the PMBus interface of the MAX20730 using the standard MAXPOWERTOOL002# connectors. The MAXPOWERTOOL002# GUI is used to monitor and control the MAX20730 buck converter. Figure 4 shows the MAXPOWERTOOL002# GUI when connected to the MAXREFDES1131. For more information on using the MAXPOWERTOOL002# GUI, see the [MAXPOWERTOOL002# Quick Start Guide](#). For a full list of allowed PMBus commands, see [Application Note 6042](#).

The MAX20730 device only reports the differential voltage measured across the V_{SENSE+} and V_{SENSE-} pins. When feedback resistors are used to program the output voltage, the voltage measured on these pins is a scaled down version of the output. To obtain the correct output voltage reading, the resistor-divider scaling factor must be set in the PMBus Command tab of the GUI. Figure 5 demonstrates where the resistor divider ratio is set. The scaling factor is the same as the previously calculated K_{DIV} value.

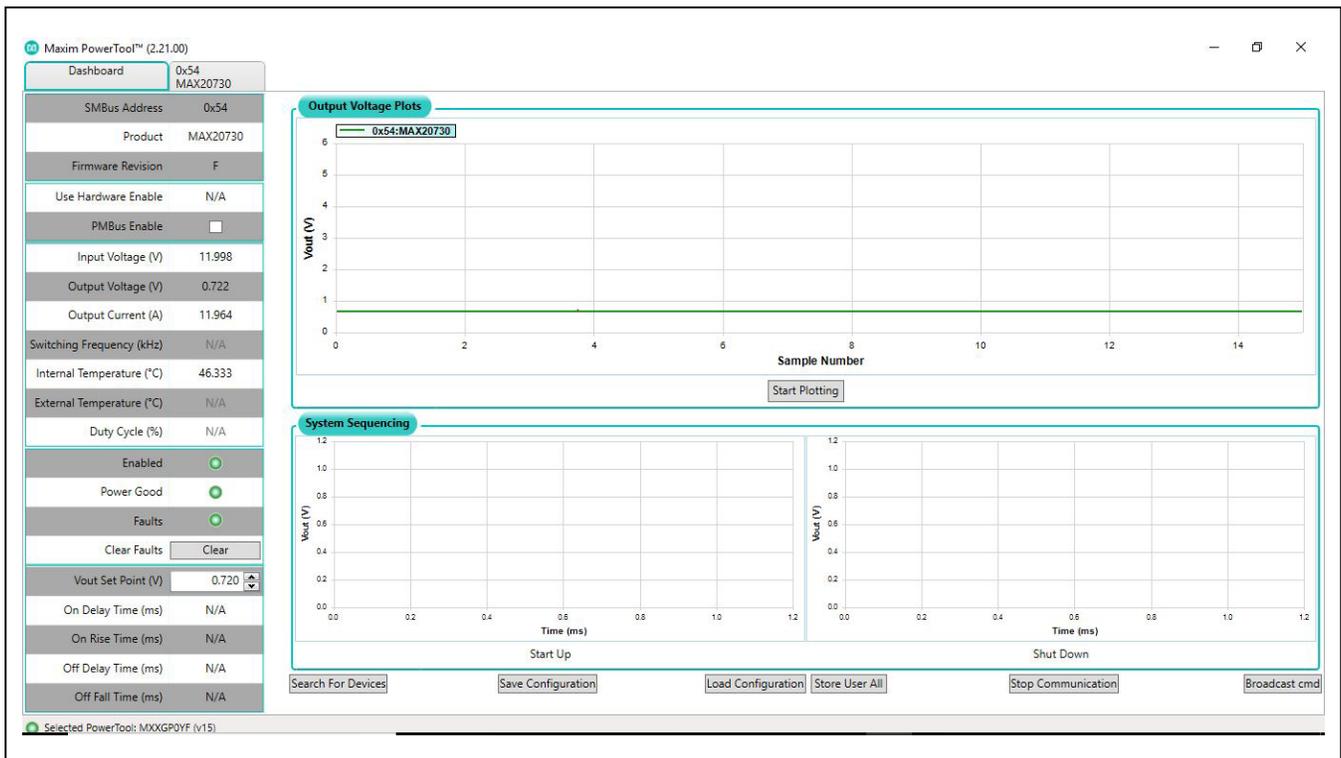


Figure 4. MAXPOWERTOOL002# GUI connected to the MAXREFDES1131.

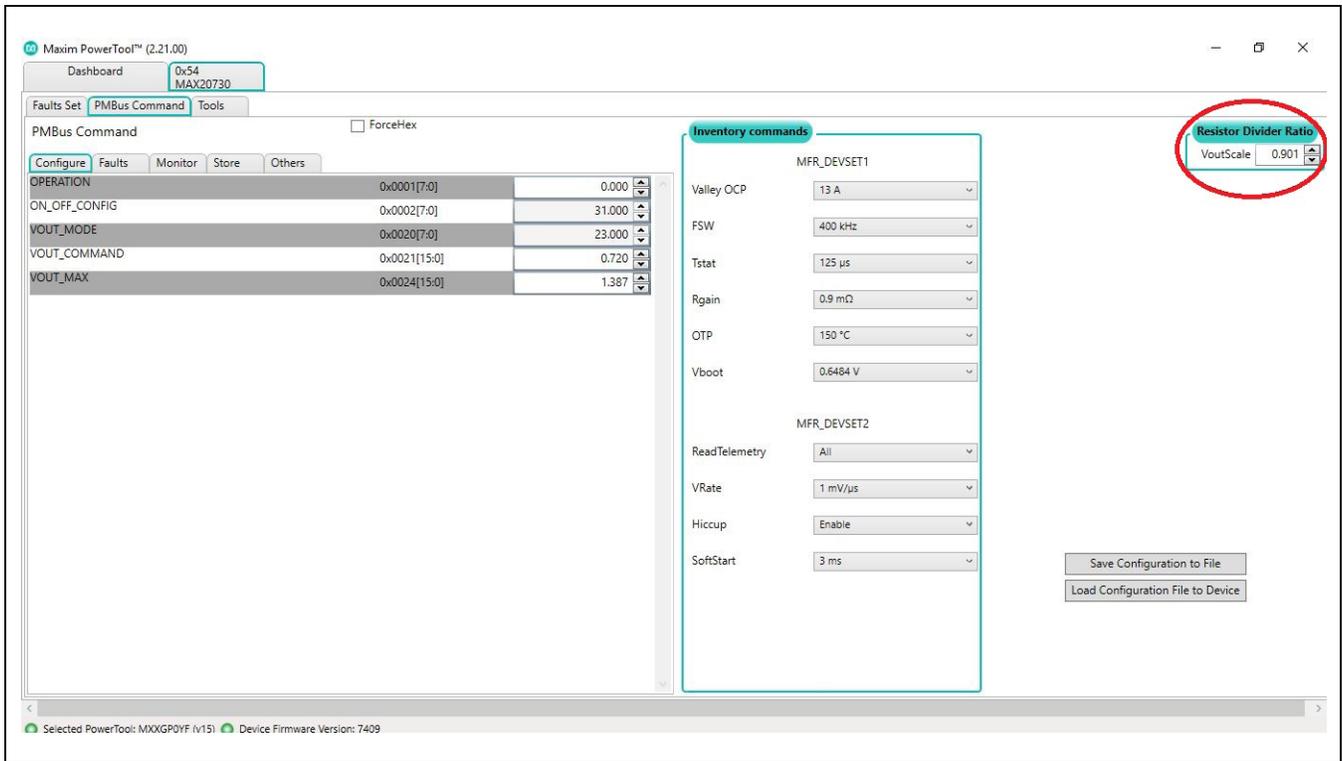


Figure 5. MAXPOWERTOOL002# GUI showing the output voltage scaling factor circled in red.

Design Resources

Download the complete set of [Design Resources](#) including the schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/19	Initial release	—

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