64W and 48W Dual Output DC-DC Buck Converter Using the MAX17559

MAXREFDES1039

Introduction

The MAX17559 is a dual-output, synchronous step-down controller that drives nMOSFETs. The device uses a constant-frequency, peak-current-mode architecture. The two outputs can be configured as independent voltage rails. Input capacitor size is minimized by running the two outputs 180° out of phase. The IC supports current sensing using either an external current-sense resistor for accuracy or an inductor DCR for improved system efficiency. Current foldback or latch-off limits MOSFET power dissipation under short-circuit conditions. The IC provides independent adjustable soft-starts/stops for each output and can start up monotonically into a pre-biased output. The IC can be configured in either PWM or DCM modes of operation, depending on whether constant-frequency operation or light-load efficiency is desired. The IC operates over the -40°C to +125°C temperature range and is available in a lead(Pb)-free, 7mm x 7mm, 32-pin TQFP, package.

Application

- Industrial Power Supplies
- Distributed DC Power Systems
- Motion Control
- Programmable Logic Controllers
- Computerized Numerical Control

Benefits and Features

Other features include:

- Wide 4.5V to 60V Input Voltage Range
- Wide 0.8V to 24V Output Voltage Range
- RSENSE or Inductor DCR Current-Sensing
- Fixed 180° Out-of-Phase Operation
- Adjustable 100kHz to 2.2MHz Switching Frequency
- Independent Enable and PGOOD
- Available in a Lead(Pb)-Free 7mm x 7mm, 32-Pin TQFP Package
- Enhances Power Efficiency
  - Low-Impedance Gate Drives for High Efficiency
- DCM Operation at Light Loads
- Auxiliary Bootstrap LDO
- Operates Reliably in Adverse Industrial Environments
- Independent Adjustable Soft-Start/Stop or Tracking
- Current Selectable Foldback or Latch-off Limits
- MOSFET Heat Dissipation During a Short-Circuit Condition
- Operates Over the -40°C to +125°C Temperature Range
- Output Overvoltage and Overtemperature Protections

Hardware Specification

A dual output buck converter using MAX17559 is demonstrated for 16V and 24V DC output application. The power supply delivers up to 4A at 16V and 2A at 24V. Table 1 shows an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	MAX
Input Voltage	V_{IN}	36V	51V
Frequency	f_{SW}	350kHz	
Output Voltage1	V_{OUT1}	16	
Output Voltage2	V_{OUT2}	24	
Output Current1	I_{OUT1}	0	4A
Output Current2	I_{OUT2}	0	2A
Output Voltage Ripple1	ΔV_{OUT1}	1% of V_{OUT1}	
Output Voltage Ripple2	ΔV_{OUT2}	1% of V_{OUT2}	
Output Power1	P_{OUT1}	64W	
Output Power2	P_{OUT2}	48W	
Maximum Efficiency 1	η_1	95%	
Maximum Efficiency 2	η_2	95%	

Designed–Built–Tested

This document describes the hardware shown in Figure 1. It provides a detailed systematic technical guide to designing a dual output buck converter using the Maxim MAX17559 current-mode controller. The power supply has been built and tested, details of which follow later in this document.

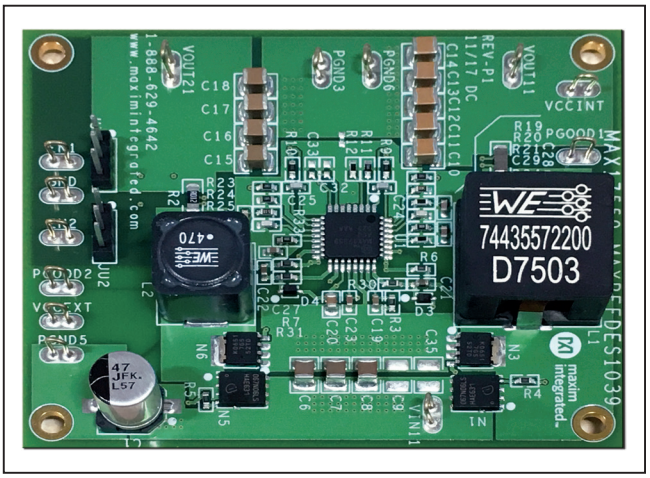

Figure 1. MAXREFDES1039 hardware.

Operation of a Buck Converter

The main components of a buck converter are the power switch, which usually comes in the form of a MOSFET, the inductor, and the diode. As the MOSFET is switched on and off, a magnetic field is generated in the inductor. When the switch is on (or closed), current flows into the inductor and through the output. When the switch is off (or open), due to the magnetic field, current still flows from the inductor to the output load. When the transistor switch is on, it supplies the output load with current. Initially, current flow to the load is restricted as energy is also being stored in the inductor. The current in the load and the charge on the output capacitor, therefore, build up relatively slowly compared with the switch-on time of the MOSFET. During the on period there is a large voltage across the diode, which causes it to be reverse-biased. When the transistor switch is off, the energy that had been stored in the inductor's magnetic field is released. The voltage across the inductor is now in reverse polarity, and sufficient stored energy is available to maintain current flow while the transistor is open. The reverse polarity of the inductor allows current to flow in the circuit through the load and the diode, which is now forward-biased. Once the inductor has been drained of the majority of its stored energy, the load voltage begins to fall, and the charge stored in the output capacitor then becomes the main source of current. This leads to the ripple waveform shown in Figure 2.

Proper interleaving of the phases reduces the input, and output ripple-current stress ensures high efficiency by equally sharing the load current. With the MAX17559, there is a 180° out-of-phase operation that reduces stress on the input capacitors. The 180° phase-shift operation between two output channels have the following advantages:

- Reduction of input and output capacitor RMS current
- Lower input-voltage ripple

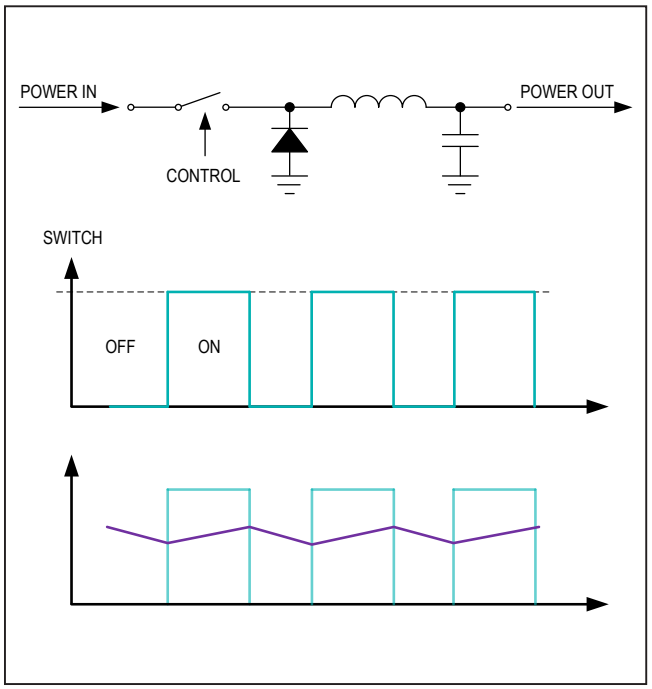

Figure 2. Typical buck converter power supply.

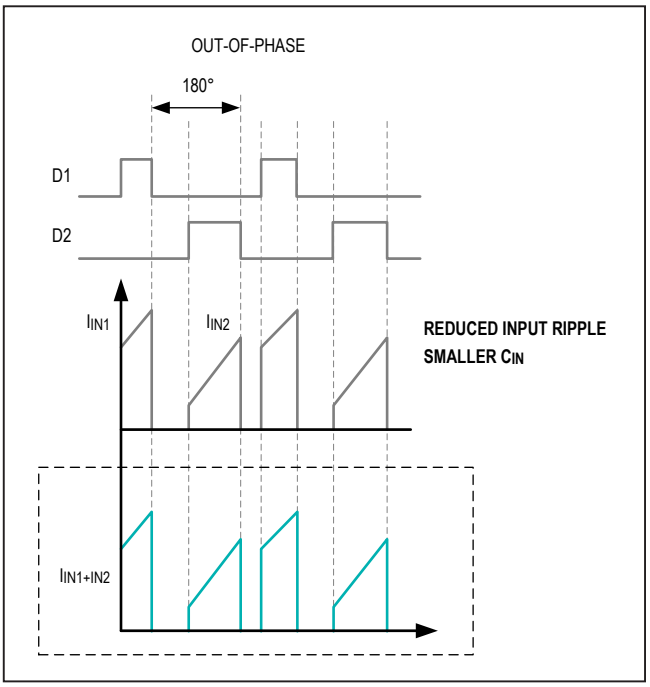

Figure 3. 180° out-of-phase operation reduces stress on the input capacitors.

Design Procedure for Dual-Output Buck Using MAX17559

Step 1: Selection of Switching Frequency

The selection of switching frequency involves a trade-off between efficiency and components size. Low-frequency operation increases efficiency by reducing MOSFET-switching losses and gate-drive losses, but requires a larger inductor and/or capacitor to maintain low output ripple voltage.

The switching frequency of the device can be programmed between 100kHz to 2.2MHz using the RT pin. A resistor RT is connected between the RT pin and GND for the setting of switching frequency. For this design we have selected a switching frequency of 350kHz for both the outputs. The following expression is used to find the required resistor for a given switching frequency.

$$R_{RT} = \frac{f_{SW} + 133}{8.8}$$

$$R_{RT} = \frac{350 + 133}{8.8} = 54.88k\Omega$$

A typical resistor of 54.9k is used as R_{RT}, R_{RT} = 54.9kΩ

Step 2: Selection of Inductors

Three key inductor parameters must be specified to select the output inductor.

1) Inductance (L)
2) Inductor saturation current (I_{SAT})
3) DC resistance of inductor (DCR)

The required inductance (L) is calculated based on the ratio of the inductor's peak-to-peak ripple AC current to its DC average current. This is called the inductor ripple current ratio, or LIR. In this design for both the outputs we have selected LIR of 0.3. The switching frequency f_{SW}, input voltage V_{IN}, output voltage V_{OUT}, and selected LIR then determine the inductor value as follows:

$$L = \frac{V_{OUT} \times (1 - D)}{LIR \times I_{LOAD} \times f_{SW}}$$

D is the duty cycle, which is equal to the ratio of V_{OUT} and V_{IN}. Depending on the variation in the input voltage range, the duty cycle (D_1) of the first output (V_{OUT1}) varies from 0.313 to 0.414. Similarly, the duty cycle (D_2) of the second output (V_{OUT2}) varies from 0.47 to 0.67. Substituting these in the above expression gives the minimum, typical, and maximum values of inductance L_1 and L_2 required for the two outputs as follows:

$$21.16\mu H \le 25.40\mu H \le 26.14\mu H$$

$$38.10\mu H \le 57.14\mu H \le 60.50\mu H$$

We selected L_1 = 47µH an L_2 = 22µH, respectively. The minimum inductor saturation current should be greater than the maximum inductor peak current that is given by the following expression:

$$I_{L\_Peak} = I_{OUT} + \frac{\Delta I_{L\_PK-PK}}{2}$$

$\Delta I_{L\_PK-PK(max)}$ is the maximum inductor ripple current and can be calculated as follows:

$$\Delta I_{L\_PK-PK(max)} = \frac{V_{OUT} \times \left[1 - \frac{V_{OUT}}{V_{INMAX}}\right]}{L \times f_{SW}}$$

The maximum inductor ripple currents $\Delta I_{L1\_PK-PK(max)}$ and $\Delta I_{L2\_PK-PK(max)}$ for the two outputs can be calculated as follows:

$$\Delta I_{L1\_PK-PK(max)} = \frac{16 \times \left[1 - \frac{16}{51}\right]}{22\mu \times 350k} = 1.426$$

$$\Delta I_{L2\_PK-PK(max)} = \frac{24 \times \left[1 - \frac{24}{51}\right]}{47\mu \times 350k} = 0.77$$

The peak inductor currents for the two outputs can be calculated as follows:

$$I_{L1\_Peak} = 4 + \frac{1.426}{2} = 4.71A$$

$$I_{L2\_Peak} = 2 + \frac{0.77}{2} = 2.386A$$

For V_{OUT1}, we selected the Würth Elektronik power inductor 74435572200 of 22µH with a saturation current limit of 11A. Similarly, for V_{OUT2}, we selected the Würth Elektronik power inductor 7447709470 of 47µH with a saturation current limit of 3.8A.

Step 3: Current Sense Resistor Selection

The current-sensing is performed by an external current-sense resistor for both the outputs. The current sense resistors values can be calculated as follows:

$$R_{SENSE} = \frac{V_{CS}}{I_{LOAD(max)} + \frac{\Delta I_{L\_PK-PK(max)}}{2}}$$

V_{CS} is the selected current sense threshold of 30mV. The current sense resistors for the two outputs can be calculated as follows:

$$R_{SENSE1} = \frac{30m}{4 + \frac{1.426}{2}} = 6.36m\Omega$$

$$R_{SENSE2} = \frac{30m}{2 + \frac{0.77}{2}} = 12.57m\Omega$$

Typical values of 6mΩ and 12mΩ are selected as R_{SENSE1} and R_{SENSE2}, respectively. The power rating requirements of the selected current sense resistors are calculated as follows:

$$P_{RSENSE} = I_{OUT}{}^2 + \frac{\Delta I_{L\_PK-PK}^2}{12}$$

Substituting values in the above expression, we get:

$$P_{RSENSE1} = 4^2 + \frac{1.426^2}{12} = 97mW$$

$$P_{RSENSE1} = 2^2 + \frac{0.77^2}{12} = 48.5mW$$

Step 4: Peak Current Limit Programming

The device features an adjustable peak-current-limit threshold independently for each controller. Connect a resistor from the ILIM_ pin to GND to program the current limit. The resistor value can be calculated using the following expression:

$$R_{ILIM(k\Omega)} = \frac{ILIM\_THRESHOLD}{5\mu \times 50}$$

Where $ILIM_{\_THRESHOLD}$ can be calculated from the following expression:

$$ILIM\_THRESHOLD = \left[I_{OUT} + \frac{\Delta I_{L\_PK-PK(max)}}{2} \right] \times R_{SENSE}$$

For the two outputs $ILIM_{\_THRESHOLD}$ can be calculated as follows:

$$ILIM1\_THRESHOLD = \left[4 + \frac{1.426}{2} \right] \times 6m = 28.27mV$$

$$ILIM2\_THRESHOLD = \left[2 + \frac{0.77}{2} \right] \times 12m = 28.62mV$$

Based on the above results the R_{ILIM} for the two outputs can be calculated as follows:

$$R_{ILIM1(k\Omega)} = \frac{28.27m}{5\mu \times 50} = 140k\Omega$$

$$R_{ILIM2(k\Omega)} = \frac{28.63m}{5\mu \times 50} = 140k\Omega$$

Typical resistor values of 140kΩ are selected as R_{ILIM1} and R_{ILIM2}.

Step 5: Setting Output voltages

The output voltage of each output is set by connecting a resistor-divider (comprising resistors R_1 and R_2) to the FB_ pin from the corresponding output to GND (Figure 4).

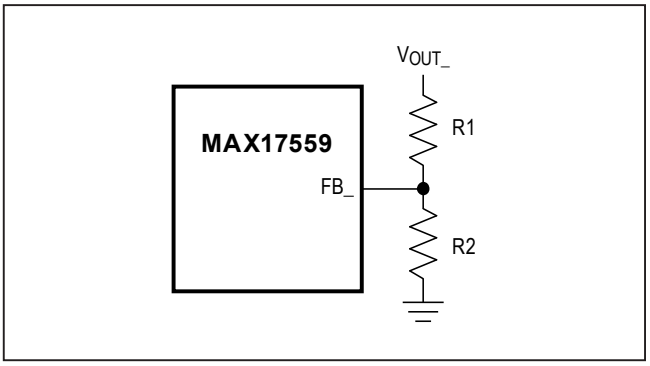

Figure 4. Output-voltage programming.

Assuming 0.2% offset present on the V_{OUT} we can calculate output voltage offsets for the two outputs. The calculated values of offsets α1 and α2 will be 32mV and 48mV, respectively. The expression below gives maximum possible values of R_1 as follows:

$$R_1 \le \frac{\alpha}{I_{FB\_}}$$

Where $I_{FB\_}$ is the maximum leakage current of the FB_ pin and is equal to 0.1µA. The maximum values of R_1 for the two outputs can be calculated as follows:

$$R_{1\_1} \le \frac{32m}{0.1\mu} \Rightarrow R_{1\_1} \le 320k\Omega$$

$$R_{1\_2} \le \frac{48m}{0.1\mu} \Rightarrow R_{1\_2} \le 480k\Omega$$

In our design we have selected a typical value of 200kΩ as R_{1_1} and R_{1_2}.

The value of R_2 can be calculated as follows:

$$R_2 = \frac{R_1}{\frac{V_{OUT}}{0.8} - 1}$$

The corresponding values of R_2 for the two outputs can be calculated as follows:

$$R_{2\_1} = \frac{200k}{\frac{16}{0.8} - 1} = 10.5k\Omega$$

$$R_{2\_2} = \frac{200k}{\frac{24}{0.8} - 1} = 6.89k\Omega$$

Typical resistor values of 10.5kΩ and 6.8kΩ are selected for R_{2_1} and R_{2_2}, respectively.

Step 6: Enable and Setting Input Under Voltage Lockout

The two controllers of the IC can be independently shut down and enabled using the EN1 and EN2 pins. In this design, the EN pins are left unconnected to have both outputs on all of the time. However, if required, a resistor divider can be used to set up the input under voltage lockout level, as explained in the datasheet.

Step 7: Soft-Start

The soft-start/stop time of each controller's output voltage is controlled by the voltage on the relevant SS_ pin for that controller. When the voltage on the SS_ pin is less than the 0.8V internal reference, the device regulates the FB_ voltage to the SS_ pin voltage, instead of the 0.8V internal fixed reference. This allows the SS_ pin to be used to program the output voltage soft-start/stop time by connecting an external capacitor from the SS_ pin to GND. For this design we have set a soft-start time of 10.8ms for both the outputs. The soft-start capacitor value can be calculated based on the following expression:

$$C_{SS} = t_{SS} \times \frac{5\mu A}{0.8V}$$

The soft-start capacitors for the two outputs can be calculated as follows:

$$C_{SS1} = 10.8m \times \frac{5\mu A}{0.8V} = 67.5nF$$

$$C_{SS2} = 10.8m \times \frac{5\mu A}{0.8V} = 67.5nF$$

A typical capacitor of 68nF is selected as C_{SS1} and C_{SS2}. A typical resistor of 2kΩ is used in series with both the soft-start capacitors, as stated in the datasheet.

Step 8: Operation Under Current Limit (ILIMSEL)

For this design, latch-off mode is selected for the current limit. Under an overcurrent limit condition, whenever the output voltage drops below 70% of its set value, the controller enters latch-off mode and both the high and low-side MOSFETs are kept off. The latch-off is not active during soft-start. The controller remains idle until the corresponding EN_ pin or the IC supply is cycled to GND and activated again. The ILIMSEL pin of both outputs is connected to GND to configure this mode.

Step 9: Light-Load Current Operation (SKIP)

The MAX17559 can be configured to operate in either discontinuous-conduction mode (DCM) for high light-load efficiency or fixed-frequency pulse-width-modulation (PWM) mode. In this design we have selected the PWM mode of operation under light-load conditions and connected the SKIP pin to V_{CCINT}.

Step 10: Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. For each output channel, the input capacitance required for a specified input-ripple ΔV_{IN} can be calculated using the following expression:

$$C_{IN} = \frac{I_{LOAD} \times D \times (1-D)}{\eta \times \Delta V_{IN} \times f_{SW}}$$

D = Duty Cycle

Η = Target efficiency

ΔV_{IN} = Allowed Peak to Peak ripple voltage

For a D = 0.5 (worst case), Η = 95% and ΔV_{IN} = 2% of V_{INmin} the minimum input capacitor values for both the outputs can be calculated as follows:

$$C_{IN1} = \frac{4 \times 0.5 \times (1-0.5)}{0.95 \times 0.720 \times 350k} = 4.177\mu F$$

$$C_{IN2} = \frac{2 \times 0.5 \times (1-0.5)}{0.95 \times 0.720 \times 350k} = 2.085\mu F$$

Considering capacitors derating due to component tolerances, temperature, and DC biasing, 3 x 4.7µF 80V capacitors are used as C_{IN} for both controllers.

Step 11: Output Capacitor Selection

The key selection parameters for the output capacitor are capacitance value, ESR, and voltage rating. These parameters affect the overall stability, output ripple voltage, and transient response. The output capacitor is chosen to have 3% output voltage deviation for a 50% load step of the rated output current. The bandwidth is usually selected in the range of F_{SW}/10 to F_{SW}/20. For the present design, the bandwidth is chosen as F_C = 23.33kHz.

$$T_{RESPONSE} \cong \left(\frac{0.33}{F_C} + \frac{1}{F_{SW}}\right) = \frac{0.33}{23.33k} + \frac{1}{350k} = 17\mu s$$

The required output capacitance can be calculated from the expression below:

$$C_{OUT} = \frac{I_{STEP} \times T_{RESPONSE}}{2 \times \Delta V_{OUT}}$$

I_{STEP} is equal to 50% of the full load current for both the outputs. This is equal to 2A and 1A for V_{OUT1} and V_{OUT2} respectively. From the above expression, the required output capacitance for the two outputs can be calculated as follows:

$$C_{OUT1} = \frac{I_{STEP} \times T_{RESPONSE}}{2 \times \Delta V_{OUT}} = \frac{2 \times 17\mu}{2 \times 0.480} = 35.4\mu F$$

$$C_{OUT2} = \frac{I_{STEP} \times T_{RESPONSE}}{2 \times \Delta V_{OUT}} = \frac{1 \times 17\mu}{2 \times 0.720} = 11.8\mu F$$

A ceramic capacitor of 22µF 25V degrades to 7µF at 16V. Hence five 22µF, 25V capacitors are selected as C_{OUT1} for V_{OUT1}.

Similarly, a ceramic capacitor of 4.7µF 50V degrades to 3.2 µF at 24V. Hence, four 4.7µF, 50V capacitors are selected as C_{OUT2} for V_{OUT2}.

The total ESR of selected output capacitors is as follows:

ESR1 = 0.4mΩ

ESR2 = 0.75mΩ

Step 12: Loop Compensation

The controller uses a peak-current-mode-control scheme that regulates the output voltage by forcing the required current through the external inductor. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor, in the case of voltage mode control, resulting in a smaller phase-shift and requiring less elaborate error-amplifier compensation. Typical type-II compensation used with peak current-mode control is shown in Figure 5.

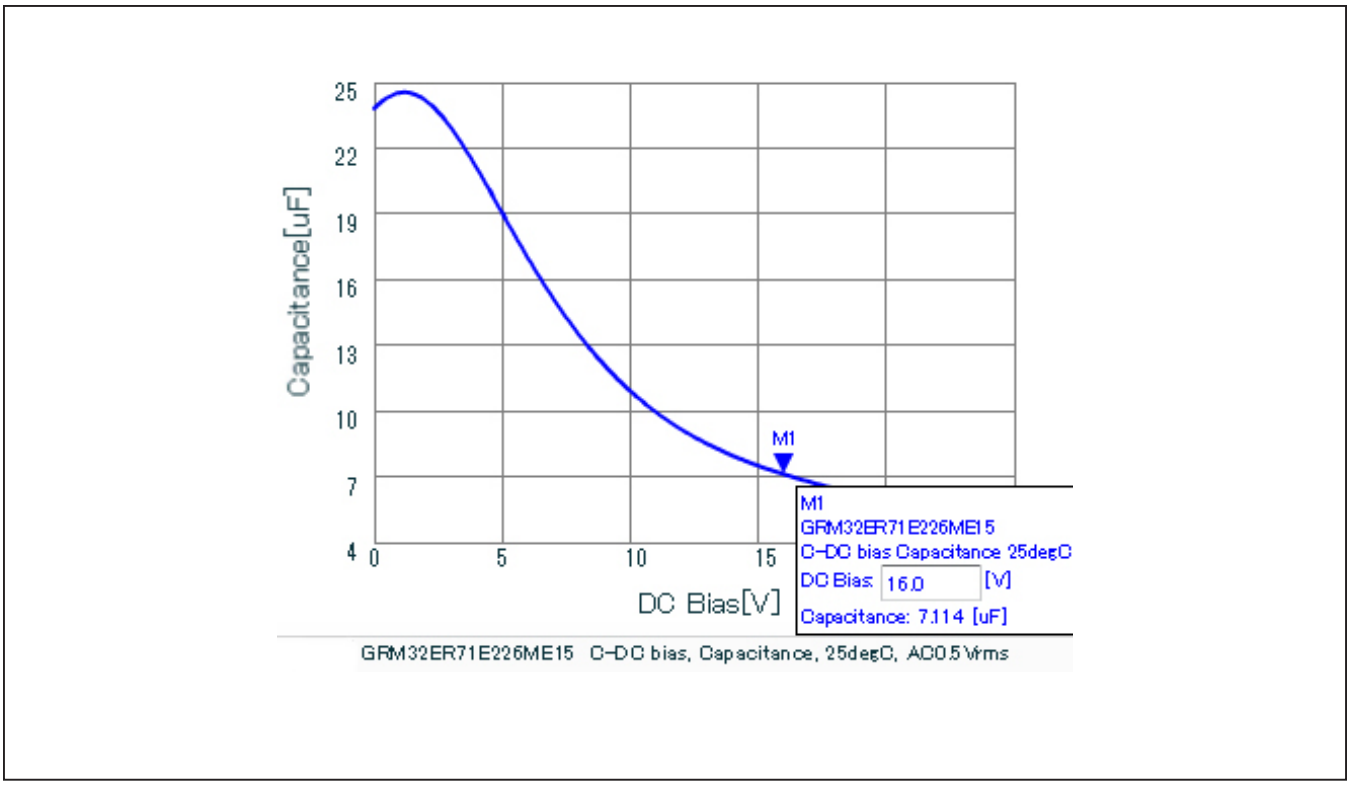

Figure 5. DC bias characteristic of C_{OUT1}.

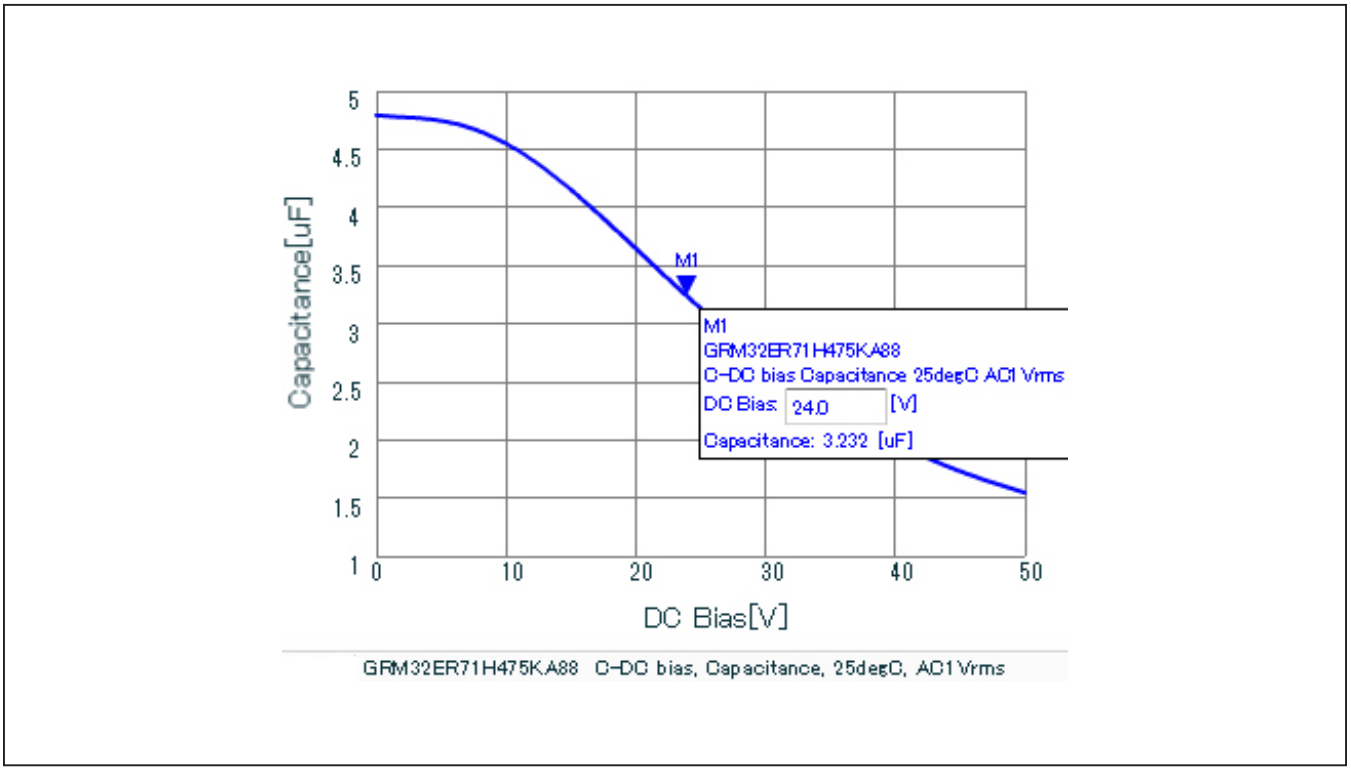

Figure 6. DC bias characteristic of C_{OUT2}.

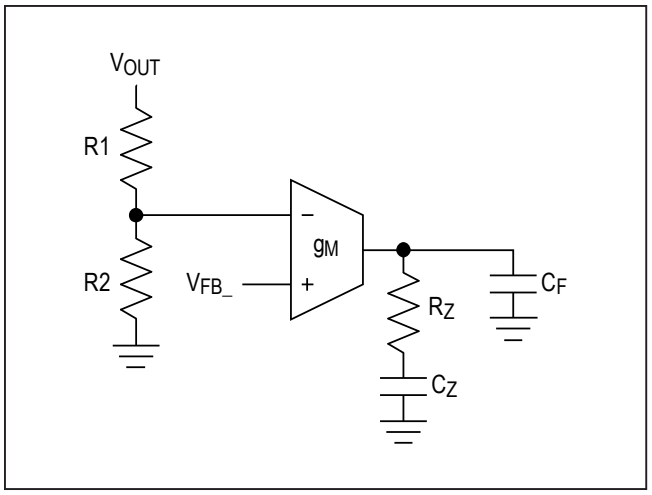

Figure 7. Typical Type-2 Compensation Network

Calculate the compensation resistor R_Z using the following expression:

$$R_Z = \frac{2 \times \pi \times f_{CO} \times C_{OUT} \times G_{CS} \times R_{SENSE}}{g_M \times G_{FB}}$$

f_{CO} = Cut-off frequency of 23.33kHz

C_{OUT} = Worst-case output capacitance, C_{OUT1} = 35µF and C_{OUT2} = 12.8µF

G_{CS} = Current-sense amplifier gain of 12

g_M = Internal transconductance amplifier gain of 2m A/V

G_{FB} = Output voltage feedback divider gain of (0.8/VOUT), G_{FB1} = 0.05 and G_{FB2} = 0.033

Compensation resistor values for the two outputs can be calculated as follows:

$$R_{Z1} = \frac{2 \times \pi \times 23.33k \times 35\mu \times 12 \times 6m}{2m \times 0.05} = 3.69k\Omega$$

$$R_{Z2} = \frac{2 \times \pi \times 23.33k \times 12.8\mu \times 12 \times 12m}{2m \times 0.033} = 4.05k\Omega$$

Typical resistor values of 4.12k and 4.42k are selected as R_{Z1} and R_{Z2}, respectively.

f_{P_Load} is the load pole frequency that can be calculated as follows:

$$f_{P\_Load} = \frac{1}{2 \times \pi \times C_{OUT} \times \frac{V_{OUT}}{I_{LOAD}}}$$

For both outputs, the load pole frequency can be calculated as follows:

$$f_{P\_Load1} = \frac{1}{2 \times \pi \times 35\mu \times \frac{16}{4}} = 1136.8Hz$$

$$f_{P\_Load2} = \frac{1}{2 \times \pi \times 12.8\mu \times \frac{24}{2}} = 1036.16Hz$$

C_Z is calculated using the following expression:

$$C_Z = \frac{1}{2 \times \pi \times f_{P\_Load} \times R_Z}$$

For both outputs the C_Z can be calculated as follows:

$$C_{Z1} = \frac{1}{2 \times \pi \times 1136.8 \times 4.12k} = 33.98nF$$

$$C_{Z2} = \frac{1}{2 \times \pi \times 1036.16 \times 4.42k} = 33.75nF$$

A typical capacitor of 33nF is selected as C_{Z1} and C_{Z2}.

The minimum of ESR zero frequency given by the following expression:

$$f_{Z\_ESR} = \frac{1}{2 \times \pi \times C_{OUT} \times ESR}$$

For both outputs, the f_{Z_ESR} can be calculated as follows:

$$f_{Z\_ESR1} = \frac{1}{2 \times \pi \times 35\mu \times 0.4m} = 11368.2kHz$$

$$f_{Z\_ESR2} = \frac{1}{2 \times \pi \times 12.8\mu \times 0.75m} = 16578.6kHz$$

Calculate C_F using the following expression:

$$C_F = \frac{1}{2 \times \pi \times R_Z \times f_{P\_EA}}$$

f_{P_EA} is the pole frequency created by R_Z and C_F, and we set it to the minimum ESR zero frequency calculated above. For both outputs the C_F can be calculated as follows:

$$C_{F1} = \frac{1}{2 \times \pi \times 4.12k \times 11368.2k} = 3.39pF$$

$$C_{F1} = \frac{1}{2 \times \pi \times 4.42k \times 16578.6k} = 2.17pF$$

A typical capacitor of 3.3pF is selected as C_{F1} and C_{F2}.

Step 13: External MOSFET Selection

Each controller drives two external, logic-level nMOSFETs as the circuit switch elements. The key selection parameters to choose these MOSFETs include:

- On-resistance $R_{DS(ON)}$
- Maximum drain-to-source voltage $V_{DS(max)}$
- Miller Plateau voltage on high side MOSFET Gate (VMIL).
- Total gate charge Q_{Gate}
- Output capacitance C_{OSS}
- Power dissipation rating and package thermal resistance

Both MOSFETs must be logic-level types with guaranteed on-resistance specifications at V_{GS} = 4.5V. A 60V 50A MOSFET BSC067N06LS3 G from Infineon is used as the high-side MOSFET for both outputs. A 60V 45A MOSFET RJK0653DPB-00#J5 from Renesas Technology Corporation is used as the low-side MOSFET for both outputs.

Step 13: Bootstrap Selection

The selected high-side MOSFET determines the appropriate bootstrap capacitance values according to the following expression:

$$C_{BST} = \frac{Q_{Gate}}{\Delta V_{BST}}$$

Q_{Gate} = Total gate charge of high side MOSFET which is 15n C for the selected high side MOSFET

ΔV_{BST} = Voltage variation allowed on the high-side MOSFET driver after turn-on. It is selected to be equal to 100m V as advised in the datasheet.

The minimum bootstrap capacitance value for both the outputs can be calculated as follows:

$$C_{BST1} = \frac{15nC}{100mV} = 150nF$$

$$C_{BST2} = \frac{15nC}{100mV} = 150nF$$

A typical value of 1µF is selected as bootstrap capacitor for both the outputs.

Design Resources

Download the complete set of **Design Resources** including schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/18	Initial release	—

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

© 2018 Maxim Integrated Products, Inc. All rights reserved. Maxim Integrated and the Maxim Integrated logo are trademarks of Maxim Integrated Products, Inc., in the United States and other jurisdictions throughout the world. All other marks are the property of their respective owners.