5A/12V Step-Down DC-DC Converter with Integrated HS Switch and External LS Switch Using the MAX17506

MAXREFDES1032

Introduction

The MAX17506 is a high-efficiency switching regulator that delivers up to 5A load current at output voltages from 0.9V to (0.9 x V_{IN}). The device integrates the high-side MOSFET and operates over 4.5V to 60V, making it ideal for on-board point-of load and post-regulation applications.

The device features a peak current-mode control architecture. Built-in compensation across the output voltage range eliminates the need for external compensation components. The feedback regulation accuracy over -40°C to +125°C is ±1.4%

Output overload hiccup protection and cycle-by-cycle peak-current limit provide for ultra-safe operation in short-circuit conditions.

Other features include the following:

- No Schottky-Synchronous Operation
- Internal Compensation for Any Output Voltage
- Built-In Soft-Start
- 100kHz to 2.2MHz Adjustable Switching Frequency
- 3.5µA Shutdown Current
- Hiccup or Latchoff Mode Overload Protection
- Programmable EN/UVLO Threshold
- Overtemperature Protection

Hardware Specification

In this document a step-down DC-DC converter using the MAX17506 is demonstrated for a 12V output application. The power supply delivers up to 5A at 12V. Table 1 shows an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	MAX
Input Voltage	V_{IN}	24V	36V
Input Voltage Ripple	ΔV_{IN}	720mV	
Frequency	f_{SW}	710kHz	
Efficiency	η	92%	
Output Voltage	V_{OUT}	12V	
Output Voltage Ripple	ΔV_{OUT}	120mV	
Output Current	I_{OUT}	5A	
Output Power	P_{OUT}	60W	

Designed–Built–Tested

This document describes the hardware shown in Figure 1. It provides a detailed systematic technical guide to designing a step-down (buck) DC-DC converter using Maxim's MAX17506 current-mode controller. The power supply has been built and tested, details of which follow later in this document.

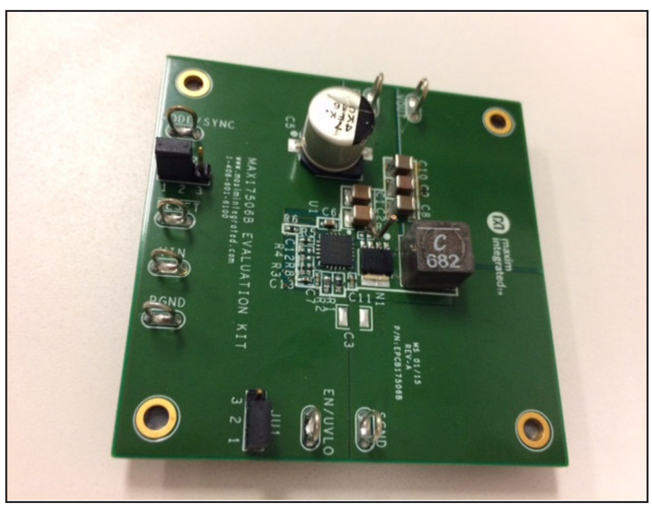

Figure 1. MAXREFDES1032 hardware.

The Synchronous Buck

The MAX17506 is a synchronous buck converter. Synchronous buck converters, as opposed to conventional buck converters, can achieve high efficiency in today's low-voltage, high-current applications because they replace the catch diode of buck converters with a MOSFET. As a result, the power they dissipate in the off-period is reduced significantly.

Figure 2 shows the basic operation of the synchronous buck converter. During the first cycle when the high-side switch Q1 is on, the input current gradually rises and flows through the inductor and output capacitor. This results in energy being stored in the inductor and the capacitor.

During the second cycle, the high-side switch Q1 turns off and after some dead-time the low-side switch Q2 turns on. This results in the energy stored in the magnetic field of the inductor being released back into the circuit. As the energy stored in the inductor decreases, the capacitor starts discharging, keeping the current flowing until the next cycle. In steady-state conditions, this cycle of turning the high-side and low-side switches on and off complementary to each other regulates the output voltage to its set value.

To prevent cross-conduction (both the high-side and the low-side switches are on simultaneously), the switching scheme must be break-before-make. Because of this, a small diode is still required to conduct during the interval between the high-side turning off and the low-side turning on (dead time). When a MOSFET is used as a synchronous switch, the current normally flows in reverse (source to drain), and this allows the integrated body diode to conduct current during the dead time. When the synchronous rectifier switch is on, the current flows through the MOSFET channel. Because of the very low-channel resistance for power MOSFETs, the standard forward drop of the rectifying diode can be reduced to a few millivolts. Synchronous rectification can provide efficiencies well above 90%.

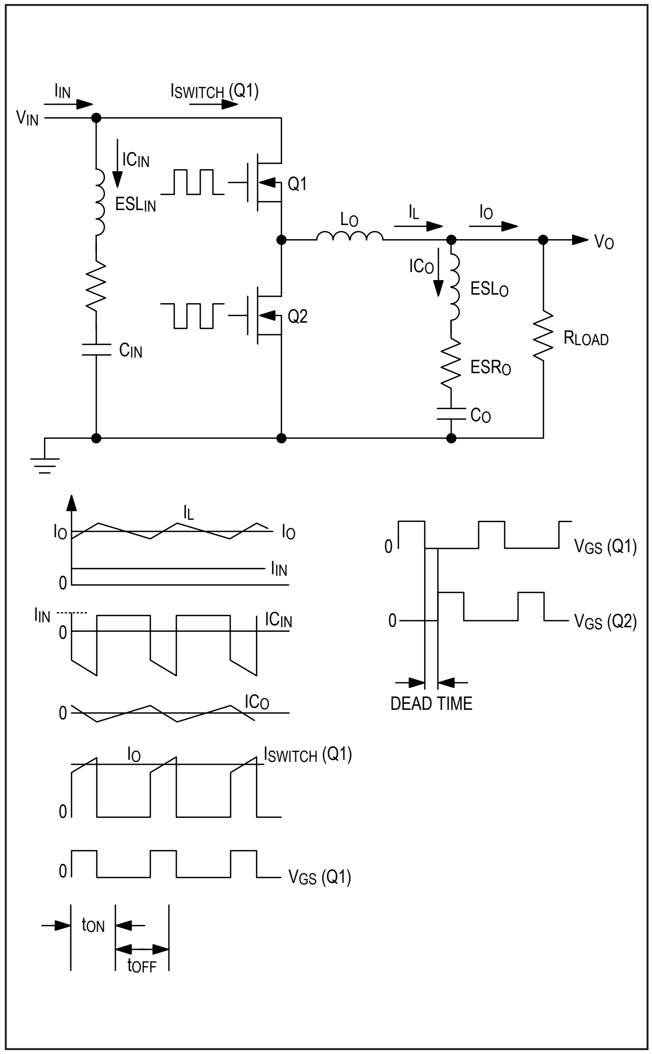

Figure 2. Synchronous buck waveforms.

Design Procedure for Step-Down DC-DC Converter Using MAX17506

Now that the principle of the synchronous buck converter operation is understood, a practical design example can be illustrated. The converter design process can be divided into three parts: the power stage design, the setup of MAX17506 current-mode controller, and closing the control loop. This document is intended to complement the information contained in the MAX17506 data sheet.

The following design parameters are used throughout this document:

SYMBOL	FUNCTION
V_{IN}	Input Voltage
V_{FB}	Feedback Threshold
V_{OUT}	Output Voltage
ΔV_{OUT}	Output ripple voltage
I_{OUT}	Output current
f_{SW}	Switching frequency
D	Duty cycle

Step 1: Choosing a Suitable Switching Frequency

The MAX17506 switching frequency can be programmed from 100kHz to 2.2MHz by using a resistor connected from the RT pin to SGND. The switching frequency (f_{SW}) is related to the resistor connected at the RT pin (R_{RT}) by the following equation:

$$R_{RT} = \frac{19 \times 10^3}{f_{SW}} - 1.7$$

where R_{RT} is in kΩ and f_{SW} is in kHz. Leaving the RT pin open causes the device to operate at the default 500kHz switching frequency. For our design, a 24.9kΩ resistor was used for R_{RT} to obtain approximately 710kHz switching frequency.

Step 2: Selecting the Inductor

A high-valued inductor results in reduced inductor-ripple current, leading to a reduced output-ripple voltage. However, a high-valued inductor results in either a larger physical size or a high series resistance (DCR) and a lower saturation current rating. Typically, we choose an inductor value to produce a current ripple ΔI_L equal to 30% of load current, giving a LIR of 0.3.

We select the inductor with the following equation:

$$L = \frac{V_{OUT}}{f_{SW} \times LIR \times I_{LOAD}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$L = \frac{12}{710\text{kHz} \times 0.3 \times 5}\left(1 - \frac{12}{36}\right) = 7.5\mu\text{H}$$

Select the inductor value L = 6.8µH with saturation current that is higher than the peak current.

$$I_{PK} = I_{OUT} + \frac{1}{2}\Delta I_{L(P-P)}$$

where the inductor ripple current is:

$$\Delta I_{L(P-P)} = \frac{(V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

For our design:

$$\Delta I_{L(P-P)} = \frac{(36 - 12) \times \frac{12}{36}}{6.8\mu\text{H} \times 710\text{kHz}} = 1.66\text{A}$$

$$I_{PK} = 5 + \frac{1}{2}(1.66) = 6.83\text{A}$$

Choose Coilcraft XAL8080-682 with 14A saturation current rating.

Step 3: Selecting the Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The discontinuous input-current waveform of the buck converter causes large ripple currents in the input capacitor. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple dictate the capacitance requirement. The device's high switching frequency allows the use of smaller value input capacitors.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = \left[\frac{\left[V_{OUT} \times (V_{IN} - V_{OUT})\right]^{0.5}}{V_{IN}}\right] \times I_{OUT(MAX)}$$

For our example:

$$I_{RMS} = \left[\frac{\left[12 \times (36 - 12)\right]^{0.5}}{36}\right] \times 5 = 2.36\text{A}$$

where $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so $I_{RMS(MAX)} = I_{OUT(MAX)}/2$. Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \left(\frac{I_{OUT(MAX)} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{INRIPPLE}}\right)$$

For our example with a maximum high ripple voltage of 720mV:

$$C_{IN} = \left(\frac{5A \times 0.333 \times (1-0.333)}{0.9 \times 710kHz \times 720mV}\right) \approx 2.4\mu F$$

where D = V_{OUT}/V_{IN} is the duty ratio of the controller, f_{SW} is the switching frequency, $\Delta V_{INRIPPLE}$ is the allowable input voltage ripple, and η is the efficiency. In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

If we allow for a ±10% capacitor tolerance and a further reduction of 40% capacitance due to the DC bias effect (operating an 100V ceramic capacitor at 36V), our final nominal value is:

$$C_{IN} = \frac{2.4\mu F}{90\% \times 60\%} \approx 4.4\mu F$$

We can achieve this by placing two 2.2µF ceramic capacitors (Murata GRM32ER72A225KA35) in parallel. The AC current in each capacitor is:

$$\frac{I_{RMS}}{2} \approx 1.2A_{RMS}$$

which is well within specification for the selected capacitor.

Step 4: Selecting the Output Capacitor

The output capacitor is chosen to have 4% output voltage deviation for a 50% load step of the rated output current. The bandwidth (closed-loop crossover frequency, f_C) is selected to be $f_{SW}/9$ if the switching frequency is less than or equal to 450kHz. If the switching frequency is more than 450kHz, select the bandwidth to be 50kHz. For the present design, the bandwidth is chosen as 50kHz since the switching frequency is 710kHz.

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}}\right)$$

$$t_{RESPONSE} \cong \frac{0.33}{50k} + \frac{1}{710k} = 8\mu s$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{2 \times \Delta V_{OUT}}$$

$$C_{OUT} = \frac{2.5 \times 8\mu}{2 \times 4 \times 0.120} = 21\mu F$$

If we allow for a ±10% capacitor tolerance and a further reduction of 20% capacitance due to the DC bias effect (operating a 25V ceramic capacitor at 12V), our final nominal value is:

$$C_{OUT} = \frac{21\mu F}{90\% \times 80\%} \approx 29\mu F$$

We can achieve this by placing three 10µF ceramic capacitors (Murata GRM32DR71E106KA12K) in parallel.

Step 5: Setting the Output Voltage

The MAX17506 output voltage is adjustable from 0.9V to $0.9V_{IN}$ by connecting the FB to the center tap of the resistor-divider between the output and the SGND. Calculate resistor R3 from the output to FB as follows:

$$R3 = \frac{451 \times 10^3}{f_C \times C_{OUT}}$$

where R3 is in kΩ, crossover frequency f_C is in kHz, and output capacitor is in µF. Since the switching frequency is more than 450kHz, select f_C to be 50kHz.

Calculate resistor R4 from FB to SGND as follows:

$$R4 = \frac{0.9 \times R3}{(V_{OUT} - 0.9)}$$

For our design, select R3 = 392kΩ, ±1%:

$$R3 = \frac{451 \times 10^3}{50kHz \times 23\mu F} = 392.2k\Omega$$

For our design, select R4 = 31.6kΩ, ±1%:

$$R4 = \frac{0.9 \times 392k}{(12 - 0.9)} = 31.8k\Omega$$

Design Resources

Download the complete set of **Design Resources** including the schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/17	Initial release	—