Selectable Single-Output SEPIC Converter Using MAX16990

MAXREFDES1017

Introduction

The MAX16990 is a high-performance, current-mode PWM controller with 4µA (typ) shutdown current for wide input voltage range boost/SEPIC converters. The 4.5V to 36V input operating voltage range makes this device ideal in automotive applications such as for front-end "pre-boost" or "SEPIC" power supplies and for the first boost stage in high power LED lighting applications. An internal low-dropout regulator (PVL regulator) with a 5V output voltage enables the MAX16990 to operate directly from an automotive battery input. The input operating range can be extended to as low as 2.5V when the converter output is applied to the SUP input. The MAX16990 operates in different frequency ranges. It can be synchronized to an external master clock using the FSET/SYNC input. In addition, the MAX16990 has a factory-programmable spread-spectrum option. It is available in compact 12-pin TQFN and 10-pin µMAX® packages.

Main features include the following:

- Minimized Radio Interference with 2.5MHz Switching Frequency Above the AM Radio Band
- Space-Efficient Solution Design with Minimized External Components
  - 100kHz to 1MHz Switching-Frequency Range
  - 12-Pin TQFN (3mm x 3mm) and 10-Pin µMAX Packages
- Spread Spectrum Simplifies EMI Management Design
- Flexibility with Available Configurations for Boost, SEPIC, and Multiphase Applications
  - Adjustable Slope Compensation
  - Current-Mode Control
  - Internal Soft-Start (9ms)
- Protection Features Support Robust Automotive Applications
  - Operating Voltage Range Down to 4.5V (2.5V or Lower in Bootstrapped Mode), Immune to Load-Dump Transient Voltages Up to 42V
  - PGOOD Output and Hiccup Mode for Enhanced System Protection
  - Overtemperature Shutdown
  - -40°C to +125°C Operation

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Hardware Specification

A single-output SEPIC converter using the MAX16990 is demonstrated for a 18V to 32V input voltage range application. The output is selectable to be equal to either +24V or +5V using configurable jumpers present on the PCB. The power supply delivers up to 0.9A max load current. Table 1 shows an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	MAX
Input Voltage	V_{IN}	18V	32V
Frequency	f_{SW}	500kHz	
Maximum Efficiency	η	88%	
Output Voltage	V_{OUT}	24V/5V	
Output Voltage Ripple	ΔV_{OUT}	1% of V_{OUT} max	
Output Current	I_{OUT}	0.35A (typ), 0.9A (max)	
Maximum instantaneous Output Power	P_{OUT}	21.6W	

Designed–Built–Tested

This document describes the hardware show in Figure 1. It provides a detailed systematic technical guide to designing a SEPIC converter using Maxim's MAX16990 current mode controller. The power supply uses uncoupled inductors and has been built and tested, details of which follow later in this document.

Figure 1. MAXREFDES1017 hardware.

Board Configuration

The board can be configured to output either +24V or +5V. Configure jumpers JU1, JU2, JU3, JU6, and JU7 to either +5V or 24V as marked on the PCB silkscreen. Jumpers JU4 and JU5 must be installed for proper board operation.

SEPIC Principle

The single-ended primary inductor converter (SEPIC) is a type of DC-DC voltage converter ("regulator") that can step-up ("boost") or step-down ("buck") an input voltage. In other words, the output of a SEPIC converter can be greater than, equal to, or less than the applied input voltage. The conventional buck/boost converter can do this too, but the SEPIC has a number of advantages that are discussed later in this document.

The SEPIC converter architecture is originally based on the boost topology. In a boost converter when the switch is closed, the magnetic energy stored in the inductor (L1) increases and current flows through the switch to ground. The diode (D1) is reverse-biased. When the switch is open, the output capacitor (C2) and the output load are the only paths for the stored magnetic energy in the inductors to flow. In this case, V_{OUT} must be greater than V_{IN}. Otherwise, D1 is always forward-biased and nothing prevents current flow from V_{IN} to V_{OUT}. The SEPIC eliminates this constraint by inserting a series capacitor (C1) between L1 and D1.

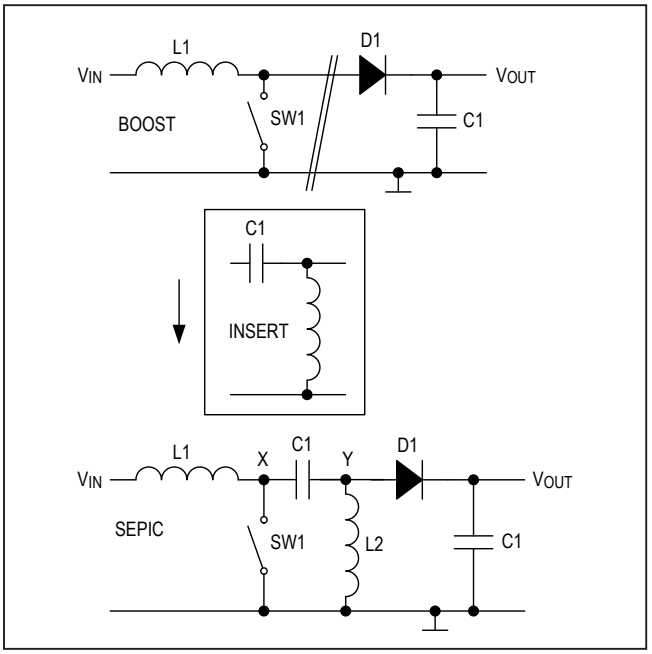

Figure 2. Boost to SEPIC transformation.

This capacitor (C1) prevents any DC component from input to output. However, D1's anode must connect to a known potential in order to operate. This is created by connecting D1's anode to ground through an inductor (L2).

SEPIC Operation

It is known that the average voltage across any inductor is zero. This principle can be used for inductors L1 and L2 of the SEPIC configuration to evaluate the magnitude of the steady-state DC voltage present across the coupling capacitor C1. From Figure 2 we can see that one end of inductor L1 is connected to input voltage V_{IN} while the other end is connected to the junction X, which consists of a switching MOSFET, SW1, and capacitor C1 (i.e., voltage on the drain of the switching MOSFET). The average voltage across L1 can be zero only when the average voltage at this junction X is equal to V_{IN}. Similarly, one end of inductor L2 is connected to ground (GND) while the other end is connected to junction Y, which consists of capacitor C1 and diode D1. The average voltage across L2 can be zero only when the average voltage at junction Y is also equal to zero (GND). From this analysis, we can say that the value of DC voltage develop across the coupling capacitor, $V_{C1(AVG)}$, is:

$$V_{C1(AVG)} = V_X - V_Y$$

$$V_{C1(AVG)} = V_{IN} - GND$$

$$V_{C1(AVG)} = +V_{IN}$$

In the light of above discussion, we can conclude that under steady-state condition coupling capacitor C1 develops an average voltage equal to input voltage V_{IN} across it. Therefore, for any SEPIC design the series coupling capacitor must have a voltage rating to endure the maximum input voltage. A SEPIC is said to be operating in continuous-conduction mode (CCM) if the current through the inductor L1 never falls to zero. In this document, we discuss only the CCM operation of SEPIC converter. Next, we will discuss how the SEPIC circuit behaves during the switching period on- and off-times.

When Switch is On

When the switch is closed (on), the magnetic energy stored in both inductors (L1 and L2) increases. The input

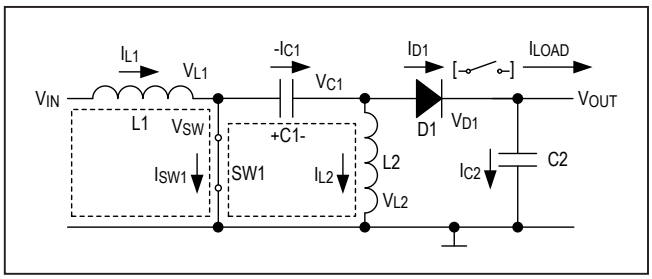

Figure 3. SEPIC topology when the switch closes.

current (I_{IN}) builds up a field in L1. Capacitor C1 discharges, building up a field in L2. The diode is reverse-biased as shown in Figure 3, so only output capacitor C2 supplies current to the load.

The voltage expression for the input voltage loop can be written as follows:

$$V_{IN} = V_{L1} + V_{SW}$$

as V_{SW} = 0 (assuming negligible switch voltage drop).

$$V_{L1} = +V_{IN}$$

Similarly, the voltage expression for the middle loop can be written as:

$$V_{SW} = V_{C1} + V_{L2}$$

$$V_{C1} + V_{L2} = 0$$

$$V_{C1} = -V_{L2}$$

It is evaluated already that average voltage across coupling capacitor C1 is equal to input voltage. Substituting this in the above expression yields the voltage across inductor L2 during the on-time of the switch.

$$V_{L2} = -V_{IN}$$

Thus, during the on-time the voltage across the inductor L1 is equal to the input voltage, V_{IN} whereas, the voltage across the inductor L2 is $-V_{IN}$. The current in L1 has a slope of $+V_{IN}/L1$ while the current in L2 has a slope of $-V_{IN}/L2$. Finally, as the switch is on, therefore, the drain voltage V_D of the switching MOSFET is at 0V.

$$V_D = 0V$$

Current flow in different nodes of the circuit can be evaluated using KCL expressions as shown below:

$$I_{L1} - I_{SW1} - I_{C1} = 0$$

Rearranging the above expression yields the current in inductor L1 as follows:

$$I_{L1} = I_{SW1} + I_{C1}$$

As the diode is reverse-biased, therefore, the current in series capacitor can be written as:

$$I_{C1} = -I_{L2}$$

$$I_{D1} = 0 \text{ (diode reverse-biased)}$$

The output capacitor C2 provides current to the load.

$$I_{LOAD} = I_{C2}$$

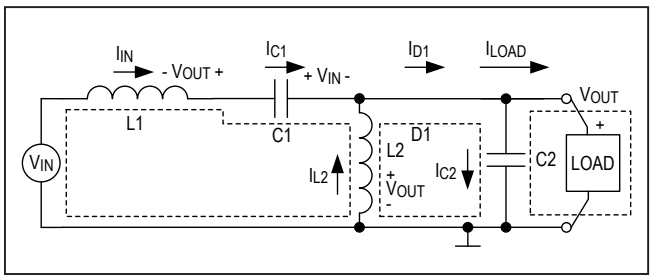

Figure 4. SEPIC topology when the switch opens.

When Switch is Off

When the switch is open (off), the magnetic energy stored in L1 charges C1 and supplies current to the load. The diode is forward biased as shown in Figure 4 and the current from L2 continues in a negative direction and supplies the load. In the off cycle, C1 is charged so that it can recharge L2 during the on cycle.

Input voltage loop expression can be written as follows:

$$V_{L1} + V_{C1} + V_{L2} = V_{IN}$$

Assuming negligible forward voltage drop of the diode, the output voltage V_{OUT} is clamped across L2. Therefore, during the off-time the voltage across L2 can be written as:

$$V_{L2} = V_{OUT}$$

The voltage across inductor L1 can be calculated by substituting values of V_{L2} and V_{C1} in the above expression:

$$V_{L1} = V_{IN} - (V_{IN} + V_{OUT})$$

$$V_{L1} = -V_{OUT}$$

Thus, during the off-time the voltage across the inductor L1 is equal to $-V_{OUT}$, whereas, the voltage across the

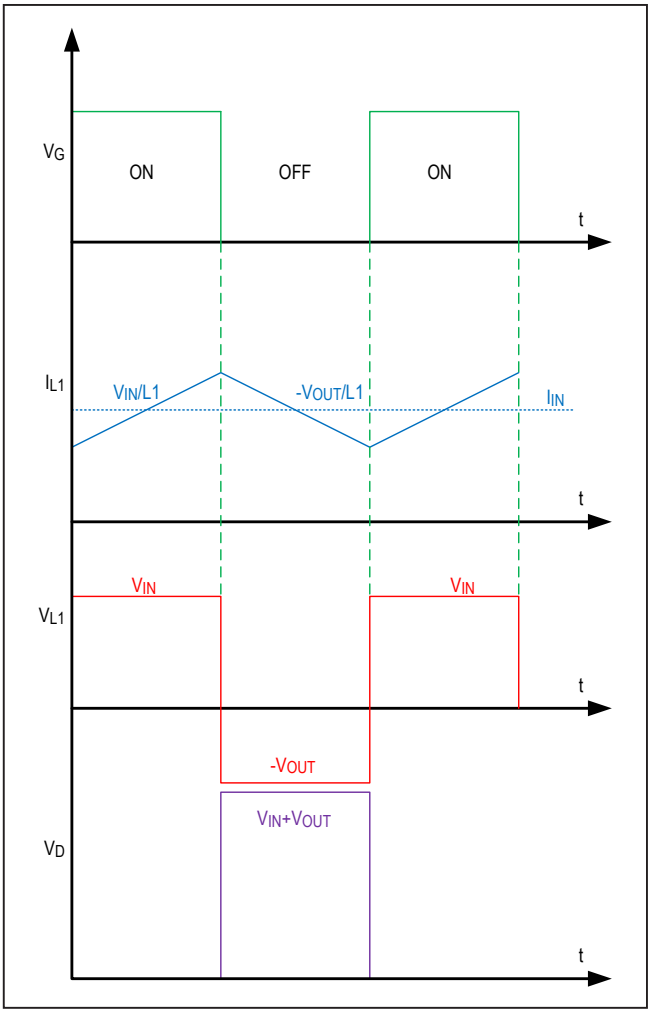

Figure 5. Voltage and current waveforms of inductor L1 in the CCM SEPIC converter.

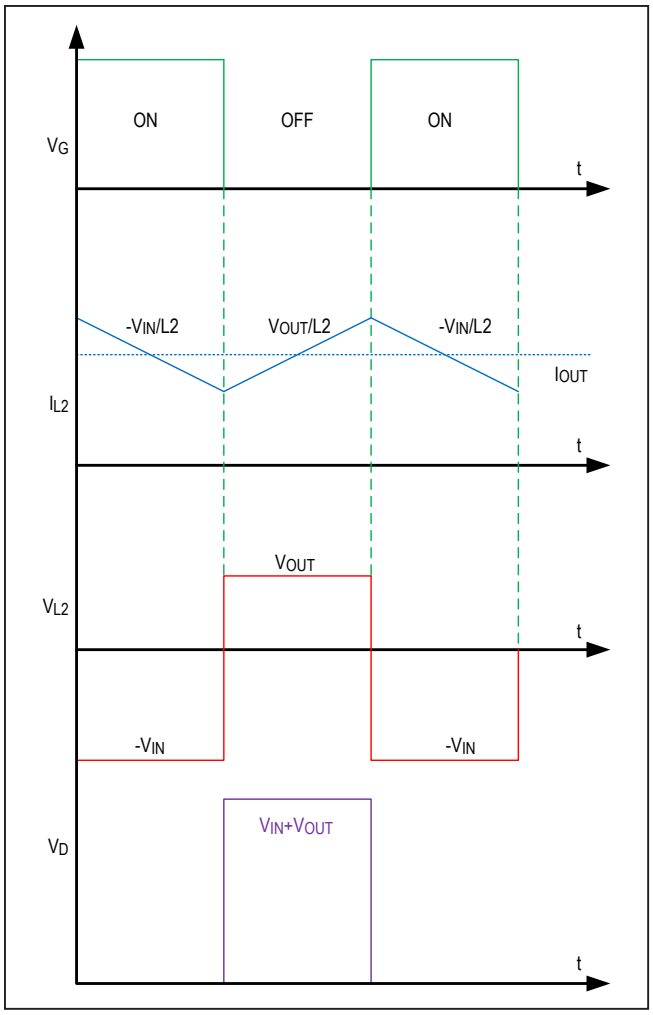

Figure 6. Voltage and current waveforms of inductor L2 in the CCM SEPIC converter.

inductor L2 is V_{OUT}. The current in L1 has a slope of $-V_{OUT}/L1$ while the current in L2 has a slope of $+V_{OUT}/L2$. The MOSFET switch is off and total voltage drop over the drain voltage V_D of the switching MOSFET can be written as follows:

$$V_D = V_{C1} + V_{DIODE} + V_{OUT}$$

Assuming negligible diode drop, the voltage stress on the drain of the MOSFET can be written as:

$$V_D = V_{IN} + V_{OUT}$$

Thus, the selected MOSFET must be able to endure the voltage stress equivalent to sum of input and output voltages.

Current flowing in different nodes of the circuit can be evaluated using the KCL expressions as follows:

$$I_{IN} = I_{C1}$$

$$I_{C1} = I_{D1} - I_{L2}$$

$$I_{D1} = I_{LOAD} + I_{C2}$$

The inductor volt-second balance expressions can be used to evaluate the voltage gain of the SEPIC converter. The volt-second balance can be used either for L1 or L2 and both give the same value of the voltage gain.

For L1 it can be written as:

$$V_{IN} \times t_{ON} = V_{OUT} \times t_{OFF}$$

$$V_{IN} \times \frac{t_{ON}}{t} = V_{OUT} \times \frac{t_{OFF}}{t}$$

$$V_{IN} \times D = V_{OUT} \times (1 - D)$$

D is the duty cycle of the switching period.

$$\frac{V_{OUT}}{V_{IN}} = \frac{D}{1 - D}$$

This is the same voltage gain as a typical buck-boost converter. The SEPIC converter has an advantage of delivering noninverting output to load as compared to conventional buck-boost configuration where output is inverted in polarity. The coupling capacitor C1 also acts as a DC isolation barrier between output and input to protect input circuit components in case of a short-circuited output. SEPIC configuration is very useful in automotive/battery applications where output voltage requirements can be less than, greater than, or equal to the input voltage of the battery.

Design Procedure for SEPIC Converter Design Using MAX16990

Now that the basic principle of operation of the SEPIC is understood, a practical design can be illustrated. This document is primarily concerned with the design of the power stage and the feedback loop, and is intended to complement the information contained in the MAX16990 data sheet. For details on how to set up supervisory and protection functions of the controller, refer to the IC data sheet. All expressions used in design calculation are based on Maxim **Application Note 5740**.

The switching frequency is determined by the operating range of the controller used in our design. The MAX16990 has a 100kHz to 1MHz frequency range. For this design, we have selected a switching frequency of 500kHz, so:

$$f_{SW} = 500kHz$$

As the power supply is configurable to provide either a +24V or +5V output, therefore, in order to ensure a compact design both inductors (primary inductor L_P and secondary inductor L_S), series capacitor (C_S), and MOSFET specifications are selected to fulfill both the output options. The design is optimized for 24V output, therefore, 5V output is not as efficient as 24V; however, it provides dual-output options in a space-constrained, compact design with simple configuration options to change the output voltage into two possible values.

Step 1: Calculations of Inductor Current Range

Suppose initial design efficiency of 85% and calculate the input current range that is equivalent to the primary inductor current operating range. The minimum average inductor current can be calculated as follows:

$$I_{INAVG\_MIN} = I_{LPAVG\_MIN} = \frac{V_{OUT} \times I_{OUTMIN}}{V_{INMAX} \times \eta}$$

For 24V output:

$$I_{INAVG\_MIN} = I_{LPAVG\_MIN} = \frac{24 \times 0.35}{32 \times 0.85} = 0.3088A$$

For 5V output:

$$I_{INAVG\_MIN} = I_{LPAVG\_MIN} = \frac{5 \times 0.35}{32 \times 0.85} = 0.06433A$$

Similarly, the maximum average inductor current can be calculated as follows:

$$I_{INAVG\_MAX} = I_{LPAVG\_MAX} = \frac{V_{OUT} \times I_{OUTMAX}}{V_{INMIN} \times \eta}$$

For 24V output:

$$I_{INAVG\_MAX} = I_{LPAVG\_MAX} = \frac{24 \times 0.9}{18 \times 0.85} = 1.4117A$$

For 5V output:

$$I_{INAVG\_MAX} = I_{LPAVG\_MAX} = \frac{5 \times 0.9}{18 \times 0.85} = 0.294A$$

The secondary inductor's average current range is equal to the minimum and maximum output current:

For both 24V and 5V outputs:

$$I_{LSAVG\_MIN} = I_{OUTMIN} = 0.35A$$

$$I_{LSAVG\_MAX} = I_{OUTMAX} = 0.9A$$

Step 2: MOSFET and Diode Selection

The next step is to calculate the duty-cycle range. However, to do this we need to choose the external MOSFET. This selection requires MOSFET's rating calculations. The peak drain current that flows into the MOSFET is the average peak inductor current plus the inductor current ripple $\Delta I_{L/2}$.

Assuming a maximum LIR of 0.5 when the input and output currents are at their maximum, then:

$$I_{INMOS\_PK(EST)} = (I_{INAVG\_MAX} + I_{OUTMAX}) \times \left(1 + \frac{LIR}{2}\right)$$

For 24V output:

$$I_{INMOS\_PK(EST)} = (1.4117 + 0.9) \times \left(1 + \frac{0.5}{2}\right) = 2.889A$$

For 5V output:

$$I_{INMOS\_PK(EST)} = (0.294 + 0.9) \times \left(1 + \frac{0.5}{2}\right) = 1.492A$$

Because we must select one MOSFET for both output options, therefore, we select:

$$I_{NMOS\_PK(EST)} = 2.889A$$

The maximum reverse voltage rating of the output diode can be calculated as follows:

$$V_{DMAX} = V_{INMAX} + V_{OUTMAX}$$

For both 24V and 5V outputs:

$$V_{DMAX} = 32 + 24 = 56V$$

A 60V 5A Schottky diode (STMicroelectronics STPS5L60) is selected. The forward voltage drop V_D of this diode is approximately 0.5V.

The maximum voltage stress on the MOSFET can be calculated as follows:

$$V_{DSMAX} = V_{INMAX} + V_{OUTMAX} + V_D$$

For both 24V and 5V outputs:

$$V_{DSMAX} = 32 + 24 + 0.5 = 56.5V$$

Based on this information, a Fairchild FDS5670 nMOS rated for a drain current of 10A is selected. The typical $R_{DS(ON)}$ of this transistor is 15mΩ with a V_{GS} = 5V, which is the drain-source voltage provided by the MAX16990. The rated drain-source voltage for this device is 60V, which is higher than the maximum drain-source voltage calculated by the V_{DMAX} expression.

Step 3: Duty-Cycle Range Calculation

Next, we evaluate the duty-cycle range to calculate D_{MIN} and D_{MAX} at which the regulator operates. This can be determined with the following two equations:

$$D_{MIN} = \frac{V_{OUT} + V_D}{V_{INMAX} + V_{OUT} + V_D - \left[\begin{matrix}(R_{DS(ON)} + R_{SENSE}) \\ \times (I_{INAVG\_MIN} + I_{OUTMIN})\end{matrix}\right]}$$

$$D_{MAX} = \frac{V_{OUT} + V_D}{V_{INMIN} + V_{OUT} + V_D - \left[\begin{matrix}(R_{DS(ON)} + R_{SENSE}) \\ \times (I_{INAVG\_MAX} + I_{OUTMAX})\end{matrix}\right]}$$

V_D is the forward voltage of the rectifier diode.

$R_{DS(ON)}$ is the drain-source resistance of the MOSFET.

R_{SENSE} is the sense resistor.

We can ignore R_{SENSE} in the equations for now. We make a more accurate estimate of the duty-cycle range later. This calculation is to ensure that the estimated duty-cycle range is within the specification of the MAX16990 (4% to 93%).

For 24V output:

$$D_{MIN} = \frac{24 + 0.5}{32 + 24 + 0.5 - \left[(15m + 0) \times (0.3088 + .35)\right]} = 0.433$$

$$D_{MAX} = \frac{24 + 0.5}{18 + 24 + 0.5 - \left[(15m + 0) \times (1.4117 + 0.9)\right]} = 0.576$$

This means that for the 24V output, we would require slope compensation as the maximum duty cycle is approximately 58%.

For 5V output:

$$D_{MIN} = \frac{5 + 0.5}{32 + 5 + 0.5 - \left[(15m + 0) \times (0.3088 + .35)\right]} = 0.146$$

$$D_{MAX} = \frac{5 + 0.5}{18 + 5 + 0.5 - \left[(15m + 0) \times (1.4117 + 0.9)\right]} = 0.234$$

This means that for the 5V output, we would not require slope compensation as the maximum duty cycle is approximately 24%.

The maximum duty cycle of the MAX16990 is 93%, therefore, we have proved that for our design the device operates within its specified duty-cycle range for both the possible output voltages. This ensures continuous-conduction mode (CCM) operation of the device.

Step 4: Inductors Selection

The minimum required values for primary inductor L_P and secondary inductor L_S can be calculated form the expressions below:

$$L_P \geq \frac{(V_{OUT} + V_D) \times (1 - D_{MIN})}{2 \times f_{SW} \times I_{INAVG\_MIN}}$$

$$L_S \geq \frac{(V_{OUT} + V_D) \times (1 - D_{MIN})}{2 \times f_{SW} \times I_{OUT\_MIN}}$$

For 24V output:

$$L_P \geq \frac{(24 + 0.5) \times (1 - 0.433)}{2 \times 500k \times 0.3088} = 44.98\mu H$$

$$L_S \geq \frac{(24 + 0.5) \times (1 - 0.433)}{2 \times 500k \times 0.35} = 39.69\mu H$$

For 5V output:

$$L_P \geq \frac{(5 + 0.5) \times (1 - 0.146)}{2 \times 500k \times 0.06433} = 73\mu H$$

$$L_S \geq \frac{(5 + 0.5) \times (1 - 0.146)}{2 \times 500k \times 0.35} = 13.4\mu H$$

We must select a commercial value that is always higher than the critical inductance. In this way, we guarantee continuous-conduction mode (CCM) operation throughout the application range. To ensure both 24V and 5V output operation, we select the following values for L_P and L_S:

$$L_P = 82\mu H$$

$$L_S = 47\mu H$$

Inductor ripple current ratio is another parameter to remember when choosing proper inductors. It is defined as the ratio of the peak-to-peak inductor current and the average input current:

$$LIR = \frac{I_{L\_PK-PK}}{I_{L\_AVG}}$$

The relationship between the inductors (L_P and L_S) and the LIR is shown in the following equations:

$$LIR_{LP} = \frac{(V_{OUT} + V_D) \times (1 - D_{MAX})}{L_P \times f_{SW} \times I_{INAVG\_MAX}}$$

$$LIR_{LS} = \frac{(V_{OUT} + V_D) \times (1 - D_{MAX})}{L_S \times f_{SW} \times I_{OUT\_MAX}}$$

For 24V output:

$$LIR_{LP} = \frac{(24 + 0.5) \times (1 - 0.576)}{82\mu \times 500k \times 1.4117} = 0.18$$

$$LIR_{LS} = \frac{(24 + 0.5) \times (1 - 0.576)}{47\mu \times 500k \times 0.9} = 0.4925$$

For 5V output:

$$LIR_{LP} = \frac{(5 + 0.5) \times (1 - 0.234)}{82\mu \times 500k \times 0.294} = 0.349$$

$$LIR_{LS} = \frac{(5 + 0.5) \times (1 - 0.234)}{47\mu \times 500k \times 0.9} = 0.199$$

This results in inductors and MOSFET peak currents of:

$$I_{LP\_PK} = I_{INAVG\_MAX} \times \left[1 + \frac{LIR_{LP}}{2}\right]$$

$$I_{LS\_PK} = I_{OUT\_MAX} \times \left[1 + \frac{LIR_{LS}}{2}\right]$$

$$I_{MOSFET\_PK} = I_{LP\_PK} + I_{LS\_PK}$$

For 24V output:

$$I_{LP\_PK} = 1.4117 \times \left[1 + \frac{0.18}{2}\right] = 1.538A$$

$$I_{LS\_PK} = 0.9 \times \left[1 + \frac{0.4925}{2}\right] = 1.12A$$

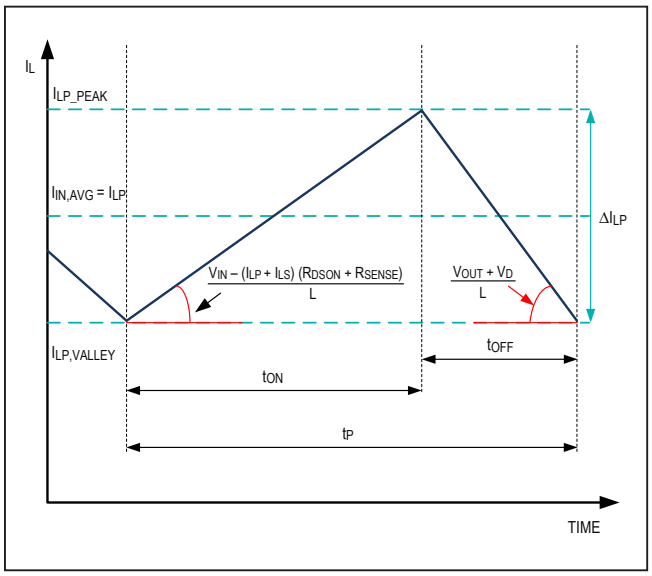

Figure 7. Inductor current of primary inductor.

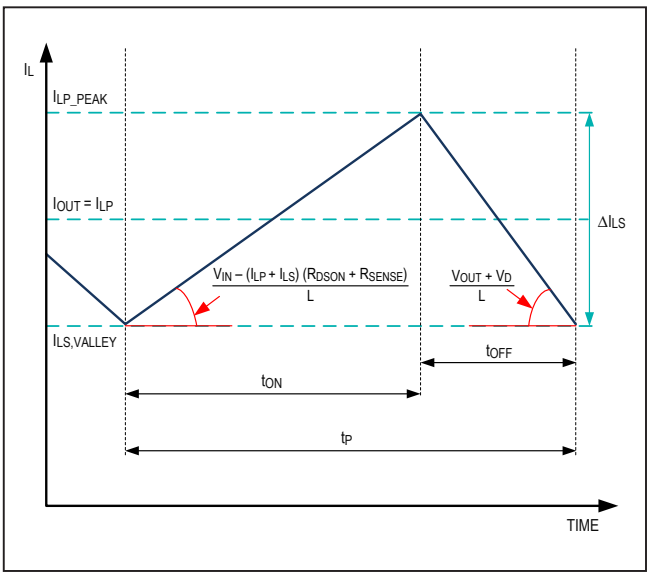

Figure 8. Inductor current of secondary inductor.

For 5V output:

$$I_{LP\_PK} = 0.294 \times \left[1 + \frac{0.349}{2}\right] = 0.345A$$

$$I_{LS\_PK} = 0.9 \times \left[1 + \frac{0.199}{2}\right] = 0.989A$$

Based on this information, a Würth Elektronik 82µH inductor 744770182 is selected for L_P (I_R = 2.25A, I_{SAT} = 2.45A). Similarly, a Würth Elektronik 47µH inductor 7447714470 is selected for L_S (I_R = 2.2A, I_{SAT} = 2.5A).

In the light of above discussion, the actual peak current flows in the MOSFET can be calculated as follows:

$$I_{MOSFET\_PK} = I_{LP\_PK} + I_{LS\_PK}$$

For 24V output:

$$I_{MOSFET\_PK} = 1.538 + 1.12 = 2.658A$$

For 5V output:

$$I_{MOSFET\_PK} = 0.435 + 0.989 = 1.334A$$

Because we are using the same MOSFET for both output options, we select the peak MOSFET current as:

$$I_{MOSFET\_PK} = 2.658A$$

Step 5: Series Capacitor Selection

The series capacitor is charged at a DC voltage equal to the input voltage. It must carry the primary inductor current during the off-time and the secondary inductor current during the on-time. This makes this capacitor selection challenging, even somewhat tricky.

As the first requirement, the voltage rating of the series capacitor must be higher than the maximum input voltage (V_{INMAX}).

The RMS current flowing through the capacitor is given by the following equation:

$$I_{CS\_RMS} = I_{OUTMAX} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

For 24V output:

$$I_{CS\_RMS} = 0.9 \times \sqrt{\frac{0.576}{1 - 0.576}} = 1.05A$$

For 5V output:

$$I_{CS\_RMS} = 0.9 \times \sqrt{\frac{0.234}{1 - 0.234}} = 0.497A$$

Because we are using the same C_S for both possible outputs, the selected series capacitor must be rated for 1.05A RMS current.

The ripple across the series capacitor is determined by the capacitor value and its equivalent series resistance (ESR). Assuming a 1% voltage ripple across the series capacitor due to the ESR, the series capacitor ESR must be lower than:

$$ESR_{CS} < MIN\left[\frac{0.01\times V_{INMIN}}{I_{LP\_PK}}, \frac{0.01\times V_{INMIN}}{I_{LS\_PK}}\right]$$

For 24V output:

$$ESR_{CS} < MIN\left[\frac{0.01\times 18}{1.538}, \frac{0.01\times 18}{1.12}\right]$$

Thus, ESR_{CS} < 117mΩ.

For 5V output:

$$ESR_{CS} < MIN\left[\frac{0.01\times 18}{0.345}, \frac{0.01\times 18}{0.989}\right]$$

Thus, ESR_{CS} < 182mΩ.

Because we are using the same C_S for both possible outputs, the selected series capacitor must have an ESR less than 117mΩ.

Finally, the minimum required value of series capacitor can be calculated as follows:

$$C_S > \frac{I_{OUTMAX}\times D_{MAX}}{0.05\times V_{INMIN}\times f_{SW}}$$

For 24V output:

$$C_S > \frac{0.9\times 0.576}{0.05\times 18\times 500k} = 1.2\mu F$$

For 5V output:

$$C_S > \frac{0.9\times 0.234}{0.05\times 18\times 500k} = 0.5\mu F$$

We selected C_S as a 10µF 50V X7R capacitor. This value is high enough to guarantee a low-voltage ripple percentage.

Step 6: Sense Resistors Calculation

Now that the actual peak MOSFET current has been calculated, it is possible to select the sense resistor, R_{SENSE}. The MAX16990 triggers the current limit when the voltage drop on the ISNS pin reaches 212mV (min). This voltage is due to the drop on the sense resistor, R_{SENSE}, and the drop on the slope resistor, R_{SLOPE}, which is used for slope compensation. It is recommended to leave 100mV of headroom for slope compensation. Therefore, R_{SENSE} should generate a voltage drop of 112mV at the current-limit threshold. In the following equation, R_{SENSE} is calculated with a current-limit threshold 20% higher than the peak MOSFET current.

$$R_{SENSE} = \frac{0.112}{1.2\times I_{MOSFET\_PK}}$$

For 24V output:

$$R_{SENSE} = \frac{0.112}{1.2\times 2.658} = 35.1m\Omega$$

For 5V output:

$$R_{SENSE} = \frac{0.112}{1.2\times 1.334} = 69.9m\Omega$$

Typical values for R_{SENSE} selected for 24V and 5V are 39mΩ and 75mΩ, respectively, for this design.

Step 7: Output Capacitor Selection

Selecting the correct output capacitor, C_{OUT}, and its related ESR is very important for minimizing output voltage ripple. Assume that the output voltage ripple is equally distributed between the voltage drop (which is due to the capacitor discharging during off-time) and the ESR voltage drop. The minimum capacitance and the maximum ESR for the output capacitor can be calculated as follows:

$$C_{OUT} > \frac{I_{OUTMAX}\times D_{MAX}}{0.5\times V_{OUT\_RIPPLE}\times f_{SW}}$$

$$ESR < \frac{0.5\times V_{OUT\_RIPPLE}}{I_{LP\_PK} + I_{LS\_PK} - I_{OUTMAX}}$$

For 24V output (assuming static DC ripple allowance of 1%):

$$C_{OUT} > \frac{0.9\times 0.576}{0.5\times(0.01\times 24)\times 500k} = 8.6\mu F$$

$$ESR < \frac{0.5\times(0.01\times 24)}{1.538 + 1.12 - 0.9} = 68m\Omega$$

For 5V output (assuming static DC ripple allowance of 1%):

$$C_{OUT} > \frac{0.9\times 0.234}{0.5\times(0.01\times 5)\times 500k} = 16.85\mu F$$

$$ESR < \frac{0.5\times(0.01\times 5)}{0.345 + 0.989 - 0.9} = 57.4m\Omega$$

Considering DC biasing and other parasitics effects, we selected individual 2 x 10µF 50V X7R capacitors as C_{OUT} for both outputs.

Step 8: Type II Voltage Compensation and Slope Compensation

Using the electronic calculator in **Application Note 5740**, it is now possible to extrapolate the following component values for compensation. The compensation network is designed for worst-case 18V input voltage and 350mA output current.

For 24V output, we obtained a 5.7kHz crossover frequency with a phase margin of approximately 70° by selecting the following components for Type II voltage compensation and slope compensation.

$$R_{SLOPE} = 2.53k\Omega$$
$$C_{COMP} = 10nF$$
$$R_{COMP} = 10k\Omega$$
$$C_{2COMP} = 680pF$$

For 5V output, we obtained a 3.3kHz crossover frequency with a phase margin of approximately 62° by selecting the following components for Type II voltage compensation and slope compensation:

$$R_{SLOPE} = 0\Omega$$
$$C_{COMP} = 33nF$$
$$R_{COMP} = 1.5k\Omega$$
$$C_{2COMP} = 680pF$$

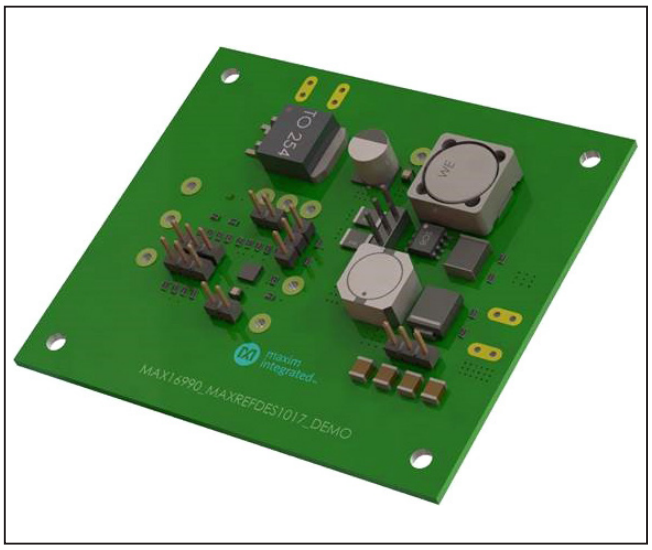

Figure 9. A 3D representation of the MAXREFDES1017 board.

Design Resources

Download the complete set of **Design Resources** including the schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/17	Initial release	—