IEEE 802.3af/at-Compliant, PD Interface with Three Ultra-Small, High-Efficiency, Synchronous DC-DC Buck Converters

MAXREFDES1009

Introduction

Power over Ethernet (PoE) is a technology that allows network cables to deliver power to a powered device (PD) via power-sourcing equipment (PSE) or midspan, and has many advantages over traditional methods of delivering power.

PoE allows power and data to be combined, removing the need for altering the AC mains infrastructure and can be installed by non-electricians. PoE is an intelligent system designed with protection at the forefront, preventing overload, underpowering, and installation errors, while allowing simple scalability and reliability.

High-efficiency, step-down switching regulators minimize power loss with efficiencies greater than 90%, allowing reductions in excessive heat, longer lifetime of ICs, and maximum power available to the PD. Ultra-small packaging, no Schottky diode, and the use of all ceramic capacitors reduce the overall size of the design.

Other features include the following:

- IEEE 802.3af/at Compliance
- 2-Event Classification
- No Schottky-Synchronous Operation for High Efficiency and Reduced Cost
- Internal Compensation and Feedback Divider for 5V Fixed Output Saves Space
- All-Ceramic Capacitors, Ultra-Compact Layout
- Peak Efficiency > 90%
- 3mm × 2mm, 10-Pin TDFN and 5mm × 4.4mm, 14-Pin TSSOP Packages (MAX17502)
- Thermally Enhanced, 3mm × 3mm, 10-Pin TDFN (MAX5969B)

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Hardware Specification

This reference circuit consists of the MAX5969B PD controller and three ultra-small, high-efficiency, synchronous, step-down, DC-DC converters. A 1GbE RJ45 magnetic jack is also included and two diode bridges for separating data and DC power provided by an endspan or midspan PoE system. The MAX17502 features peak-current-mode control with pulse-width modulation (PWM) and operates with fixed switching frequency at any load. The low-resistance, on-chip MOSFETs ensure high efficiency at full load and simplifies layout. There is also a MAX17502 EE-Sim® model available for design and verification. Table 1 shows an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	TYP	MAX
Power Range	P_{IN}	12.95W		25.5W
Undervoltage Lockout Voltage	V_{UVLO}			31.3V
Input Voltage	V_{IN}	37V	48V	57V
Frequency	f_{SW}	560kHz	600kHz	640kHz
12V OUTPUT				
Output Voltage Ripple	ΔV_{OUT}		$72mV_{P-P}$	
Output Current	I_{OUT}			1A
Output Power	P_{OUT}			12W
Peak Duty Cycle	D		25%	
Peak Efficiency	η		96%	
7.5V OUTPUT				
Output Voltage Ripple	ΔV_{OUT}		$72mV_{P-P}$	
Output Current	I_{OUT}			300mA
Output Power	P_{OUT}			2.2W
Peak Duty Cycle	D		15%	
Peak Efficiency	η		81%	
5V OUTPUT				
Output Voltage Ripple	ΔV_{OUT}		$33mV_{P-P}$	
Output Current	I_{OUT}			500mA
Output Power	P_{OUT}			2.5W
Peak Duty Cycle	D		10%	
Peak Efficiency	η		87%	

Designed–Built–Tested

This document describes the hardware shown in Figure 1. It provides a detailed technical guide to designing a complete interface for a PD to comply with the IEEE® 802.3af/at standard in a power-over-Ethernet (PoE+/Type II) Class 4 system and provides a 3-output, non-isolated, ultra-small, high-efficiency, synchronous, step-down DC-DC conversion.

MAX5969B PD Interface

A PoE system delivers power and data to an end device (PD) typically through an RJ45 cable power from an endspan (PSE) (Figure 2) or a midspan (Figure 3). The power is separated from the data through diode bridges to deliver a typical 48V for efficient power transfer, which is low enough to be considered a safe voltage, and removes the need to rewire AC mains and saves cost.

Although this voltage is safe for humans, it still can damage equipment if not properly delivered. This is where MAX5969B classification is required, ensuring the equipment can handle the power delivery. Before the PSE can enable power to a connected IP camera or other PD, it must perform a signature detection.

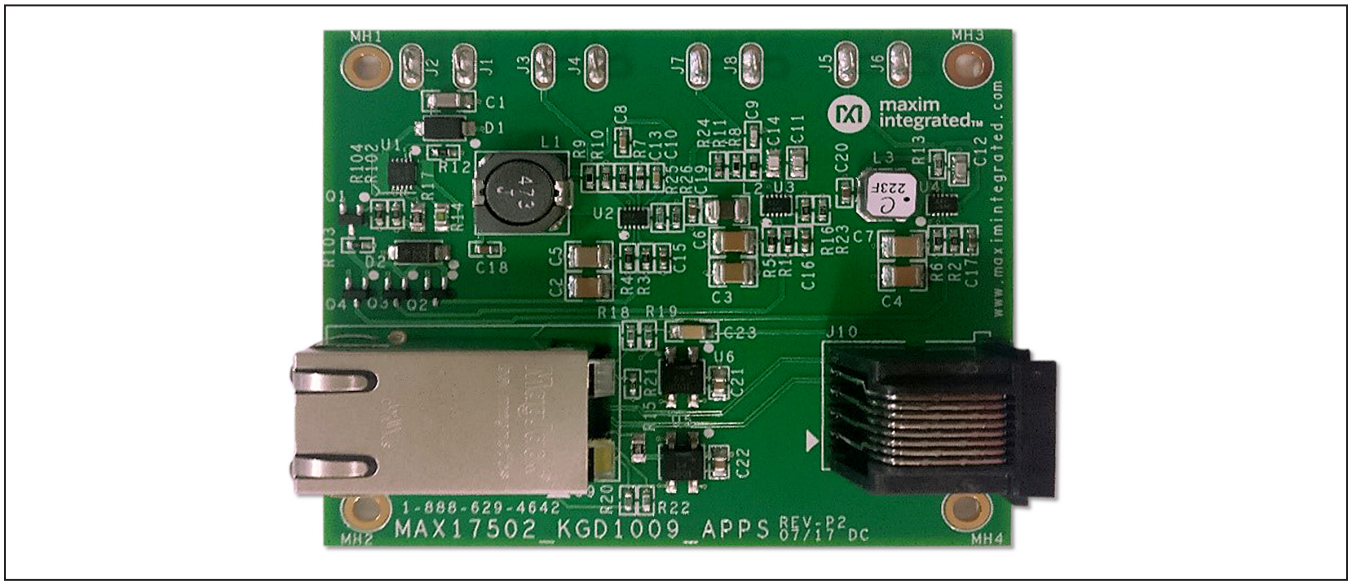

Figure 1. MAXREFDES1009 hardware.

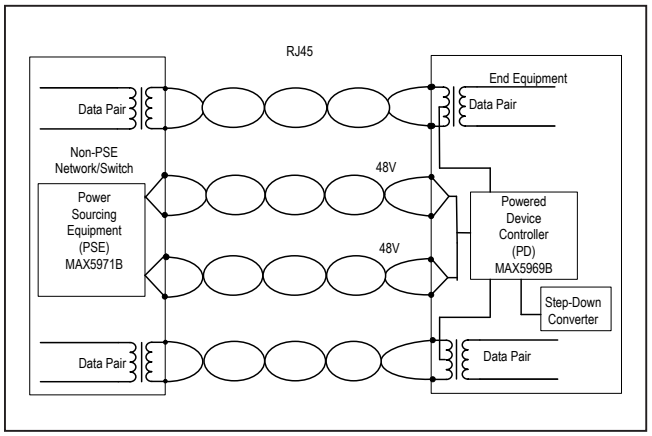

Figure 2. PoE endspan power injector.

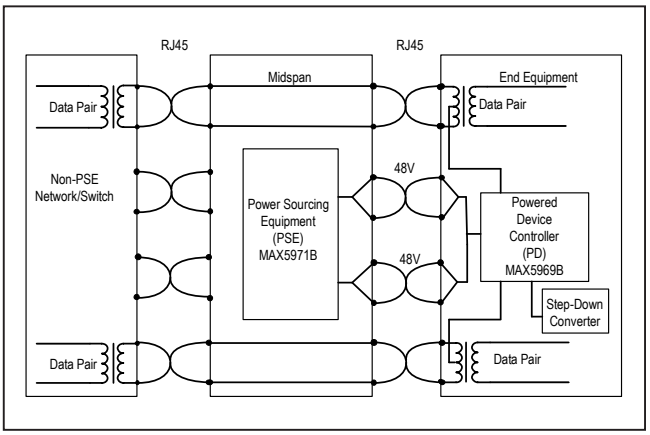

Figure 3. PoE midspan power injector.

Signature Detection

Signature detection uses a lower voltage to detect a characteristic signature of IEEE-compatible PDs (a 24.9kΩ resistance). See Figure 4. Once this signature has been detected, the PSE knows that higher voltages can be safely applied. The PSE applies two voltages on V_{IN} in the range 1.4V to 10.1V (1V step minimum) and then records the current measurements at the two applied voltages. The PSE then computes the change in current when each voltage was applied (ΔV/ΔI) to ensure the presence of the 24.9kΩ signature resistor.

Classification

In classification mode, the PSE classifies the PD based on the power consumption required. This design is a Class 4 system and uses 2-event classification to efficiently manage power distribution. (The IEEE 802.3af/at standard defines only Class 0 to 4 and Class 5 for any special requirement.)

An external resistor (R_{CLS}) of 30.9Ω connected from CLS to V_{SS} sets the classification current. The PSE determines the class of a PD by applying a voltage at the PD input and measuring the current sourced from the PSE.

When the PSE applies a voltage between 12.6V and 20V, the MAX5969A/MAX5969B exhibit a current of 36.4mA to 43.6mA. The PSE uses the classification current information to classify the power requirement of the PD (MAX5969B).

The classification current includes the current drawn by R_{CLS} and the supply current of the MAX5969A/MAX5969B so the total current drawn by the PD is within the IEEE 802.3af/at standard figures. The classification current is turned off whenever the device is in power mode (Figure 5).

2-Event Classification

During 2-event classification, a Type 2 PSE probes PD for classification twice. In the first classification event, the PSE presents an input voltage between 12.6V and 20V and the MAX5969A/MAX5969B present the programmed load I_{CLASS}. The PSE then drops the probing voltage below the mark event threshold of 10.1V and the MAX5969A/MAX5969B present the mark current (I_{MARK}). This sequence is repeated one more time.

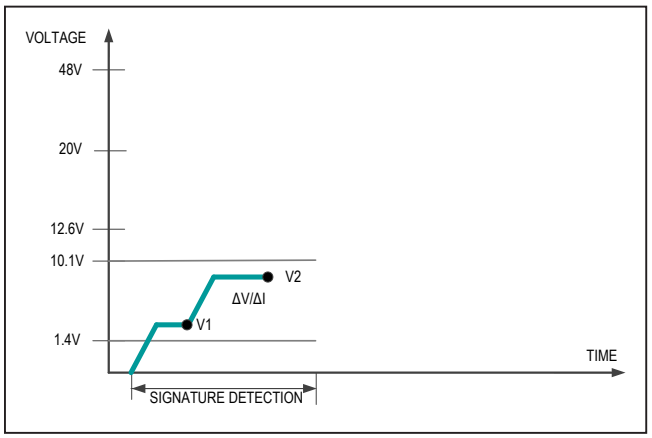

Figure 4. Signature detection.

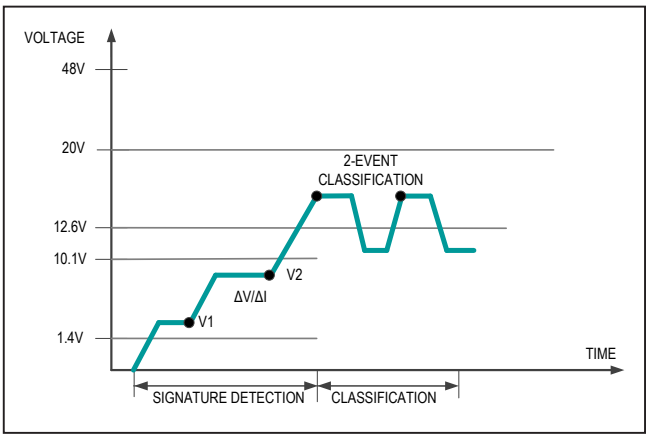

Figure 5. Classification.

Table 2. Setting Classification Current

CLASS	MAXIMUM POWER USED BY PD (W)	R_{CLS} (Ω)	V_{IN}* (V)	CLASS CURRENT SEEN AT V_{IN} (mA)		IEEE 802.3af/at PSE CLASSIFICATION CURRENT SPECIFICATION (mA)	
				MIN	MAX	MIN	MAX
0	0.44 to 12.95	619	12.6 to 20	0	4	0	5
1	0.44 to 3.94	117	12.6 to 20	9	12	8	13
2	3.84 to 6.49	66.5	12.6 to 20	17	20	16	21
3	6.49 to 12.95	43.7	12.6 to 20	26	30	25	31
4	12.95 to 25.5	30.9	12.6 to 20	36	44	35	45
5	> 25.5	21.3	12.6 to 20	52	64	—	—

**V_{IN} is measured across the MAX5969A/MAX5969B input V_{DD} to V_{SS}.*

Power Mode

The final stage after detection and classification of a newly connected PD is to enable power. The 48V supply from the PSE is connected to the PD through the RJ45 cable. Once enabled, the PSE continues to monitor how much current is being delivered to the PD and cuts power to the cable if the power drawn is not within the correct range. This protects the PSE against overload, underpowering and ensuring that the PSE is disconnected from the cable if the PD is unplugged or faulted. See Figure 6.

The MAX5969B enters power mode when V_{IN} rises above the undervoltage lockout threshold (V_{ON}). Note that V_{ON}/V_{OFF} = 38.6V/31V for the MAX5969B. When V_{IN} rises above V_{ON}, the MAX5969B turns on the internal n-channel isolation MOSFET to connect GND to RTN. The open-drain power-good output (PG) remains low for a minimum of t_{DELAY} until the power MOSFET fully turns on to keep the downstream DC-DC converter disabled during inrush. The P_{GOOD} open-drain output is also connected to three small-signal transistors to prevent the DC converters from powering up before the power from the PD is allowable. See Figure 7.

Design Considerations for MAX5969B

Place the input capacitor, classification resistor, and transient voltage suppressor as close as possible to the MAX5969A/MAX5969B. Use large SMT component pads for power dissipating devices such as the MAX5969A/MAX5969B and the external diodes. Use short and wide traces for high-power paths.

The MAX5969B enters undervoltage lockout when the input voltage drops below 31V. When the input drops below this value, the isolation MOSFET switches off, disconnecting the 48V from the buck converters. The MAX5969B exits undervoltage lockout when the input exceeds 38.6V, where the isolation MOSFET switches on again, connecting the MAX17502 converters.

DC Step-Down/Buck Operation

A buck or step-down converter is a DC-to-DC power converter that steps down an input voltage to an output voltage of lower value. We achieve this using a switch and diode to deliver a ratio of the input voltage to an output voltage of lower value while keeping the current constant. When SW1 is closed, D1 is reverse-biased, the input voltage (V_{IN}) is applied across the inductor (L), and current is applied to the load. As the current is passing through the inductor, it stores energy in the form of a magnetic field. See Figure 8.

In the next stage, SW1 is open to disconnect the input voltage, causing a reverse voltage across L since inductors oppose sudden changes in current. This means D1 is now forward-biased, creating a new path for the current to travel. As the magnetic energy stored in the inductor collapses, the currents direction remains the same and uses the new path created by D1 to keep the current through R_{LOAD} consistent. See Figure 9.

High-speed switching of SW1 and SW2 can see some significant spikes and dips on the output voltage so by adding an output capacitor (C_{OUT}) we can smooth out these transitions. Due to the discontinuous nature of the input current waveform, an input capacitor is required to cope with ripple currents noise caused by switching currents, meaning decoupling is essential.

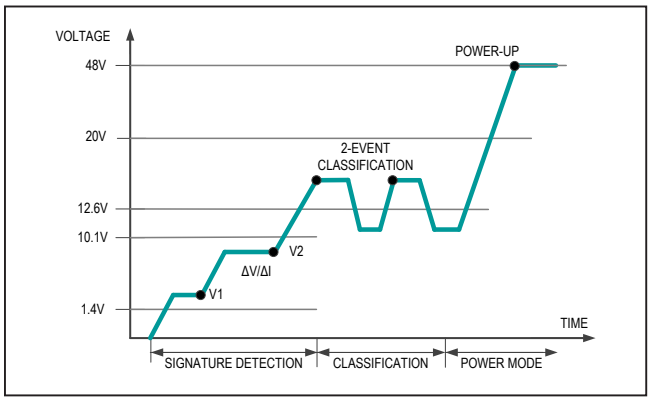

Figure 6. 48V is enabled.

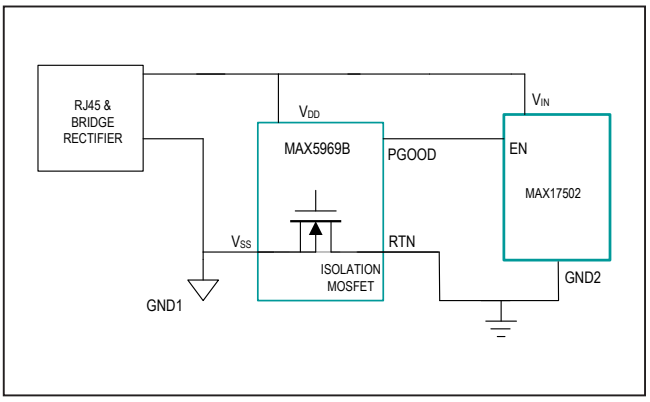

Figure 7. Isolation MOSFET and PGOOD enable the MAX17502.

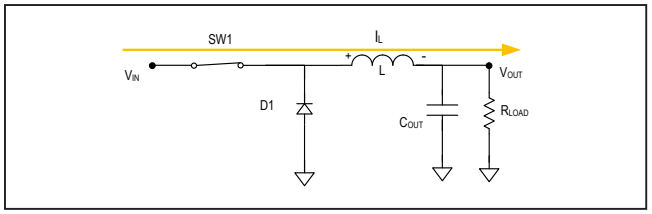

Figure 8. Operation when switch is closed.

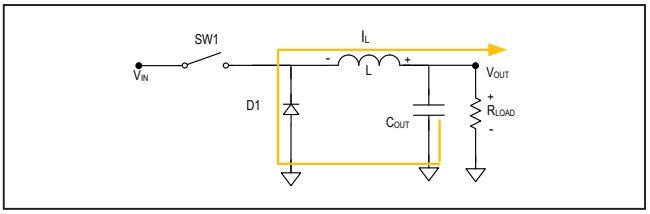

Figure 9. Operation when switch is open.

MAX17502

The MAX17502 buck converter replaces the diode and switch used in the previous example with two integrated MOSFETs that switch the paths for the output synchronously using a PWM signal. Integrating the MOSFETs makes the MAX17502 space effective and simplifies much of the buck converter design.

The MAX17502 uses a peak-current-mode control scheme. An internal transconductance error amplifier generates an integrated error voltage as feedback for the regulator. The error voltage sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator. Refer to the MAX17502 data sheet for the block diagram. At each rising edge of the clock, the high-side p-channel MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected.

During the high-side n-channel MOSFET's on-time, the inductor current ramps up. During the second half of the switching cycle, the high-side MOSFET turns off and the low-side n-channel MOSFET turns on and remains on until either the next rising edge of the clock arrives or sink current peak is detected. The inductor releases the stored energy as its current ramps down, and provides current to the output (the internal low $R_{DS(ON)}$ pMOS/nMOS switches ensure high efficiency at full load).

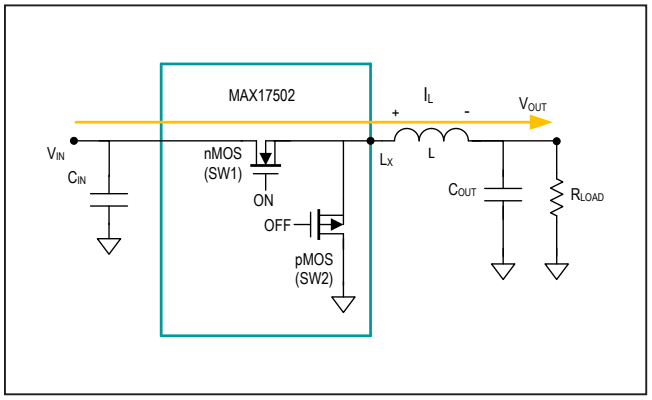

Figure 10. Operation using internal MOSFETs (first stage).

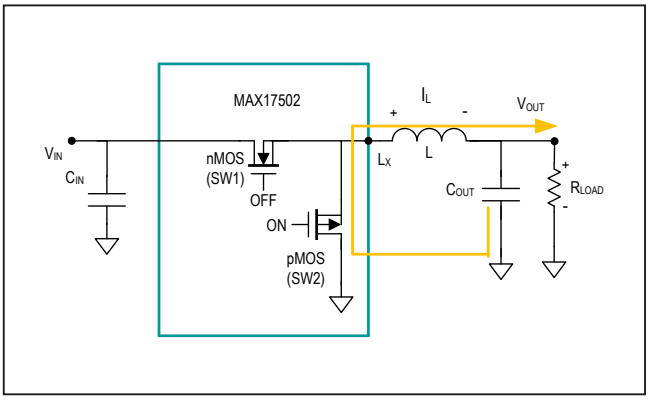

Figure 11. Operation using internal MOSFETs (second stage).

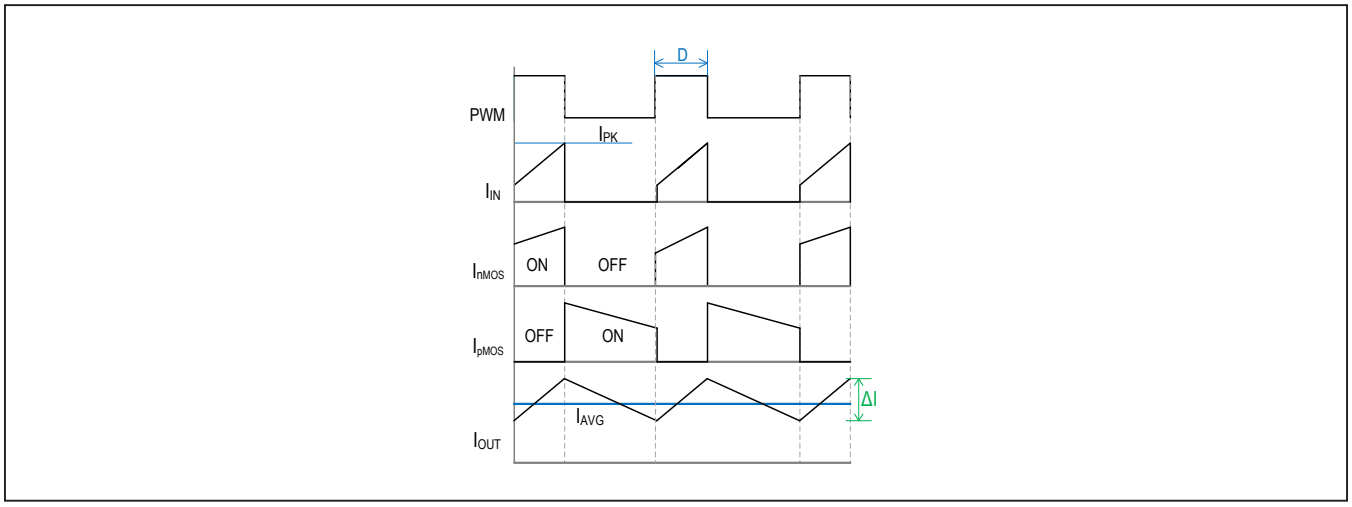

Figure 12. MAX17502 switching waveforms.

Design Procedure for the MAX17502

Calculations in this document use the 12V output as an example using the MAX17502G. The same procedure can be repeated for variable output applications of the MAX17502G/MAX17502H. The 5V output (MAX17502F) is internally compensated and has a fixed output, so it does not require calculating the output voltage or the compensation capacitors and resistor.

The device includes a $\overline{RESET}$ comparator to monitor the output voltage. The open-drain $\overline{RESET}$ output requires an external pullup resistor. $\overline{RESET}$ can sink 2mA of current while low. $\overline{RESET}$ goes high (high impedance) 1024 switching cycles after the regulator output increases above 95.5% of the designated nominal regulated voltage. $\overline{RESET}$ goes low when the regulator output voltage drops to below 92.5% of the nominal regulated voltage. $\overline{RESET}$ also goes low during thermal shutdown. $\overline{RESET}$ is valid when the device is enabled and V_{IN} is above 4.5V.

Step 1: Inductor Selection

Because the MAX17502 has a fixed frequency at any load, the switching frequency (f_{SW}) is already set to 600kHz typical for the MAX17502G/F versions. The duty cycle is also adjusted by error voltage of the PWM comparator, high-side current-sense amplifier, and slope-compensation generator of the IC.

First we calculate the duty cycle. For our calculations we assumed an efficiency of 90%, which is typical for a buck converter.

$$D = \frac{V_{OUT}}{V_{IN}} \times \eta$$

$$D = \frac{12}{48} \times 0.9$$

$$D = 22.5\%$$

Next, we can calculate the inductor value using the formula given in the MAX17502 data sheet.

$$L = \frac{2.4 \times V_{OUT}}{f_{SW}}$$

$$L = \frac{2.4 \times 12}{600k}$$

$$L = 48\mu H$$

The recommended current ripple for the inductor is on average > 20% of the output current. Higher voltages on the input and output increase the ripple value. A smaller inductor gives a higher inductor current ripple, but improves the transient response on the output.

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times D}{f_{SW} \times L}$$

$$\Delta I_L = \frac{(48 - 12) \times 0.25}{600k \times 48\mu}$$

$$\Delta I_L = 312mA$$

It is important to select an inductor with a high saturation current as a saturated core causes the inductance to reduce greatly. For our 1A output, we selected an inductor with a 1.5A saturation current.

Step 2: Setting the Output Voltage

For the MAX17502G, select the parallel combination of R4 and R5, R_P to be less than 15kΩ. For our 12V output we select the parallel combination of R4 and R5, RP to be less than 30kΩ. Once R_P is selected, calculate R4 as:

$$R4 = \frac{R_P \times V_{OUT}}{0.9}$$

$$R4 = \frac{13k \times 12}{0.9}$$

$$R4 = 174k\Omega$$

Calculate R5 as:

$$R5 = \frac{R4 \times 0.9}{(V_{OUT} - 0.9)}$$

$$R5 = \frac{174k \times 0.9}{(12 - 0.9)}$$

$$R5 = 14k\Omega$$

Step 3: Input Capacitor Selection

The minimum input capacitor value for the MAX17502 is a 2.2µF ceramic capacitor. The discontinuous input-current waveform of the buck converter causes large ripple currents in the input capacitor. Higher capacitance values help reduce ripple on the input, so for this design we chose two 10µF ceramic capacitors in parallel. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple that reflects back to the source dictate the capacitance requirement. The device's high switching frequency allows the use of smaller value input capacitors.

X7R capacitors are recommended in industrial applications for their temperature stability. In applications where the source is distanced from the device input, an electrolytic capacitor should be added in parallel to the 2.2µF ceramic capacitor to provide necessary damping for potential oscillations caused by the longer input power path and input ceramic capacitor.

Step 4: Output Capacitor Selection

The output capacitor is usually sized to support a step load of 50% of the maximum output current in the application, so the output-voltage deviation is contained to ±3% of the output-voltage change.

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

where I_{STEP} is the load current step, $t_{RESPONSE}$ is the response time of the controller, and ΔV_{OUT} is the allowable output-voltage deviation.

$$t_{RESPONSE} \cong \frac{0.33}{f_C} + \frac{1}{f_{SW}}$$

$$t_{RESPONSE} = 8.2\mu s$$

f_C is the target closed-loop crossover frequency, and f_{SW} is the switching frequency. Select f_C to be 1/12th of f_{SW}.

$$C_{OUT} = \frac{1}{2} \times \frac{0.5 \times 8.2\mu}{0.2}$$

$$C_{OUT} = 10.25\mu F$$

Consider DC bias and aging effects while selecting the output capacitor. DC bias on a ceramic capacitor has a dramatic effect on the capacitance value. Refer to the capacitor's data sheet for capacitance vs. voltage graphs.

Step 5: Soft-Start Capacitor Selection

The MAX17502 implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to GND programs the soft-start period. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 19 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

$$C_{SS} \geq 2.2nF$$

$$C_{SS} = 6.8nF$$

The soft-start time (t_{SS}) is related to the capacitor connected at the SS pin (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{5.55 \times 10^{-6}}$$

$$t_{SS} = \frac{6.8n}{5.55 \times 10^{-6}}$$

$$t_{SS} = 1.2ms$$

Step 6: External Loop Compensation for Adjustable Output Versions

The MAX17502 uses a peak current-mode control scheme and needs only a simple RC network to have a stable, high-bandwidth control loop for the adjustable output voltage versions. The basic regulator loop is modeled as a power modulator, an output feedback divider, and an error amplifier. The power modulator has DC gain $G_{MOD(dc)}$, with a pole and zero pair. The following equation defines the power modulator DC gain:

$$G_{MOD(dc)} = \frac{2}{\frac{1}{R_{LOAD}} + \frac{0.4}{V_{IN}} + \left(\frac{0.5 - D}{f_{SW} \times L_{SEL}}\right)}$$

where $R_{LOAD} = V_{OUT}/I_{OUT(MAX)}$, f_{SW} is the switching frequency, L_{SEL} is the selected output inductance, D is the duty ratio, $D = V_{OUT}/V_{IN}$.

$$G_{MOD(dc)} = \frac{2}{\frac{1}{12} + \frac{0.4}{48} + \left(\frac{0.5 - 0.225}{600k \times 48\mu}\right)}$$

$$G_{MOD(dc)} = 22$$

Figure 13 shows the compensation network. R_Z can be calculated as:

$$R_Z = 6000 \times f_C \times C_{SEL} \times V_{OUT}$$

$$R_Z = 6000 \times 50k \times 10\mu \times 12$$

$$R_Z = 37.2k\Omega$$

Choose f_C to be 1/12th of the switching frequency.

C_Z can be calculated as follows:

$$C_Z = \frac{C_{SEL} \times G_{MOD(dc)}}{2 \times R_Z}$$

$$C_Z = \frac{10\mu \times 22}{2 \times 37.2k}$$

$$C_Z = 3nF$$

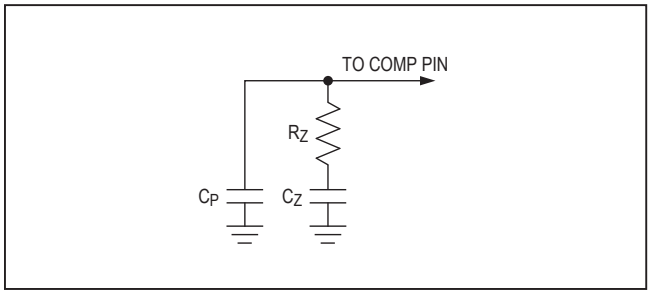

Figure 13. External compensation network.

Step 7: Setting the Undervoltage Threshold

Set the voltage at which the device turns on with a resistive voltage-divider connected from V_{IN} to GND (see Figure 14). Connect the center node of the divider to EN/UVLO. Choose R1 as 3.3MΩ, and then calculate R2 as:

$$R2 = \frac{R1 \times 1.218}{V_{INU} - 1.218}$$

$$R2 = \frac{3.3M \times 1.218}{37 - 1.218}$$

$$R2 = 112k\Omega$$

where V_{INU} is the voltage at which the device is required to turn on. For adjustable output voltage devices, ensure that V_{INU} is higher than 0.8 x V_{OUT}.

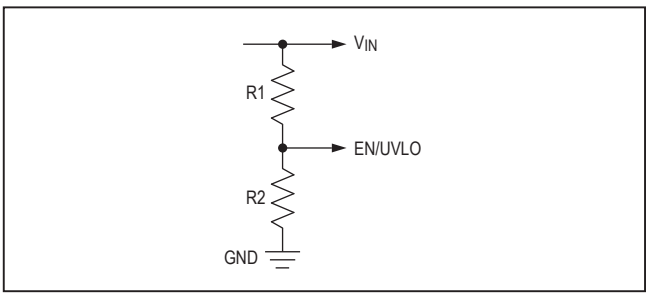

Figure 14. Adjustable EN/UVLO network.

Design Resources

Download the complete set of **Design Resources** including the schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/17	Initial release	—