0.68V Power Supply Using MAX15112 as a Current-Mode Step-Down Regulator

MAXREFDES1006

Introduction

The MAX15112 high-efficiency, current-mode step-down regulator with integrated power switches operates from 2.7V to 5.5V and delivers up to 12A of output current in a small 2mm x 3mm package. The MAX15112 offers excellent efficiency with skip mode capability at light-load conditions, yet provides unmatched efficiency under heavy load conditions. The combination of small size and high efficiency makes this device suitable for both portable and nonportable applications.

The MAX15112 uses a current-mode control architecture with a high-gain transconductance error amplifier, which allows a simple compensation scheme and enables a cycle-by-cycle current limit with fast response to line and load transients. A factory-trimmed switching frequency of 1MHz (PWM operation) allows for a compact, all-ceramic capacitor design.

Integrated switches with low on-resistance ensure high efficiency at heavy loads while minimizing critical inductances.

Other features include the following:

- ±1% Feedback Accuracy Over Load, Line, and Temperature
- Input Undervoltage Lockout
- Programmable Soft-Start
- Adjustable Soft-Start
- External Reference Input
- Selectable Skip Mode Option for Improved Efficiency at Light Loads

Hardware Specification

A current-mode synchronous buck is demonstrated using the MAX15112 for a 0.68V DC output application. The power supply delivers up to 4A at 0.68V. Table 1 shows an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	MAX
Input Voltage	V_{IN}	2.7V	4.5V
Frequency	f_{SW}	1MHz	
Efficiency	η	86%	
Output Voltage	V_{OUT}	0.68V	
Output Voltage Ripple	ΔV_{OUT}	20mV	
Output Current	I_{OUT}	0A	4A
Output Power	P_{OUT}	2.7W	

Designed–Built–Tested

This document describes the hardware shown in Figure 1. It provides a detailed systematic technical guide to designing a synchronous buck using Maxim's MAX15112 current-mode controller. The power supply has been built and tested, details of which follow later in this document.

Figure 1. MAXREFDES1006 hardware.

Note: The MAXREFDES1006 uses the same board and PCB layout as the MAX15112 EV kit (MAX15112EVKIT).

Synchronous Buck

Synchronous buck converters, as opposed to conventional buck converters, can achieve high efficiency in today's low-voltage, high-current applications because they replace the catch diode of buck converters with a MOSFET. As a result, the power they dissipate in the off-period is reduced significantly.

In steady state, the low-side MOSFET is driven such that it is complementary with respect to the high-side MOSFET. This means whenever one of these switches is on, the other is off. In steady-state conditions, this cycle of turning the high-side and low-side MOSFETs on and off complementary to each other regulates V_{OUT} to its set value.

The basic operation of a synchronous buck converter can be explained from the simple circuit diagram shown in Figure 2. The main operation depends on the current in the inductor operated through main switch S1, generally a MOSFET, and the secondary switch S2. Initially when switch S1 is in the on state, the current starts flowing from the source through switch S1, inductor and to the load while the switch S2 is off. The operation time of switch S1 depends on the duty cycle. Now the current through the inductor charges the inductor. During this interval of time when the switch is in on state, switch S2 is in reverse bias and therefore switch S2 does not conduct.

For the next interval of time, when switch S1 is in the off state, the charged energy stored in the inductor now starts discharging. For this discharge of energy, the circuit needs to be closed. Now because the inductor is being discharged, the polarities of the inductor reverses and the switch S2 conducting state becomes forward-biased. When the duty cycle is very low, the inductor's charging time is less when compared to the discharging time. Since switch S2 is in the on state during the discharging time, the secondary switch S2 conducts for a longer time than the main switch.

The synchronous rectifier switch is open when the main switch is closed, and the converse is also true. To prevent cross-conduction (both top and bottom switches are on simultaneously), the switching scheme must be break-before-make. Because of this, a diode is still required to conduct during the interval between the opening of the main switch and the closing of the synchronous-rectifier switch (dead time). When a MOSFET is used as a synchronous switch, the current normally flows in reverse (source to drain), and this allows the integrated body diode to conduct current during the dead time. When the synchronous rectifier switch closes, the current flows through the MOSFET channel. Because of the very low-channel resistance for power MOSFETs, the standard forward drop of the rectifying diode can be reduced to a few millivolts. Synchronous rectification can provide efficiencies well above 90%.

A feature offered in the MAX15112 is skip mode. Skip mode allows the regulator to skip cycles when they are not needed, greatly improving efficiency at light loads.

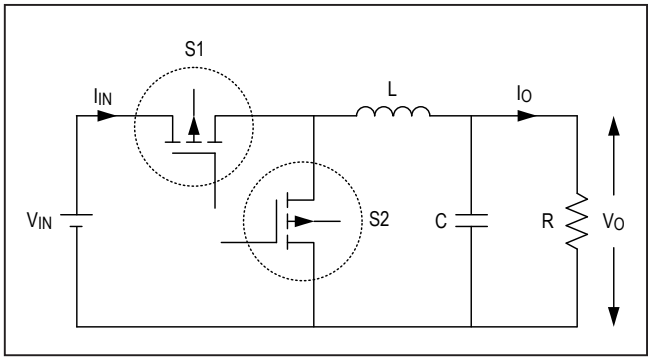

Figure 2. Synchronous converter topology.

Skip mode offers improved light-load efficiencies but at the expense of noise, because the switching frequency is not fixed and is proportional to the load current.

Various waveforms for the synchronous buck topology are shown in Figure 3. During the first cycle when Q1 conducts, the input current gradually rises and flows through the inductor and capacitor. This results in the energy being stored in the inductor and the capacitor.

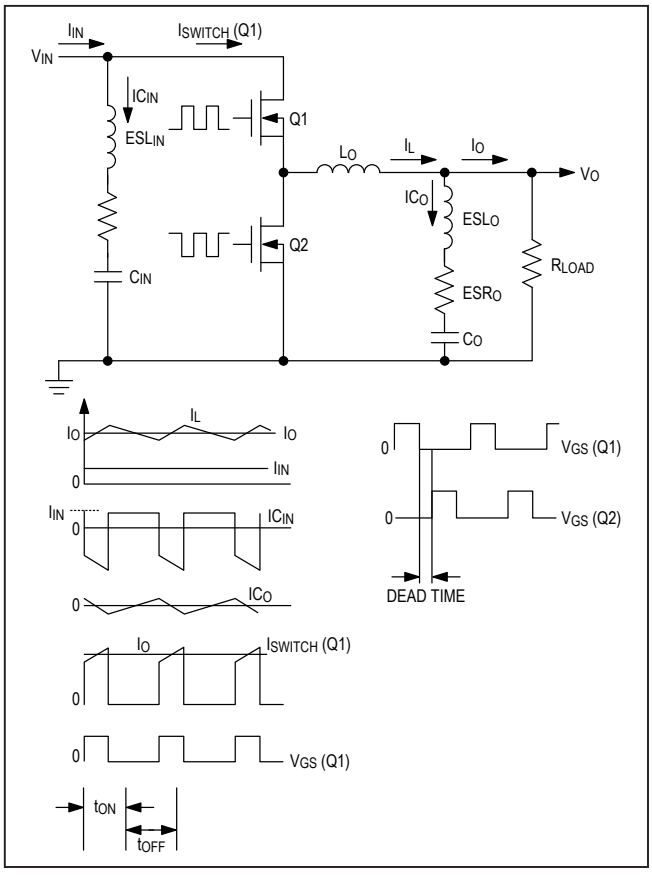

Figure 3. Synchronous buck waveforms.

During the second cycle, Q1 turns off and, after some dead time, Q2 turns on. This results in the energy stored in the magnetic field of the inductor being released back into the circuit. As the energy stored in the inductor decreases, the capacitor starts discharging keeping the current flowing until the next cycle.

An important thing to note is that the MOSFETs Q1 and Q2 cannot be on at the same time as it would result in the input being connected to the ground. Hence, there should be some time interval between the on states of the MOSFETs. This time interval is called the dead time.

Design Procedure

Now that the principle of the synchronous buck operation is understood, a practical design example can be illustrated. The design process can be divided into several stages: output voltage selection, inductor and capacitor selection, and setup of the compensation loop. This document is intended to complement the information contained in the MAX15112 IC data sheet.

The following design parameters are used throughout:

V_{IN} = Input voltage

V_{FB} = Feedback threshold voltage

V_{OUT} = Output voltage

ΔV_{OUT} = Output ripple voltage

I_{OUT} = Output current

η = Target minimum efficiency

P_{IN} = Input power

f_{SW} = Switching frequency

D = Duty cycle

The above symbols are sometimes followed by parentheses to indicate whether minimum or maximum values of the parameters are intended, for example, minimum input voltage is indicated as $V_{IN(MIN)}$. Unless otherwise noted, typical values are intended.

Step 1: Setting the Output Voltage

The MAX15118 output voltage is adjustable from 0.6V to $0.94V_{IN}$ by connecting FB to the center tap of the resistor-divider between the output and the GND. We choose the resistors R_1 and R_2 values so that the DC errors due to the FB input bias current do not affect the output voltage accuracy.

With lower value resistors, the DC error is reduced, but the power consumption increases.

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

Setting V_{OUT} = 0.68V and V_{FB} = 0.6V (typ), we get $\frac{R_1}{R_2} = \frac{2}{15}$ so select R_1 = 360Ω and R_2 = 2.7kΩ.

Step 2: Selecting the Inductor

A high-valued inductor results in reduced inductor-ripple current, leading to a reduced output-ripple voltage. However, a high-valued inductor results in either a larger physical size or a high series resistance (DCR) and a lower saturation current rating.

Typically, we choose an inductor value to produce a current ripple, ΔI_L, equal to 30% of load current giving an LIR of 0.3.

We select the inductor with the following equation:

$$L = \frac{V_{OUT}}{f_{SW} \times LIR \times I_{LOAD}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$L = \frac{0.68}{1Meg \times 0.3 \times 4}\left(1 - \frac{0.68}{3.3}\right) = 0.45\mu H$$

where L = 0.5µH.

Additionally, we need to ensure that the following relationship is satisfied:

$$I_{LPK} = I_{LOAD} + \frac{1}{2}\Delta I_{L(P-P)} < \min\left(18A, I_{LSAT}\right)$$

where:

$$\Delta I_{L(P-P)} = \frac{(V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

$$\Delta I_{L(P-P)} = \frac{(3.3 - 0.68) \times \frac{0.68}{3.3}}{0.5\mu \times 1Meg} = 1.07$$

Hence:

$$I_{L\_PK} = 4 + \frac{1}{2}(1.07) = 4.535$$

Step 3: Selecting the Input Capacitor

For a step-down converter, the input capacitor, C_{IN}, helps to keep the DC input voltage steady despite discontinuous input AC current. Use low-ESR capacitors to minimize the voltage ripple due to ESR.

We calculate C_{IN} using the following formulas:

$$C_{IN} = \left(\frac{I_{LOAD}}{f_{sw} \times \Delta V_{IN_{RIPPLE}}}\right) \times \frac{V_{OUT}}{V_{IN}}$$

$$C_{IN} = \left(\frac{4}{1M \times 0.5}\right) \times \frac{0.68}{3.3} = 1.64\mu F$$

Ensure that the input capacitor can accommodate the input-ripple current requirement imposed by the switching currents.

$$I_{RMS} = \left[\frac{[V_{OUT} \times (V_{IN} - V_{OUT})]^{0.5}}{V_{IN}}\right] \times I_{LOAD}$$

$$I_{RMS} = \left[\frac{0.68 \times (3.3 - 0.68)]^{0.5}}{3.3}\right] \times 4 = 1.33A$$

Step 4: Output Capacitor Selection

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and voltage-rating requirements. These affect the overall stability, output-ripple voltage, and transient response of the DC-DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL.

Estimate the output-voltage ripple due to the output capacitance, ESR, and ESL as follows:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

where:

$$V_{RIPPLE(C)} = \frac{\Delta I_{P-P}}{8 \times C_{OUT} \times f_{SW}}$$

$$V_{RIPPLE(ESR)} = \Delta I_{P-P} \times ESR$$

$$V_{RIPPLE(ESL)} = V_{LX} \times \frac{ESL}{L} = V_{IN} \times \frac{ESL}{L}$$

When using ceramic capacitors, which generally have low-ESR, $\Delta V_{RIPPLE(C)}$ dominates. When using electrolytic capacitors, $\Delta V_{RIPPLE(ESR)}$ dominates. Use ceramic capacitors for low ESR and low ESL at the switching frequency of the converter. The ripple voltage due to ESL is negligible when using ceramic capacitors.

Generally, a smaller inductor-ripple current results in less output-ripple voltage. Since inductor-ripple current depends on the inductor value and input voltage, the output-ripple voltage decreases.

When applying the load, limit the output undershooting by sizing C_{OUT} according to the following formula:

$$C_{OUT} = \frac{\Delta I_{LOAD}}{3 f_{CO} \times \Delta V_{OUT}}$$

where ΔI_{LOAD} is the total load change, f_{CO} is the unity gain bandwidth (or zero-crossing frequency), and ΔV_{OUT} is the desired output undershooting.

$$C_{OUT} = \frac{2}{3 \times 0.1M \times 0.02} = 333\mu F$$

We select C_{OUT} = 400µF. We obtain this value by putting four 100µF capacitors in parallel.

Step 5: Compensation

The MAX15112 uses a fixed-frequency, peak current-mode control scheme to provide easy compensation and fast transient response. The inductor peak current is monitored on a cycle-by-cycle basis and compared to the COMP voltage (output of the voltage error amplifier).

The regulator's duty cycle is modulated based on the inductor's peak current value. This cycle-by-cycle control of the inductor current emulates a controlled current source.

As a result, the inductor's pole frequency is shifted beyond the gain bandwidth of the regulator.

System stability is provided with the addition of a simple series capacitor-resistor from COMP to GND. This pole-zero combination serves to tailor the desired response of the closed-loop system.

The peak current-mode controller's modulator gain is attenuated by the equivalent divider ratio of the load resistance and the current-loop gain. G_{MOD} is the power modulator's transconductance, and R_{LOAD} is the equivalent load resistance value.

K_S is the slope compensation factor calculated as:

$$K_S = 1 + \frac{V_{SLOPE} \times f_{SW} \times L \times g_{MC}}{V_{IN} - V_{OUT}}$$

where V_{SLOPE} = 130mV and g_{MC} = 80AV^{-1}.

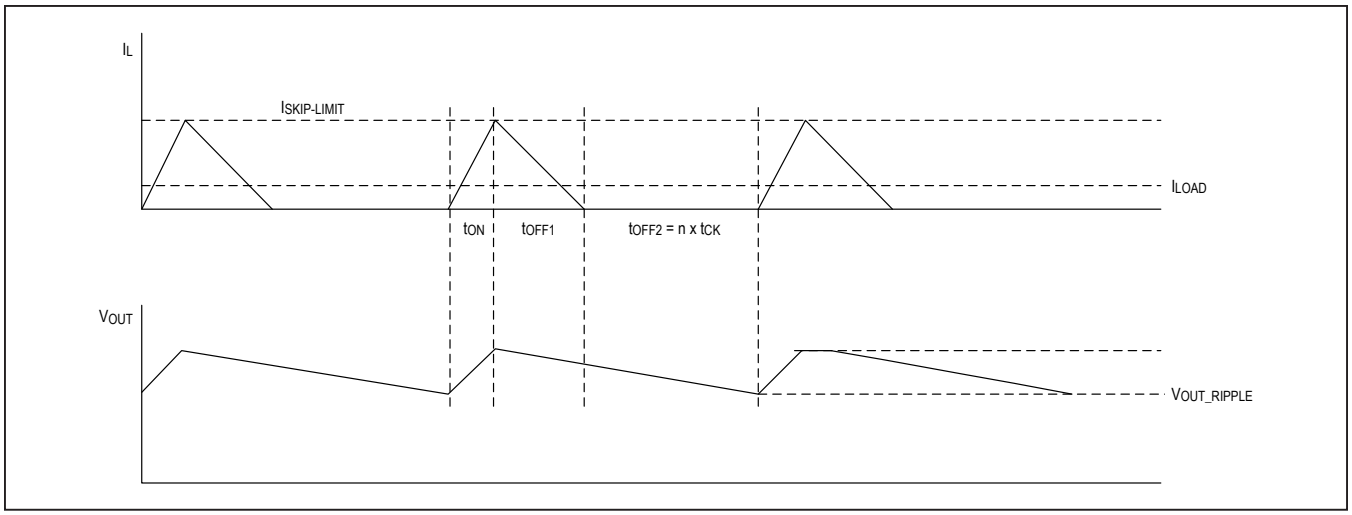

Figure 4. Skip mode waveform.

Hence:

$$K_S = 1 + \frac{0.13 \times 1Meg \times 0.5\mu H \times 80}{3.3 - 0.68} = 2.98$$

G_{MOD} becomes:

$$G_{MOD} = g_{MC} \times \frac{1}{1 + \frac{R_{LOAD}}{f_{SW} \times L} \times \left[K_S \times (1 - D) - 0.5\right]}$$

where:

$$R_{LOAD} = \frac{V_{OUT}}{I_{OUT(MAX)}} = \frac{0.68}{4} = 0.17\Omega$$

hence, G_{MOD} =

$$80 \times \frac{1}{1 + \frac{0.17}{1M \times 0.5\mu} \times \left[2.98 \times \left(1 - \frac{0.68}{3.3}\right) - 0.5\right]}$$

$$G_{MOD} = 48.94$$

Select the desired crossover frequency. Choose f_{CO} equal to 1/10th of f_{SW}, or f_{CO} at 100kHz.

Select R_C using the transfer-loop's fourth asymptote gain equal to unity, assuming $f_{CO} > f_{P1}$, f_{P2}, and f_{Z1}, R_C becomes:

$$R_C = \frac{R_1 + R_2}{R2} \times \frac{\left(1 + \frac{R_{LOAD} \times K_S\left[(1 - D) - 0.5\right]}{L \times f_{SW}}\right)}{g_M \times g_{MC} \times R_{LOAD}}$$

$$\times 2\pi \times f_{CO} \times C_{OUT}$$

$$\times \left[ESR + \frac{1}{\frac{1}{R_{LOAD}} + \frac{K_S\left[(1 - D) - 0.5\right]}{L \times f_{SW}}}\right]$$

$$g_M = 1.1mS, g_{MC} = 80AV^{-1}$$

and

$$V_{SLOPE} = 130mV$$

where:

$$R_{LOAD} = \frac{V_{OUT}}{I_{OUT(MAX)}} = \frac{0.68}{4} = 0.17\Omega$$

K_S is the slope compensation factor calculated as:

$$K_S = 1 + \frac{V_{SLOPE} \times f_{SW} \times L \times g_{MC}}{V_{IN} - V_{OUT}} = 2.98$$

Hence, R_C becomes:

$$R_C = \frac{360 + 2700}{2700}$$

$$\times \frac{\left(1 + \frac{0.17 \times 2.98\left[(1 - 0.206) - 0.5\right]}{0.5\mu \times 1Meg}\right)}{0.0011 \times 80 \times 0.17} \times 2\pi \times 100k \times 400\mu$$

$$\times \left[0.005 + \frac{1}{\frac{1}{0.17} + \frac{2.98\left[(1 - 0.206) - 0.5\right]}{0.5\mu \times 1M}}\right] = 873\Omega$$

$$R_C = 873\Omega$$

Selecting R_C = 910Ω.

Step 6: Selecting C_C

C_C is determined by selecting the desired first system zero, f_{Z1}, based on the desired phase margin. Typically, setting f_{Z1} below 1/5th of f_{CO} provides sufficient phase margin.

$$C_C \geq \frac{5}{2 \times \pi \times f_{CO} \times R_C}$$

$$C_C \geq \frac{5}{2 \times \pi \times 100k \times 910} \gg 8.74nF$$

Selecting C_C = 82nF.

Step 7: Setting the Soft-Start Time

The soft-start feature ramps up the output voltage slowly, reducing input inrush current during startup. The device utilizes an adjustable soft-start function to limit inrush current during startup. The soft-start time is adjusted by the value of C_{16}, the external capacitor from SS/REFIN to GND.

For a desired 6ms soft-start time, we calculate C_{16} as:

$$C_{16} = \frac{(10\mu A \times t_{SS})}{0.6V}$$

$$C_{16} = \frac{(10\mu A \times 0.006)}{0.6V} = 0.1\mu F$$

The resistor, in series with the soft-start capacitor (R_{14} or R_{SS}), improves load regulation. The recommended value for R_{SS} is approximately 330Ω. R_{SS} is needed to ensure that, during hiccup period, R_{SS} can be pulled down internally.

We select $R_{14} = R_{SS}$ = 470Ω.

Design Resources

Download the complete set of **Design Resources** including the schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/17	Initial release	—
1	1/18	Added note to Figure 1 that the MAXREFDES1006 uses the same board and PCB layout as the MAX15112 EV kit.	—