

Circuits from the Lab
Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0412.

Devices Connected/Referenced	
ADRV9361-Z7035	2 Rx, 2 Tx RF System-On-Module
ADRV1CRR-BOB	Breakout Carrier Board for the ADRV9361-Z7035
ADIS16460	Inertial Measurement Unit

ADRV-PACKRF Robust Portable Radio Design

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

[PackRF Radio Module \(ADRV-PACKRF\)](#)

Design and Integration Files

[Schematics, Layout Files, Bill of Materials, Software, Mechanical Drawings](#)

CIRCUIT FUNCTION AND BENEFITS

The pair of radios in the [ADRV-PACKRF](#) kit provides a radio frequency (RF) platform to software developers, system architects, algorithm developers, and product teams who want a single platform that operates over a wide tuning range (70 MHz to 6 GHz) with a wide bandwidth (200 kHz to 56 MHz). The open source hardware device language (HDL) and Linux software can stream to MATLAB®, Simulink®, or GNU Radio and allows algorithm deployment to the built in the field programmable gate

array (FPGA). The radio modules accelerate development from initial evaluation and concepts to prototype to field deployment.

Included with the radio module is a complete single carrier modem reference design. The modem is designed as a constantly transmitting frequency division duplexing (FDD) system with a single transmit channel (uplink) and a single receive channel (downlink), enabling a single bidirectional point-to-point link between two nodes. A complete wireless video link can be demonstrated with the webcams provided in this kit between disjoint nodes.

The radio is contained inside an aluminum enclosure with access to connections for power, Ethernet, USB, OLED display, audio, and micro SD card. The antennas connect to SMAs on the back of the device for transmit (Tx), receive (Rx), Tx monitoring, and global positioning satellite (GPS) input/outputs.

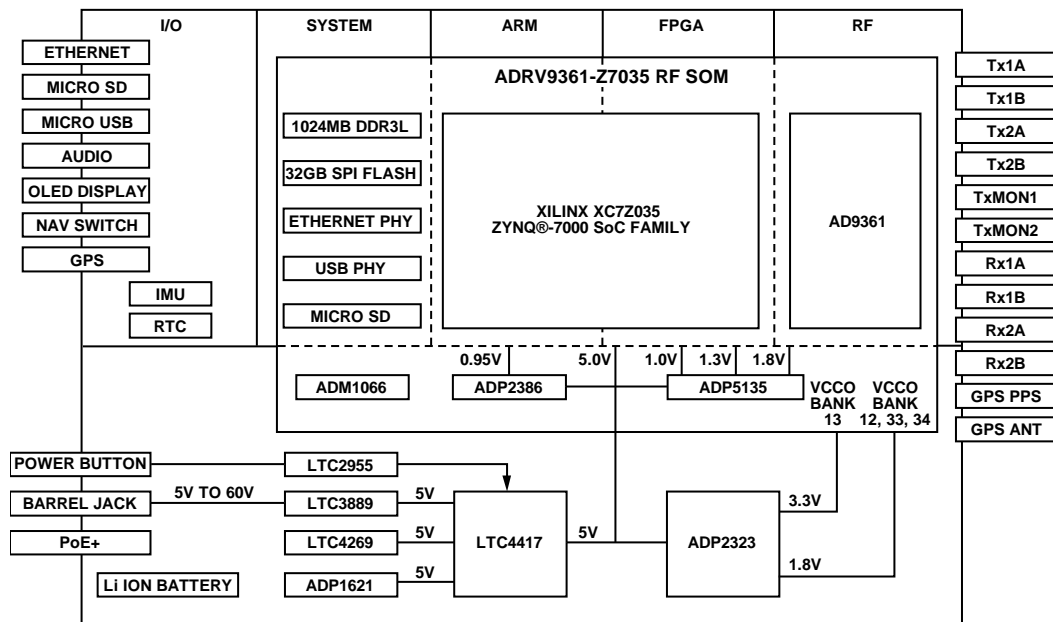


Figure 1. Portable Radio Reference Design Block Diagram

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Portable Radio Reference Design

The portable radio reference design is a combination of the [ADRV9361-Z7035](#) RF system-on-module (SOM), a custom carrier board, custom and autogenerated HDL, custom Linux kernel, and user space software. This combination provides an open source end to end reference design for hardware, software, and HDL to form a complete datalink that can make a Linux TCP/IP connection.

The project also includes MATLAB floating point simulations, Simulink floating point models, and HDL capable fixed-point models of a single carrier QPSK modem design. It also includes integrations with other SDR devices including PlutoSDR, FCOMMS2/3/4, and [ADRV-PACKRF](#) for real-world testing.

All designs have been developed to communicate over the air with one another and share a common testing harness for validation. Together, these designs demonstrate a true development cycle from simulation to hardware deployment. For deployment, which is completely untethered from MATLAB or Simulink, a specialized/custom reference design was created through the Analog Devices board support package (BSP) and demonstrates a video link with the [ADRV-PACKRF](#) kit.

ADRV9361-Z7035 RF SOM

The [ADRV9361-Z7035](#) RF system on module (SOM) provides a standardized FPGA plus transceiver platform to simplify wireless system design and prototyping. This SOM eliminates the need for end users to implement and verify the complex connectivity between an FPGA and converter device, DDR3L, USB 2.0 OTG Phy, and 10/100/1000 Ethernet Phy. Therefore, users can focus on signal processing on the SOM and designing a carrier card with any additionally required hardware.



Figure 2. [ADRV9361-Z7035](#) System on Module

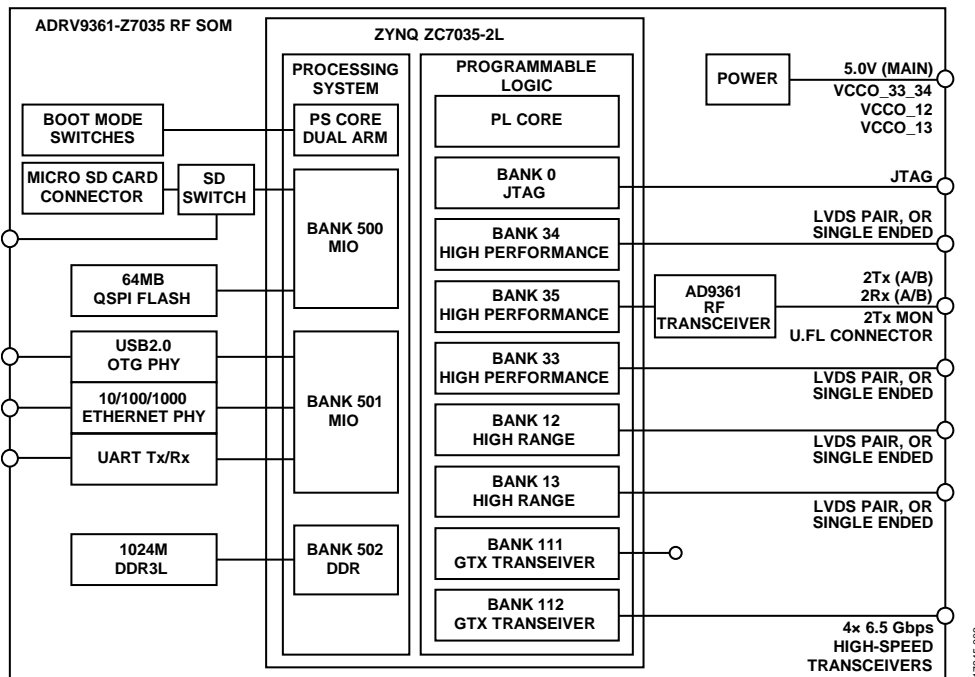


Figure 3. [ADRV9361-Z7035](#) System on Module Block Diagram

ADRV-PACKRF Carrier Card

The custom carrier card inside the [ADRV-PACKRF](#) provides the user with connectors for additional hardware peripherals required for a handheld radio applications, such as sensors, power supplies, a real time clock, and other analog functions.

Several connectors are directly mounted to the carrier card and protrude from the face plate of the [ADRV-PACKRF](#) such as Ethernet, micro SD, DC barrel jack, micro USB, and audio.

Additional headers on the carrier card provide connection to the OLED, navigation switch, IMU, ON/OFF push button, and battery. These modules connect to the carrier card through various cables.

The SOM connects to the carrier card through four 100-pin connectors. The SMAs on the face plate of the box connect directly to the RF transceiver through a series of UFL to SMA cables.

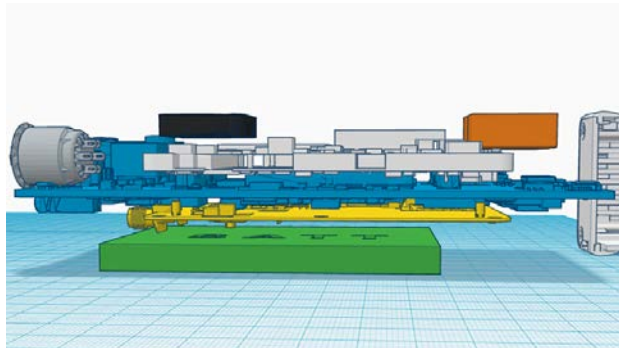


Figure 4. 3D Mechanical Assembly Drawing of the [ADRV-PACKRF](#)

Power

The carrier card is responsible for generating and distributing power to everything contained inside the [ADRV-PACKRF](#). The system can operate from any of three input power supplies:

- Power over Ethernet (PoE)
- External dc supply
- Battery backup

Each input source creates a 5 V rail capable of providing 5 A to all downstream circuitry. The [ADP2323](#) is a dual, synchronous step-down regulator, which creates 3.3 V and 1.8 V supplies needed for powering the peripherals on the [ADRV-PACKRF](#) carrier in addition to powering the [ADRV9361-Z7035](#). Figure 5 details the power distribution for the entire system.

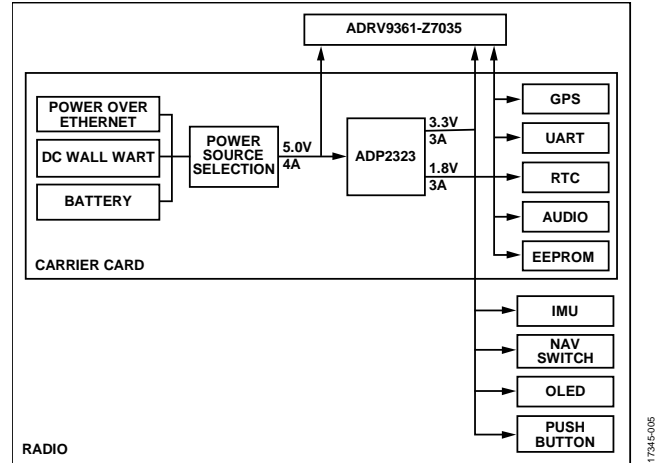


Figure 5. [ADRV-PACKRF](#) Power Distribution

The primary system power source defaults to PoE when present, followed by the external dc wall supply, before relying on the battery backup. If either the PoE or the external dc supply are detected, the battery backup is being charged up in case of power loss.

Power over Ethernet

The [ADRV-PACKRF](#) is an IEEE 802.3at-2009 Type 2 Power over Ethernet (PoE+) standard, or Class 4. Not to be confused with the original IEEE 802.3af-2003 PoE standard, which defined Class 0 to Class 3 and provides up to 12.95 W at the powered device (PD). The updated IEEE 802.3at-2009 PoE+ standard (PoE+ or PoE plus), provides up to 25.5 W of power to a Type 2, Class 4 device.

Table 1. Power over Ethernet Class Definitions.

Class	Type	Power at PSE	Power at PD
0	1 (802.3af)	15.4 W	0.44 W to 12.95W
1	1 (802.3af)	4.0 W	0.44 W to 3.84 W
2	1 (802.3af)	7.0 W	3.84 W to 6.49 W
3	1 (802.3af)	15.4 W	6.49 W to 12.95 W
4	2 (802.3at)	30 W	12.95 W to 25.5 W

The [LTC4269-1](#) high powered device (PD) with integrated synchronous flyback controller creates a 5 V rail for powering the [ADRV-PACKRF](#). It handles all necessary handshaking and only enables itself when connected to receive power from a Type 2 (25.5 W) or higher power sourcing equipment (PSE).

In operation, the trickle charge resistor, R_{TR} , is connected to V_{IN} and supplies a small current, typically on the order of 1 mA to charge C_{TR} . Initially the [LTC4269-1](#) is off and draws only its start-up current. When C_{TR} reaches the V_{CC} turn-on threshold voltage, the [LTC4269-1](#) turns on abruptly and draws its normal supply current. Switching action commences, and the converter begins to deliver power to the output. Initially the output voltage is low, and the flyback voltage is also low; therefore, C_{TR} supplies most of the [LTC4269-1](#) current (only a fraction comes from R_{TR}). V_{CC} voltage continues to drop until, after some time (typically tens of milliseconds), the output voltage approaches its desired value. The flyback winding then provides the [LTC4269-1](#) supply current, and the V_{CC} voltage stabilizes.

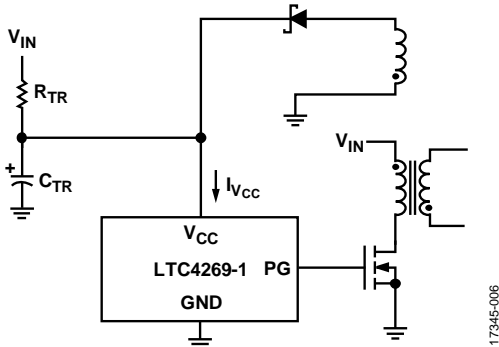


Figure 6. Power over Ethernet Application Circuit

If C_{TR} is undersized, V_{CC} reaches the V_{CC} turn-off threshold before stabilization, and the [LTC4269-1](#) turns off. The V_{CC} node then begins to charge back up via R_{TR} to the turn-on threshold, where the device again turns on. Depending on the circuit, this may result in either several startup-off cycles before proper operation is reached, or permanent startup-off oscillation at the V_{CC} node.

Make C_{TR} large enough to avoid this startup-off oscillation behavior described previously. Empirical testing is the simplest method for determining C_{TR} ; a value of 47 μF is adequate for the [ADRV-PACKRF](#).

External DC Supply

The external dc power supply input is a 5.5 mm barrel jack, which works with the wide input voltage range of the [LTC3899](#) (4.5 V to 60 V) allowing the radio to be powered from a multitude of external supplies including the following:

- AC/DC wall adapter
- Automotive lighter adapter

Not all barrel jacks are the same. The [ADRV-PACKRF](#) requires a positive center conductor, with a 2.1 mm inner diameter and 5.5 mm outer diameter. Double check the requirements: most ac/dc wall adapters have center positive polarity, but some have center negative/barrel positive polarity.

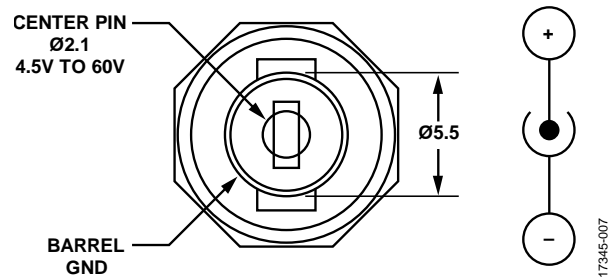


Figure 7. External DC Power Supply Barrel Jack Dimensions

Car power adaptors typically have the 5.5 mm diameter barrel jack and can therefore be used as a suitable power source. One major challenge with this type of power source, however, is the motor cold cranks that are associated with newer fuel-efficient vehicles. Many new automobiles are including an automated start-stop system that turn the engine off at red lights or traffic jams, to meet increased fuel economy metrics. As the engine is restarted, the starter motor cold cranks the battery to start the engine. For safety, the power management system must not droop any supplies during these sorts of stop-start events, where very low voltages (approximately 3 V) can be seen for 10 ms to 100 ms.

Load dump is a similar issue. The voltage surge produced by an automotive alternator when the battery or some other significant load is accidentally disconnected can temporarily be as high as 60 V in a nominal 12 V vehicle. All electronics connected to automotive supplies need to withstand these sorts of voltages.

Battery Backup

The [ADRV-PACKRF](#) includes an internal battery backup, consisting of a rechargeable 3200 mA H Li-Ion battery. The [ADP1621](#) step-up dc to dc controller regulates the battery voltage (3.7 V typical) to create an emergency supply. The battery backup is only capable of powering the system for a limited time. Heavy loads on the FPGA reduce the backup operating time to under 1 hour, but that time depends entirely on system utilization and how much power is being consumed.

The battery has a built-in protection circuit to detect over-charge, over-drain, short circuit, and over-temperature conditions to protect the battery (and system) from damage. The battery is charged from either the other two inputs and is described in detail later in this circuit note.

Battery Charging

Battery charging is overseen by the [ADP5061](#), allowing the user to set and modify certain critical variables, including but not limited to the following:

- Trickle and fast charge current level
- Trickle and fast charge voltage threshold
- Input current limit
- Watchdog time periods
- Weak battery threshold detection
- Battery temperature

Setting and modifying these critical variables ensures that the battery is charged safely and consistently.

The system charges the battery when it is powered down, but it does require power to be applied to the unit. Either PoE or the ac/dc adapter must be plugged into the radio. These voltages do not require validation from the [LTC4417](#) power source selector. The [LTC4415](#) diode ORs these voltages to create a supply voltage specifically for the [ADP5061](#) battery charger IC.

The [LTC4417](#) power source selector output voltage (5 V) is not used to power the battery charge IC because this requires the unit to be turned on to enable battery charging.

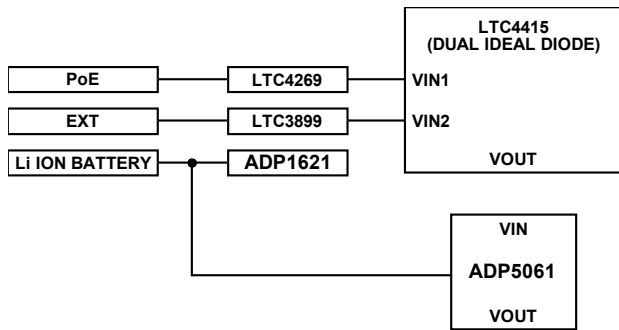


Figure 8. Simplified Battery Charging Loop

Battery Charge Maintenance

Preservation of battery charge is critical for all electronics. Excess current draw must be avoided in all forms. When the battery is not generating 5.0 V, there is a path through the diode, from +V_Batt to +5V_Batt. This means any load on that net (including the resistor dividers, and IC diodes) dissipates battery life. Placing a high current rating transistor in the current path allows a control signal to drive the gate and disconnect the current path from any load. This minimizes load on the battery when the switcher is off.

Power Source Selection

The input power supplies are validated and prioritized for use by an [LTC4417](#) Power Path™ controller. The supplies are arranged according to their physical connections to PoE (V1), external dc supply (V2), and battery backup (V3).

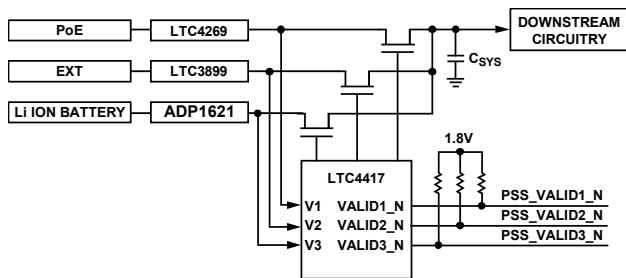


Figure 9. ADRV-PACKRF Carrier Power Source Selection Block

Each input voltage is validated independently by comparing it to undervoltage (UV) and overvoltage thresholds (OV). The voltage must remain inside the window for 256 ms or is considered invalid and the timer resets.

The valid signals are high voltage open drain outputs that pull low when the respective V1, V2, and V3 are within the OV/UV window for 256 ms. The pins are released when V1, V2, or V3 exceed the threshold windows. These connections are routed to the FPGA and allow (with a simple logic table) the system level software to comprehend which power supply is being used and manage its own state depending on which supply is active.

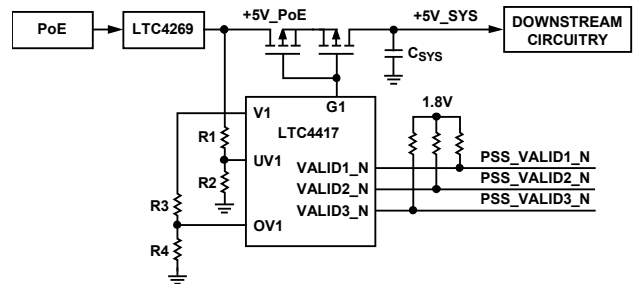


Figure 10. Simplified Threshold Diagram

The [LTC4417](#) compares the inputs at UV1 and OV1 to 1.0 V. Falling below 1.0 V on UV1 signals an undervoltage event. Rising above 1.0 V on OV1 signals an overvoltage event. Resistors are used to divide down the input voltage for comparison against the thresholds.

All three supplies are validated in real time, independent of each other. When an input supply is validated, the corresponding valid signal on the [LTC4417](#) is driven low.

Each channel has a pair of back to back MOSFETS to prevent a back feed of current from one supply to the other.

Care must be taken when deciding what voltage to use for battery validation. Using the battery output (+V_BATT) does not work well for verifying the battery input. It provides no indication if the upconverted voltage is properly regulated. It also places approximately 30 kΩ of resistance between +V_BATT (3.2 V) and GND. This creates a load of 100 μA, which cannot be disabled when the unit is off and continually drains the battery.

Hot Swapping Between Input Supplies

The [ADRV-PACKRF](#) is designed to handle hot swap events. Any of the power supplies can be plugged or unplugged during operation and the system remains powered on (pending sufficient power in the battery backup). All validation and prioritization is still handled by the [LTC4417](#).

A large capacitor bank on the output of the [LTC4417](#) provides power for the system when switching between input supplies. The size of the capacitor bank (C) was determined by a classic equation:

$$C = I \frac{dT}{dV}$$

where:

C is the amount of capacitance required to power the radio when switching between input supplies.

I is the current (maximum) consumed by the radio during operation.

dT is the amount of time over which the capacitor bank must supply the current.

dV is the drop in capacitor voltage caused by the radio consuming power.

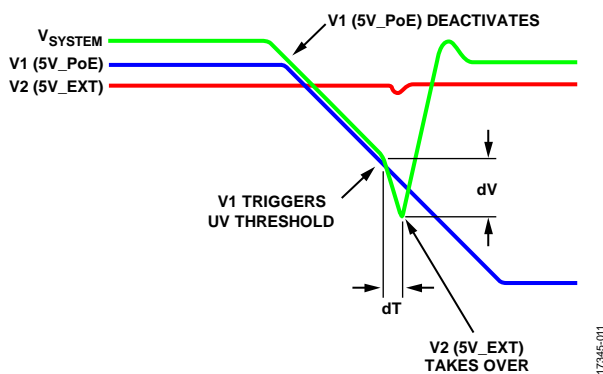


Figure 11. Hot Swap Power Level Example

The data sheet recommends a dT_{MAX} of 20 μ s. The dT used for calculation is 75 μ s to provide significant headroom during hot swap. The maximum amount of current (I) consumed is 4 A.

Determining dV is complicated. The gating item is the [ADRV9361-Z7035](#) input voltage range (4.5 V to 5.5 V). The ADM1166 power supply sequencer on the [ADRV9361-Z7035](#) protects the FPGA by adhering to the specific power on and power off specifications found in the XCZ7035 data sheet. If the voltage drops below 4.5 V, the sequencer shut down the system. Headroom must be included to accommodate switching between supplies.

Consequently, tradeoffs are involved. Insufficient headroom (50 mV) drastically reduces the amount of time the capacitor bank can remain above 4.5 V. A corresponding increase in capacitance is necessary.

$$C = I \frac{dT}{dV} = 4 \times \frac{75 \mu\text{s}}{0.05 \text{ V}} = 6 \text{ mF}$$

Increasing capacitance has negative effects on power supply stability as well as occupying too much physical area on the PCB. It cannot be assumed that the current is lower than the maximum because the radio must operate under all conditions.

Similarly, excessive headroom (400 mV) creates various problems. Although it reduces the capacitance requirement (750 μ F), it also tightens the UV and OV thresholds to a point where any initial accuracy error, line or load regulation, on the input power supplies causes false positives in the UV threshold, and also interrupts the operation of the RF SOM.

The voltage selected was approximately 200 mV:

$$C = I \frac{dT}{dV} = 4 \times \frac{75 \mu\text{s}}{0.2 \text{ V}} = 1.5 \text{ mF}$$

A few empty pads are included to allow modification of the net capacitance in case of temperature, voltage derating, or further modification.

Calculating UV Thresholds

An input power supply voltage dipping below 4.7 V triggers the UV threshold. The [LTC4417](#) input comparators have an input range of 0.985 V to 1.015 V (input error of 1.5%). Using the low end of this range (0.985 V) when working with UV thresholds guarantees operation on all devices.

$$V_{OUT} = \frac{V_{IN}}{R_1 + R_2} \times R_2$$

The values selected for R_1 and R_2 were 16.9 k Ω and 4.53 k Ω . All UV resistors are 0.1% tolerance. Using standard resistor values results in a slight increase of voltage headroom to approximately 230 mV.

Calculating OV Thresholds

An input power supply voltage rising above 5.3 V triggers the OV threshold of the [LTC4417](#). The overvoltage thresholds have the same input range as the undervoltage thresholds (0.985 V to 1.015 V). Using the high end of this range when working with OV thresholds guarantees operation on all devices.

$$V_{OUT} = \frac{V_{IN}}{R_1 + R_2} \times R_2$$

The values selected for R_1 and R_2 were 24.3 k Ω and 5.49 k Ω . All OV resistors are 0.1% tolerance. Using standard resistor values results in a slight increase of voltage headroom to approximately 230 mV.

Brownout

Having such a large capacitor bank on the PCB is helpful in maintaining system operation during hot swap. However, it also presents an unintended negative side effect. The system cannot shut down and reboot quickly (in the order of seconds) because the capacitor bank is not being discharged to ground quickly enough.

A transistor is included, driven by the SYSTEM_ENABLE signal (Figure 12) to decrease the discharge time of this capacitance.

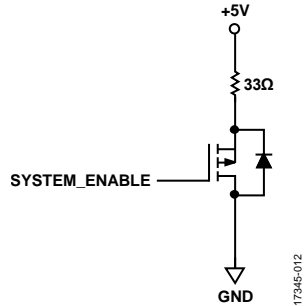


Figure 12. Brownout Circuit Solution

Push Button Controller

The LTC2955 push button controller is responsible for processing any enable, interrupt, or kill signals related to powering up or shutting down the ADRV-PACKRF. A small triple input power multiplexer allows any of the input supplies to power the enable circuitry and guarantees there is always power to this module.

Even when PoE and wall wart are disconnected, the battery voltage powers the enable circuitry and allows proper power cycling of the device. The power consumed by this circuit has minimal impact on battery charge.

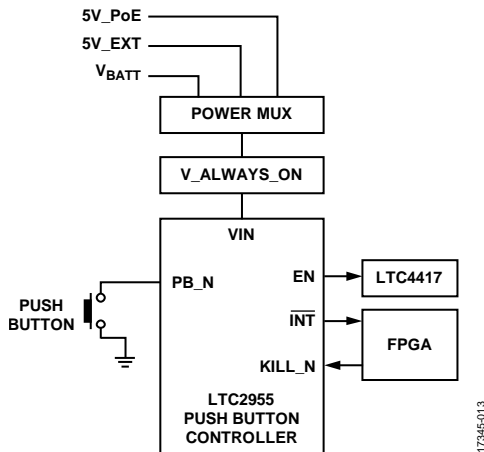


Figure 13. Push Button Controller Block Diagram

OLED Display and Navigation Switch

Each ADRV-PACKRF has a full color 1.69" OLED display and 2-axis mechanical switch with scroll wheel and center select. The display and navigation switch connect to the FPGA and provide control to navigate the menu, read variables, and set and modify characteristics of the ADRV-PACKRF (such as GPS coordinates, IP address, TX and RX LO frequency, and battery state).

IMU

The ADIS16460 is a complete inertial measurement unit (IMU) that includes a tri-axial gyroscope and a tri-axial accelerometer. The IMU is precalibrated in the factory for sensitivity, bias, and alignment. The gyroscope has a measurement range of $\pm 100^\circ/\text{sec}$, $8^\circ/\text{hr}$ (typical) in-run bias stability and $0.12^\circ/\sqrt{\text{hr}}$ (typical) angle random walk on the x-axis. The accelerometer has a $\pm 5\text{ g}$ dynamic range.

GPS

The Quectel L76-M33 IC is a small (10.1 mm x 9.7 mm) GNSS module. The IC can track any GPS or GLONASS signals, using its 33 tracking channels and 99 acquisition channels. The L76-M33 brings low power, anti-jamming, and high sensitivity (-165 dBm tracking, -148 dBm acquisition) to create a fast and accurate GPS capable system.



Figure 14. OLED Showing GPS Coordinates on an ADRV-PACKRF

RTC

The ADRV-PACKRF includes an I²C real-time clock (RTC) with battery-backed SRAM. If the system loses power, the RTC is powered from the battery voltage so it can always keep time accurately.

The RTC shares an I²C address with the ADM1166, a component on the RF SOM. As a result, an I²C address translator is included so each component can be addressed individually. The address for the RTC is changed from 0x68 to 0x69. The table below includes the I²C addresses for all devices found on the carrier board or on the RF SOM.

The interrupt signal of the RTC can be used to enable or disable the system by interacting with the push button controller (LTC2955). This allows the system to be turned on or off after a specific, programmable ΔT .

Audio

The [ADAU1761](#) stereo audio codec coupled with an accessory detection switch, allows use of any open mobile terminal platform (OMTP) or cellular telecommunications industry association (CTIA) headphone standard. With standard detection and jack insert detection, the system identifies and adapts to any standard of device as it is plugged into the box, providing clean, usable audio to the user.

Table 2. OMTP AV Connector Interface

Pin	Description
1	Ground
2	Microphone
3	Right side earpiece
4	Left side earpiece

Table 3. AHJ AV Connector Interface

Pin	Description
1	Microphone
2	Ground
3	Right side earpiece
4	Left side earpiece

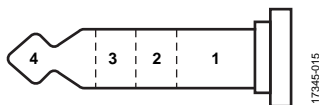


Figure 15. Connector Interface Pin Diagram

Upon insertion, the microphone audio standard is detected and the microphone connection (applies the microphone bias) and routes the ground connection to the headset ground.

Mechanical Design

The [ADRV-PACKRF](#) had several mechanical challenges.

- Component placement
- Enclosure face plate
- 3D modeling, design, and assembly

Component placement between the connectors on the edge of the PCB and the [ADRV9361-Z7035](#) is very tightly packed. The connectors, keep outs, isolation, inductors, and diodes require a great deal of PCB area. Repositioning any connector ended up dictating the rearrangement of the entire front section of the PCB.

A badly designed face plate creates an extremely poor user experience. The primary difficulty was having connectors too close together, making it difficult to interact with individual cables. It is important to remember that people’s fingers come in all shapes and sizes and need to be able to access specific parts of the design without inadvertently touching other parts.

The face plate design also influenced the high density component area of the PCB. As connectors were moved around on the face plate to create a better user experience, so was most of the previously described section of the PCB.

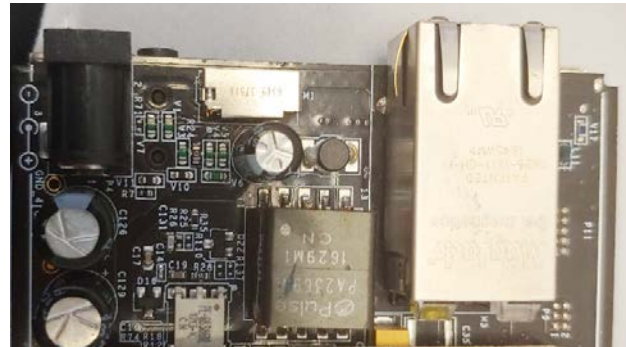


Figure 16. High Density of Component Placement on Carrier Board

3D printing tools were highly beneficial in the design of this system. The first 3D printed item was a to scale model of the prototype PCB for verification of physical constraints. During the early stages of the project, much of the 3D modelling and vertical component collision checking was done.

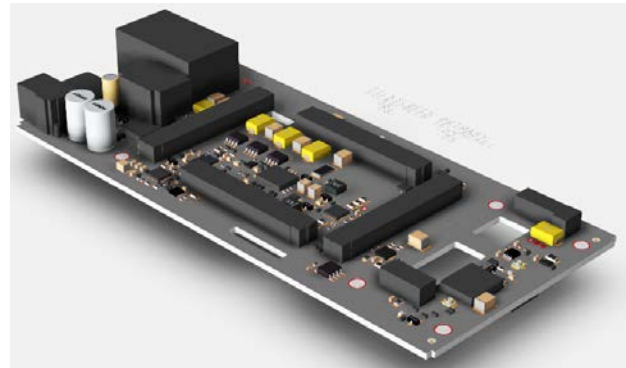


Figure 17. 3D Rendering of the ADRV-PACKRF Carrier Board



Figure 18. Final Enclosure of the ADRV-PACKRF

Face plate revisions were 3D printed as the design was updated for change verification. Slight changes in connector position which did not seem consequential but end up being very important. Therefore, the 3D modeling allowed for quick verification of a potentially expensive mistake.

The biggest assembly challenge was securing the UFL cables inside of the box. Potential for partial or fully disconnected cables is unacceptable once the case is closed. A small 3D printed plastic bracket was instrumental in creating a secure solution for the UFL connectors. The connections are secured by the individual channels in the plastic and held down by screws using the mounting holes of the PCB. Figure 19 shows how the connection of the cable to the PCB is held in place even when the cables are pushed, pulled, and routed as needed.

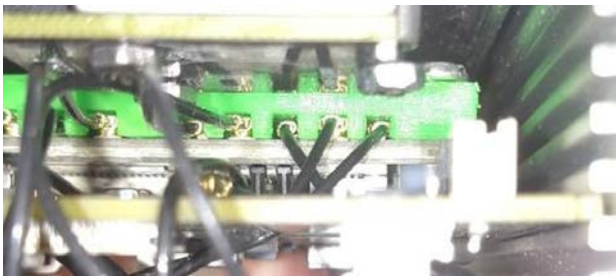


Figure 19. 3D Printed Bracket for the UFL to SMA Cable Connectors

System Software Architecture

The software for the **ADRV-PACKRF** is provided by Analog Devices as an open source reference design that can be used in various applications. The system source code consists of several components, which are used together to control on-board devices and provide connectivity to external tools for

development. The following components are either used to build the **ADRV-PACKRF** firmware or can be used remotely from a host PC through a network connection:

- FPGA HDL code
- Linux kernel/device drivers
- U-boot bootloader
- Graphical user interface (GUI)
- Modem application design
- IIO oscilloscope
- Third-party simulation and development tools
 - MATLAB, Simulink, GNU Radio

The **ADRV-PACKRF** can stream data directly into standard frameworks like MATLAB, Simulink, and GNU Radio for rapid digital signal processing (DSP) prototyping and development. Alternatively, Analog Devices also provides a complete open source application, **IIO-Oscilloscope**, which is useful for simplified debugging and evaluation of the on-board **AD9361** transceiver. This application support is built upon the industrial input/output (IIO) Linux Kernel framework and supporting libIIO userspace library. This allows for remote and on-device control of the different onboard hardware components. The standard kernel provided with the **ADRV-PACKRF** has been customized to support the additional hardware provided with the system, including those outside the IIO framework. These include the on-board GPS receiver, OLED screen, and click wheel interface, among others. For optimized designs requiring minimal PS resources, bare metal drivers are available as well for this platform using the Xilinx® Software Development Kit (XSDK).

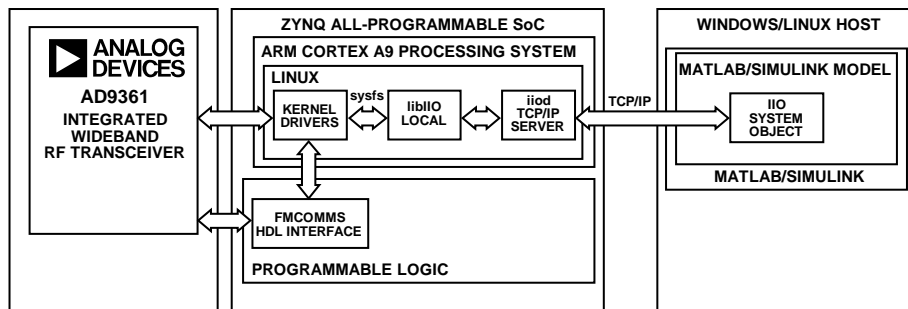


Figure 20. Linux Software Block Diagram

FPGA/HDL Design

A standard hardware device language (HDL) reference design is provided for the [ADRV9361-Z7035](#) designed specifically for the carrier to which the [ADRV9361-Z7035](#) is mounted. HDL targeting is possible through HDL Coder for this reference design for fast prototyping from MATLAB and Simulink.

The entire Rx/Tx data path from low voltage differential signaling (LVDS) transfer to double data rate (DDR) memory storage is implemented in HDL through different IP cores, which allow reconfiguration and porting to final designs.

The [AD9361](#) IP Core implements the LVDS dual port full duplex interface, which allows calibration and verification both

by using the [AD9361](#) clock and data delays and ZC7035 IO delay elements. The IP allows the generation of direct digital synthesis (DDS) signals, dc offset correction, and I/Q correction if needed.

The IP core contains a time division duplex (TDD) logic, which can be used to drive the ENABLE/TXNRX control pins of the device to achieve faster switching in TDD mode, compared to software only control.

The design of the project is highly modular to facilitate porting to a different carrier while maintaining all the IP cores that are used to drive the hardware on the [ADRV9361-Z7035](#).

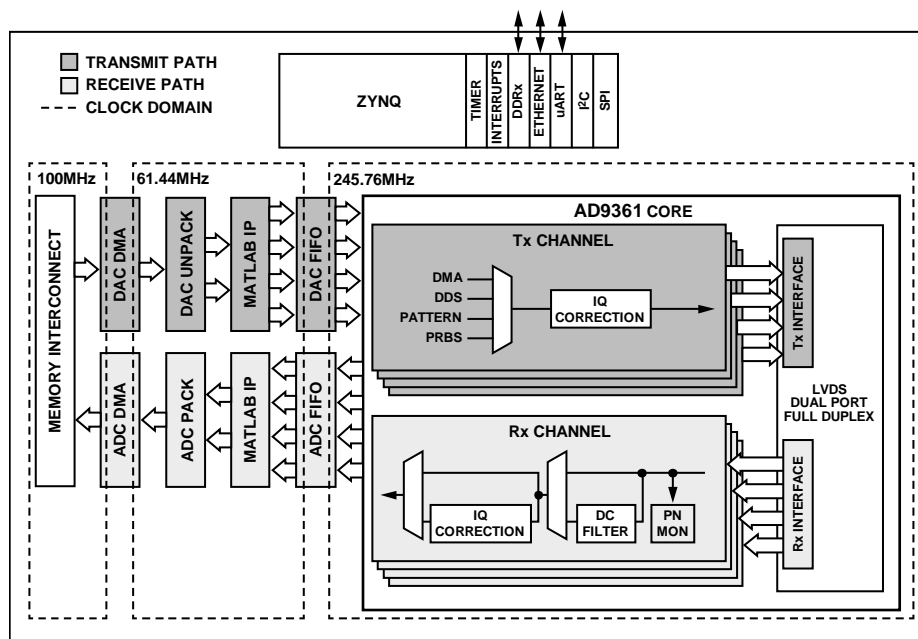


Figure 21. HDL Block Diagram

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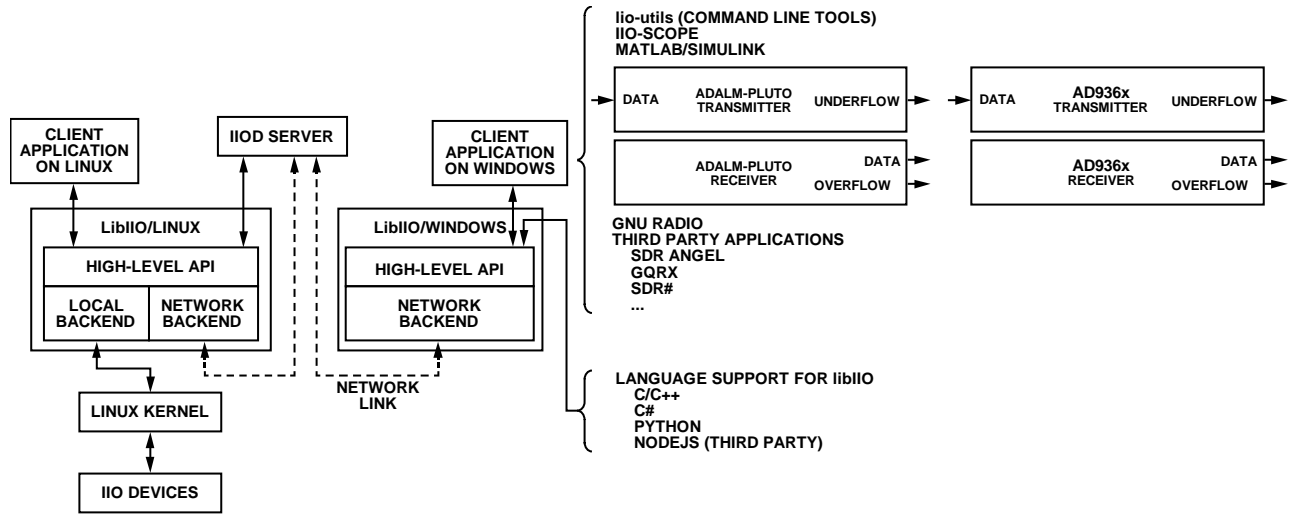


Figure 22. LibIIO Simplified Block Diagram

Linux Subsystem—LibIIO

LibIIO is used to interface to the Linux industrial input/output (IIO) subsystem. The Linux IIO subsystem provides support for Analog Device components that in some sense are analog-to-digital converters (ADCs) or digital to analog converters (DACs). These components include but are not limited to ADCs, accelerometers, gyros, IMUs, capacitance to digital converters (CDCs), pressure sensors, color, light and proximity sensors, temperature sensors, magnetometers, DACs, direct digital synthesis (DDS), phase locked loops (PLLs), variable gain amplifiers (VGAs), programmable gain amplifiers (PGAs), and RF transceivers.

LibIIO can be used natively on an embedded Linux target, or LibIIO can be used to communicate remotely to that same target from a host Linux, Windows®, or MAC computer over USB, Ethernet, or serial. LibIIO abstracts away low level details of the IIO kernel ABI, and therefore focuses on ease of use. This cross platform system library provides also high level C, C++, C#, or Python language bindings, which permits application developers to use their favorite programming languages.

Transceiver Device Driver Stack

The axi_ad9361 IP core is the HDL/FPGA transport layer core used in this project. It handles both Rx/Tx and ADC/DAC transport directions. This single physical IP core is logically split and then handled by two independent IIO drivers, one for each transport data direction. A third control driver configures and controls the AD9361 internal registers; this part is instantiated via the SPI bus and referred to as the PHY (ad9361-phy) driver. The PHY driver controls typical transceiver radio functions such as the LO frequencies, the baseband filters, rates, gain control, Tx attenuation, and more.

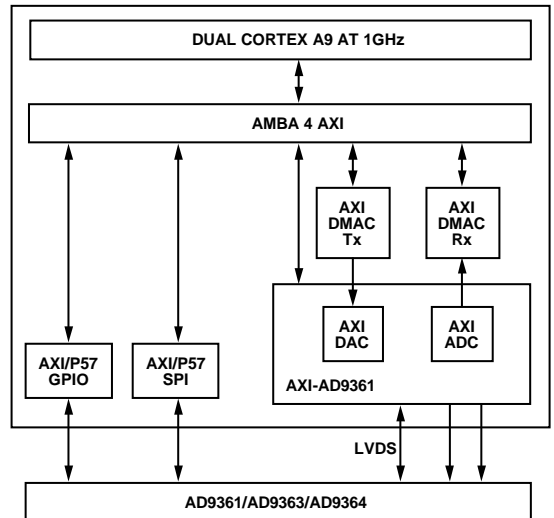


Figure 23. AD9361 Bus Interface Block Diagram

The AXI-ADC HDL driver controls the data receive direction. Device probing for the data capture driver (AXI-ADC), which controls the AXI-HDL core registers and the DMA (AXI_DMAMC), is delayed until the SPI control PHY driver is fully instantiated. This split is required because the AXI-ADC and the SPI PHY parts are instantiated via different busses but share a common data structure, which allows the PHY driver to control and query the AXI registers for parameters such as format conversion, digital interface timing verification, and tuning. Optionally, the PHY driver can also be used independently from the AXI-ADC capture drivers and underlying HDL designs. In addition, the AXI-ADC driver has the option to receive a 1 pps signal from the on-board GPS device and calculate an offset between the synchronization clock source and the baseband rate generated by the AD9361, which allows accurate frequency offset corrections.

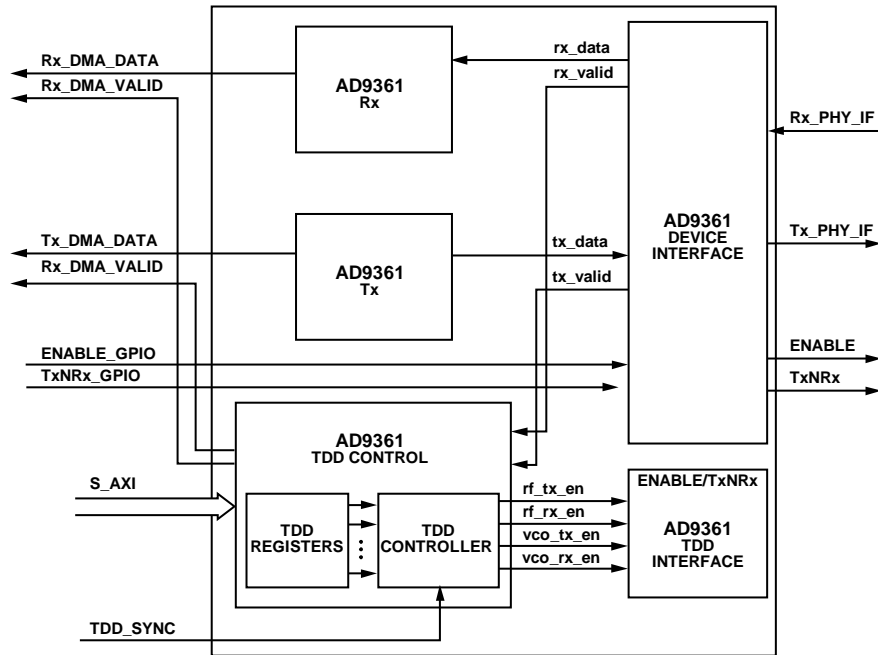


Figure 24. Rx/Tx Flow Control for AD9361 Linux Driver

1794E-024

For the transmit direction, the AXI-DAC-DDS HDL driver is used. Like the capture driver, this driver is also independent from the physical interface layer and therefore it can be used with CMOS or LVDS type interfaces. In this design, this driver is used in standalone mode. However, the Linux common clock framework (CCF) is used so that this driver knows the sampling frequency of the connected converter PHY device.

This transport layer driver also implements a polyphase dual tone DDS core per channel together with a DMA based waveform buffer mechanism. The buffer can be filled by arbitrary data, which is then either cyclically repeated or used in a streaming fashion.

The block diagram in Figure 24 shows the axi_ad9361 IP core with the integrated TDD controller modules inside. If the controller is enabled, all the data flowing to or from the AD9361 is controlled by this module. The device driver used for this block is called AXI TDD HDL driver. Relevant information about all of the software components discussed in this circuit note can be found on their respective Analog Devices Wiki pages.

Software Controlled Components

There are several other Linux device drivers used to control functions on the ADRV-PACKRF. These drivers are all provided as a standard library and included in the custom Linux image for the radio platform.

Table 4. Linux Controlled Software Components.

ADRV-PACKRF Function	Linux Driver Framework
OLED display	Framebuffer device
Rotary wheel	Input device
Navigation buttons	Input device
Power switch	Input device
LEDs	LED class
ADAU1761	ALSA SoC subsystem
ADP5061, LTC2942	Power subsystem
AD9361, ADIS16460	IIO subsystem

ADRV-PACKRF GUI

The graphical user interface (GUI) for the [ADRV-PACKRF](#) provides a simple, scriptable way to implement menus, controls, and launch external applications.

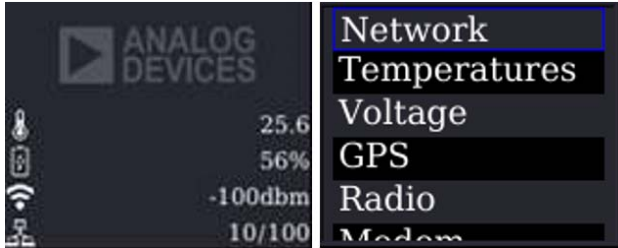


Figure 25. Images of the OLED GUI and Menu

Software Applications

There are many different applications that can be implemented with the [ADRV-PACKRF](#) including communications, instrumentation, radar, and more. Because the device is highly programmable, different HDL and software can be loaded depending on an application then swapped or reconfigured for others. By default, the [ADRV-PACKRF](#) ships with a basic design that allows direct access and control of the on-board transceiver and the raw I/Q data streams. This data can be streamed back to IIO-Scope or other supported third-party tools. To complement this standard design, a point-to-point link modem design is also available for the [ADRV-PACKRF](#). This design can be loaded by changing the supplied SD card, and can then be customized by end users. For more information on available software applications, see the [CN-0412 User Guide](#).

Digital Modem Reference Design

A common purpose for products built around the [ADRV9361-Z7035](#) are portable communication links, which are deployed into areas with no cellular infrastructure or where a user may want to remain off grid. For such applications, where disjoint radios need to communicate, signal processing must be applied to transmitted and received data streams to synchronize the radios for efficient communication. The [AD9361](#) transceiver does not provide link level synchronization because synchronization is waveform dependent. The [ADRV9361-Z7035](#) can be used for implementing the necessary algorithms for a given waveform.

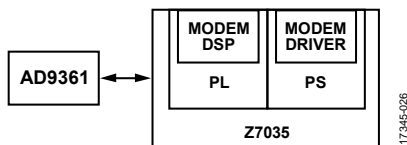


Figure 26. Modem Layout on [ADRV9361-Z7035](#)

Included with the [ADRV-PACKRF](#) is an open single carrier modem design, which demonstrates how a digital communication link can be implemented. This modem reference design (MRD) is split across the programmable logic (PL) and the processing system (PS) on the [ADRV9361-Z7035](#). This partitioning allows for deterministic highspeed digital signal processing (DSP) and flexible control and monitoring.

The MRD uses a frequency division duplexing (FDD) medium access control (MAC) layer to allow continuous transmission and reception between two disjoint radios, as shown in Figure 27, where Radio A has Uplink Frequency 1 and Downlink Frequency 2. This configuration is reversed for Radio B.

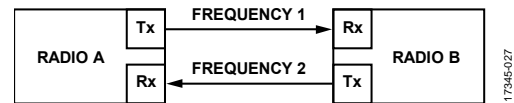


Figure 27. FDD Data Link

The receiver signal processing implemented in the PL of the [ADRV9361-Z7035](#) provides the necessary adaptive algorithms to maintain a link between two radios and converts digital symbols from the transceiver into packetized bits. This receiver signal chain is shown in Figure 28.

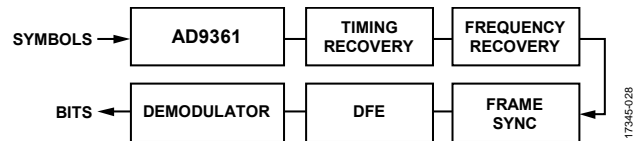


Figure 28. Modem Receiver Signal Chain

This receiver chain handles the ± 25 ppm possible offset between the radios as well as fading in the wireless channel through a decision feedback equalizer (DFE). The MRD can sustain a data rate of 5 Mbps when forward error correction (FEC) is enabled. To achieve this rate, a 5 MHz channel is used with a transceiver synthesis bandwidth of 20 MHz, at a code rate of 1/2 with QPSK modulation.

The modem is exposed to user space in the PS, which is running Linux, as a standard network interface. This was implemented using the TUN/TAP framework provided by the Linux kernel, allowing seamless application level interaction.

Networking Support

TUN/TAP provides networking packet reception and transmission for simple point-to-point or Ethernet devices. Instead of receiving packets from physical media, TUN/TAP receives them from user space program and, instead of sending packets via physical media, writes them to the user space program.

CIRCUIT EVALUATION AND TEST

The setup shown in Figure 29 allows the user to test a simple experiment with the datalink and USB webcams.



Figure 29. Complete ADRV-PACKRF Kit and Contents

Equipment Needed

The following required equipment is included in the PackRF Radio Module (ADRV-PACKRF) kit:

- 2 portable reference radios
- 2 dc wall wart power supplies
- 1 micro USB OTG cable
- 1 C270 HD USB webcam
- 2 micro SD card

Getting Started

This section describes how to set up the test and configuration to replicate the demonstration and results shown in this circuit note. For more detailed information about how to step through the setup of the reference design, see the [CN-0412 User Guide](#).

On Radio 1, use the following procedure:

1. Plug the USB webcam into the USB OTG cable.
2. Plug the USB OTG cable into the micro USB connector on the face plate.
3. Connect Radio 1 with Radio 2 via the Ethernet port using the Ethernet cable.

On Radio 1 and Radio 2, use the following procedure:

1. Insert the provided micro SD cards into the slot.
2. Attach the SMA Antenna to TX1A and RX1A.
3. Plug in the power supplies.
4. Press the power button.

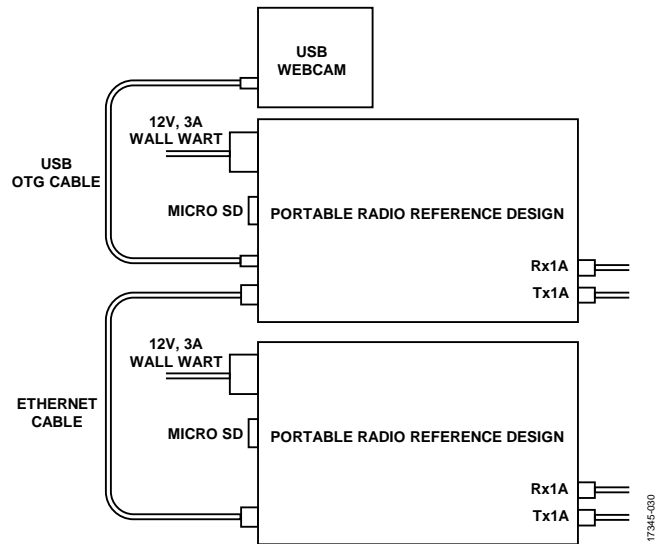


Figure 30. ADRV-PACKRF Webcam Testing Diagram

On Radio 1 (with webcam attached),

1. Open the **Network** menu from the OLED screen.
2. Set the **IP Address** to 192.168.0.101.
3. Set the **Peer IP Address** to 192.168.0.102.
4. Return to the main menu.
5. Open the **Modem** menu.
6. Set the **IP Address** to 192.168.23.1.
7. Set the **Peer IP Address** to 192.168.23.2.

On Radio 2 (no webcam attached),

1. Open the **Network** menu from the OLED screen.
2. Set the **IP Address** to 192.168.0.102.
3. Set the **Peer IP Address** to 192.168.0.101.
4. Return to the main menu.
5. Open the **Modem** menu.
6. Set the **IP Address** to 192.168.23.2.
7. Set the **Peer IP Address** to 192.168.23.1.

On Radio 1 (with webcam attached), run **Autoconfig** from the main menu and allow this action to fully complete.

On Radio 2 (with no webcam attached), go to the OLED screen and from the main menu click **Recv Video**.

On Radio 1 (with webcam attached), go to the OLED screen and from the main menu click **Send Video**.

For more information and complete details on setup, see the [CN-0412 User Guide](#).

LEARN MORE

[ADRV9361-Z7035 Evaluation Board](#)

[CN-0412 Design Support:](#)

www.analog.com/CN0412-DesignSupport

[CN-0412 User Guide](#)

[Linux Software Drivers \(EngineerZone\)](#)

[FPGA Reference Designs \(EngineerZone\)](#)

Data Sheets and Evaluation Boards

[ADRV1CRR-BOB Data Sheet](#)

[ADRV1CRR-FMC Data Sheet](#)

[LTC4417 Data Sheet](#)

[LTC2955 Data Sheet](#)

[ADP5061 Data Sheet](#)

[ADIS16460 Data Sheet](#)

[LTC4415 Data Sheet](#)

[LTC4269-1 Data Sheet](#)

[LTC3899 Data Sheet](#)

[ADP1621 Data Sheet](#)

[ADP2323 Step Down Regulator Data Sheet](#)

REVISION HISTORY

7/2019—Revision 0: Initial Version

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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