Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0305.

Devices Connected/Referenced	
AD7988-5	16-Bit, 500 kSPS PulSAR ADC
OP1177	Precision Low Noise, Low Input Bias Current Op Amp
ADR435	Ultralow Noise XFET® 5.0 V Voltage

16-Bit, 300 kSPS Low Power Data Acquisition System Optimized for Sub-Nyquist Input Signals up to 4 kHz

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0305 Circuit Evaluation Board (EVAL-CN0305-SDPZ)

System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a 16-bit, 300 kSPS successive approximation analog-to-digital converter (ADC) system that has a drive amplifier that is optimized for a low system power dissipation of 10.75 mW for input signals up to 4 kHz and sampling rates of 300 kSPS.

This approach is highly useful in portable battery powered or multichannel applications, or where power dissipation is critical. It also provides benefits in applications where the ADC is idle most of the time between conversion bursts.

Drive amplifiers for high performance successive approximation ADCs are typically selected to handle a wide range of input frequencies. However, when an application requires a lower sampling rate, considerable power can be saved because reducing the sampling rate reduces the ADC power dissipation proportionally.

To take full advantage of the power saved by reducing the ADC sampling rate, a low bandwidth, low power amplifier is required.

For example, the 80 MHz ADA4841-1 op amp (12 mW at 10 V) is recommended for inputs up to approximately 100 kHz with the AD7988-5 16-bit successive approximation register (SAR) ADC (3.5 mW at 500 kSPS and 2.1 mW at 300 kSPS). The total system power dissipation including the ADR435 reference (4.65 mW at 7.5 V) is 18.75 mW at 300 kSPS.

For input bandwidths less than 4 kHz and sampling rates less than 300 kSPS, the 1.3 MHz OP1177 op amp (4 mW at 10 V) offers excellent signal-to-noise ratio (SNR) and total harmonic distortion (THD) performance and reduces total system power from 18.75 mW to 10.75 mW, which is a 43% power savings at 300 kSPS.

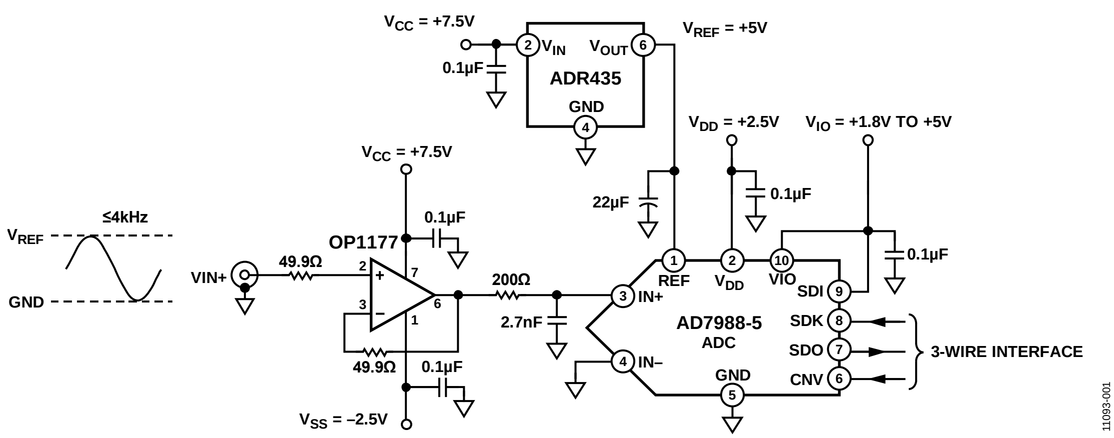

Figure 1. System Circuit Diagram of Low Power OP1177 Amplifier Driving the AD7988-5 ADC (Simplified Schematic: All Connections Not Shown)

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CIRCUIT DESCRIPTION

The circuit comprises the AD7988-5 ADC, OP1177 amplifier, and ADR435 reference. The AD7988-5 is a 16 bit, 500 kSPS SAR ADC whose low power is scalable with sampling rate and consumes 3.5 mW at 500 kSPS. Its low power also comes with industry-leading ac performance: SNR = 91 dB and THD = −114 dBc.

The driving amplifier is the low power, precision OP1177 that has a supply current of 400 µA and a gain bandwidth product of 1.3 MHz. The OP1177 can be driven with supplies ranging from 5 V to 30 V. The reference for the ADC is the ADR435, which is a high precision, low noise, 5 V XFET voltage reference. The ADR435 has a very low temperature coefficient of 3 ppm/°C at a low supply current of 620 µA. The total power for this circuit is 10.75 mW at 300 kSPS. The SNR is 90.6 dBFS, and the THD is −102 dBc with an input frequency up to 4 kHz.

The OP1177 is configured as a unity-gain buffer and has an RC filter (200 Ω, 2.7 nF) with a 295 kHz cutoff frequency between it and the AD7988-5. The filter allows the use of a higher noise amplifier, such as the OP1177, at 8nV/√Hz while still getting the benefits of much lower power consumption. The tradeoff of higher noise for lower power causes only 0.4 dB reduction in the SNR performance of the system. The higher value of R (200 Ω) relative to the recommended data sheet value (20 Ω) means the OP1177 can drive the large 2.7 nF input capacitor. The higher R value limits the maximum input bandwidth to a few kHz for low distortion.

This compares favorably to the 16-bit distortion performance (THD less than −100 dBc) of the OP1177 for up to 5 kHz inputs. Distortion increases beyond 5 kHz so that it is not advisable to use this circuit with higher input frequencies or to use this amplifier in a multiplexed application due to the long settling time. Note that the OP1177 requires at least 1.5 V of input headroom/footroom and 1 V of output headroom/footroom when setting the supplies. In addition, note that the OP1177 cannot be used to drive the AD7988-5 above 300 kSPS because the driver settling time is not sufficient for the shorter ADC acquisition time (see Figure 3).

Performance Results

The goal of this circuit is to deliver good ac performance at the lowest ADC driver power level possible for input frequencies less than 4 kHz at a sampling rate of 300 kSPS. Figure 2 shows an FFT plot of the circuit performance for a 4 kHz input. The SNR is 90.6 dBFS, and the THD is −102 dBc. The main reason for the slight reduction in SNR from the 91 dBFS specification of the AD7988-5 is the higher noise of the OP1177 of 8 nV/√Hz vs. 2 nV/√Hz for the ADA4841-1. The total system power is 10.75 mW: 2.1 mW for the ADC (running at 300 kSPS), 4 mW for the amplifier, and 4.65 mW for the reference. This represents a 43% reduction in power from using the ADA4841-1, which consumes 12 mW for a total system power of 18.75 mW.

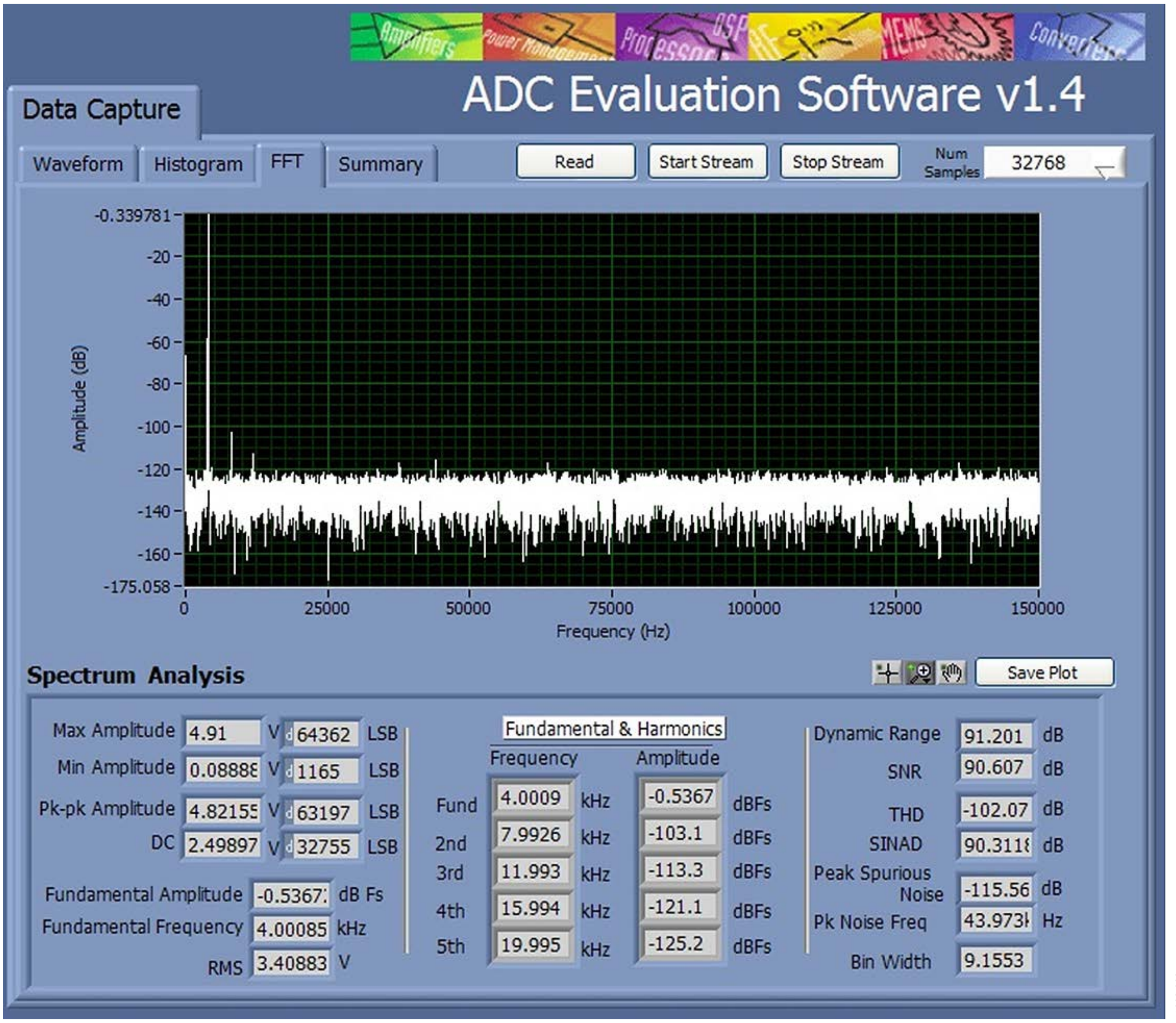

Figure 2. System Circuit Performance of Using the OP1177 Amplifier Driving the AD7988-5

Figure 3 shows how the system THD increases and the SNR decreases at higher sampling rates above 300 kSPS. For this reason, operate the ADC at 300 kSPS or lower for best performance.

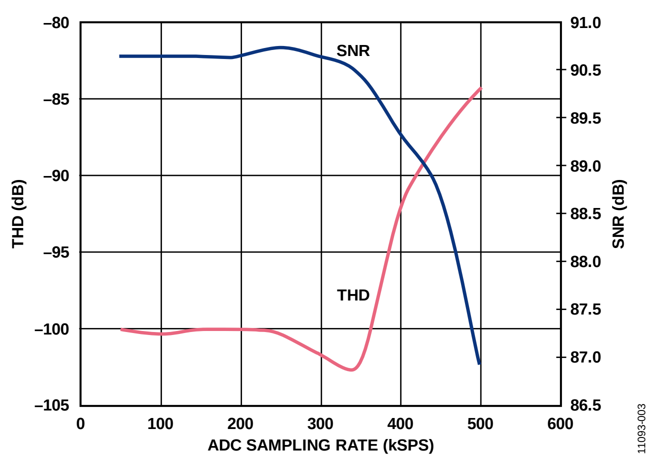

Figure 3. THD and SNR vs. ADC Sampling Rate for OP1177 Amplifier Driving the AD7988-5

Figure 4 shows how the system THD increases and the SNR decreases with input frequencies above 4 kHz. This is due to the amplifier distortion as can be seen in the THD+N vs. frequency plot shown in Figure 5.

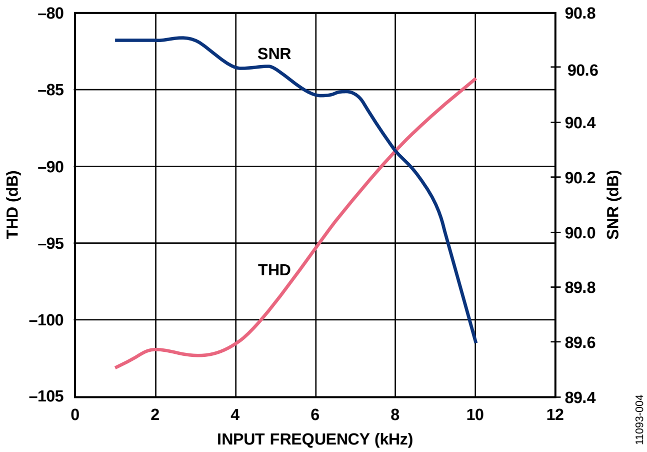

Figure 4. THD and SNR vs. Input Frequency for OP1177 Amplifier Driving the AD7988-5

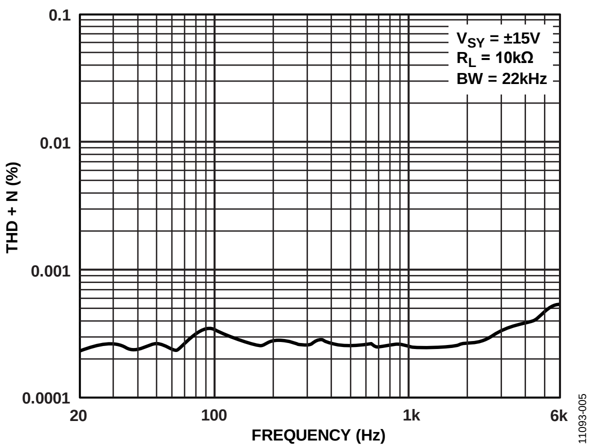

Figure 5. THD+N vs. Input Frequency Performance the OP1177 Amplifier

COMMON VARIATIONS

The OP1177 amplifier can be used to drive pin-compatible ADCs like the AD7988-1 up to 100 kSPS and the AD7980 up to 300 kSPS. The AD8641 amplifier can be used to drive the AD7988-5 at half the power (200 µA); however, only up to 100 kSPS with reduced ac performance and a lower input frequency range (see the CN-0306 circuit note).

CIRCUIT EVALUATION AND TEST

Equipment Needed (Equivalents Can Be Substituted)

The following equipment is needed:

- The EVAL-CN0305-SDPZ evaluation board
- The System Demonstration Board (EVAL-SDP-CB1Z)
- A function generator/signal source, such as the Audio Precision SYS-2522 used in these tests
- The 9 V wall power supply included with the EVAL-CN0305-SDPZ evaluation board
- A PC with a USB port, a USB cable, and the 10-lead PulSAR software installed

Setup and Test

Install the 10-lead PulSAR software downloadable from the AD7988-5 product page on the Analog Devices, Inc., website using the installation guide in the UG-340 user guide. The block diagram of the measurement setup is shown in Figure 6. Connect the 9 V wall power supply to the evaluation board power terminal. To measure the frequency response, connect the equipment as shown in Figure 6. Set the Audio Precision SYS-2522 signal generator for a 4 kHz frequency and a 5 V p-p sine wave with a 2.5 V dc offset. Set the ADC sample rate in the software window to 300 kSPS. Record the data using the evaluation board software. The software analysis is part of the evaluation board software that allows the user to capture and analyze ac and dc performance. This software and its features are described in detail in the UG-340 user guide.

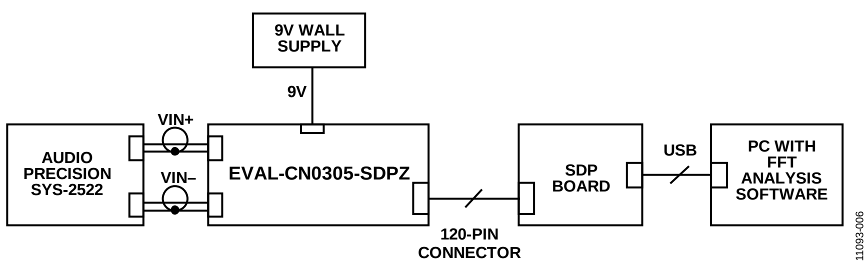

Figure 6. Functional Diagram of Test Setup

LEARN MORE

CN0305 Design Support Package: http://www.analog.com/CN0305-DesignSupport

UG-340 User Guide, *Evaluation Board for the 8-/10-Lead Family of 14-/16-/18-Bit PulSAR ADCs*, Analog Devices.

EVAL-SDP-CB1Z System Demonstration Platform (SDP)

MT-021 Tutorial, *Successive Approximation ADCs*, Analog Devices

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND,"* Analog Devices.

MT-101 Tutorial, Decoupling Techniques, Analog Devices.

Voltage Reference Selection and Evaluation Wizard, Analog Devices

Data Sheets and Evaluation Boards

CN-0305 Circuit Evaluation Board (EVAL-CN0305-SDPZ)

System Demonstration Platform (EVAL-SDP-CB1Z)

AD7988-1 Data Sheet

AD7988-5 Data Sheet

AD7980 Data Sheet

ADR435 Data Sheet

AD8641 Data Sheet

OP1177 Data Sheet

ADA4841-1 Data Sheet

REVISION HISTORY

12/13—Rev. 0 to Rev. A

Changes to Title 1

11/12—Rev. 0: Initial Version

CN11093-0-12/13(A)