ANALOG DEVICES

Circuit Note
CN-0268

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Devices Connected/Referenced	
ADL5565	6 GHz Ultrahigh Dynamic Range Differential Amplifier
AD9467	16-Bit, 200 MSPS/250 MSPS ADC

Resonant Approach to Designing a Band-Pass Filter for Narrow-Band, High IF, 16-Bit, 250 MSPS Receiver Front End

EVALUATION AND DESIGN SUPPORT

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a 16-bit, 250 MSPS, narrow-band, high IF receiver front end with an optimum interface between the ADL5565 differential amplifier and the AD9467 ADC.

The AD9467 is a buffered input 16-bit, 200 MSPS or 250 MSPS ADC with SNR performance of approximately 75.5 dBFS and SFDR performance between 95 dBFS and 98 dBFS. The ADL5565 differential amplifier is suitable for driving IF sampling ADCs because of its high input bandwidth, low distortion, and high output linearity.

This circuit note describes a systematic procedure for designing the interface circuit and the antialiasing filter that maintains high performance and ensures minimal signal loss. A resonant approach is used to design a maximally flat Butterworth fourth-order band-pass filter with a center frequency of 200 MHz.

CIRCUIT DESCRIPTION

The advantages of using a differential amplifier to drive a high speed ADC include signal gain, isolation, and source impedance matching to the ADC. The ADL5565 allows pin-strappable gain adjustments of 6 dB, 12 dB, or 15.5 dB. Alternatively, by applying two external resistors to the inputs, finer gain steps can be achieved within the 0 dB to 15.5 dB range. Additionally, the ADL5565 offers high output linearity, low distortion, low noise, and wide input bandwidth. The 3 dB bandwidth is 6 GHz, and the 0.1 dB flatness is 1 GHz. The ADL5565 is capable of achieving an output third-order intercept (OIP3) of greater than 50 dB.

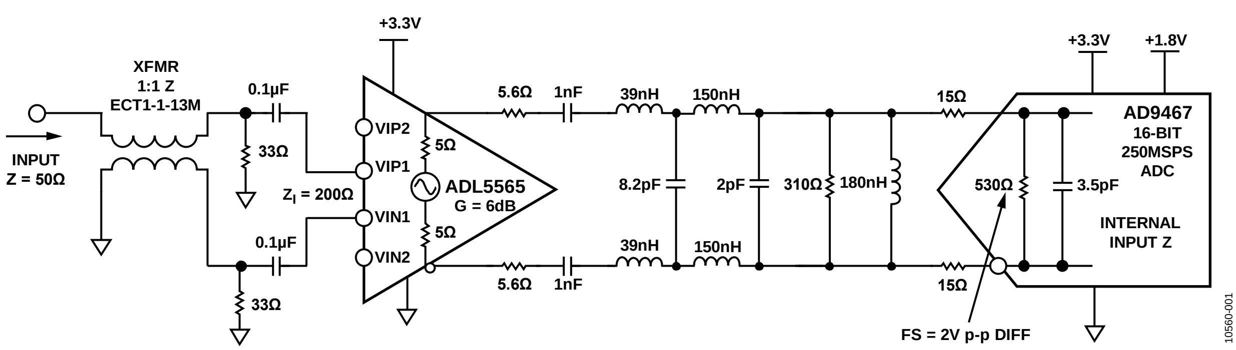

Figure 1. Resonant Filter Design for Narrow Band High IF Applications Using the ADL5565 Differential Amplifier and the AD9467 ADC

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To achieve the optimal level of performance that the ADL5565 and AD9467 have to offer, it is important to properly follow the design guidelines as specified on the respective data sheets. Some of the important design criteria include properly matching the input and output impedance of the ADL5565 for minimum signal loss and optimum linearity performance, systematic design of an antialiasing filter for improved dynamic range, and source impedance matching to the ADC inputs.

ADL5565 Input Impedance Matching

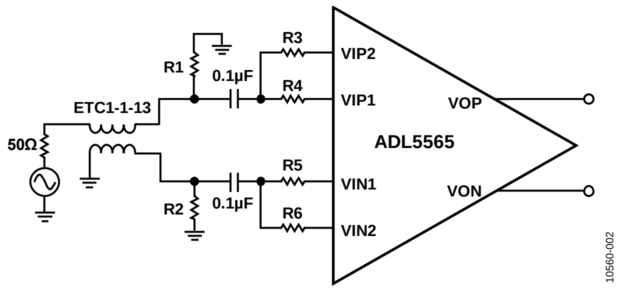

Figure 2. ADL5565 Input Impedance Match

Figure 2 shows the recommended input matching network for the ADL5565. The input impedance of the ADL5565 is gain dependent, and the differential input impedance is 200 Ω for 6 dB gain, 100 Ω for 12 dB gain, and 67 Ω for 15.5 dB gain. To match the 50 Ω source impedance of the signal generator to the input impedance of the ADL5565, R1 and R2 must be chosen so that their sum in parallel with the input impedance of the ADL5565, Z_I, is equal to 50 Ω. To maintain balance in the differential circuit, R1 must equal R2. The following formula can be used to calculate the necessary matching resistors.

$$R1 = R2$$

$$2R1 \,||\, Z_I = 50\ \Omega$$

$$R1 = R2 = \frac{25}{1-(50/Z_I)}$$

Table 1 shows the calculated termination resistors and pin configuration for the different gain settings of the ADL5565.

An alternative configuration to the one shown in Figure 2 is to replace the 1:1 balun, ETC1-1-13, with an impedance transformation RF transformer. This can eliminate the need for R1 and R2. A 1:4 transformer can be used for the 6 dB gain configuration or a 1:2 transformer for the 12 dB gain configuration. The advantages of this alternative configuration are lower component count and minimum signal loss. However, pay attention to the bandwidth of the transformer. Impedance transformation transformers have narrower bandwidths and higher insertion loss as compared to a 1:1 balun.

Figure 2 shows a single-ended-to-differential approach to driving the ADL5565 using a balun or transformer. This configuration may not be a viable or desirable option in certain applications. The ADL5565 offers flexibility in its driver interface and can be driven single ended, as shown, or differentially with a differential mixer, for example. Refer to the ADL5565 data sheet for details on the different input interfaces.

ADL5565 Output Load Matching

The ADL5565 linearity performance has been optimized for a 200 Ω output load. This is a common output impedance used to interface to ADCs and for filter design. With an optimized output load of 200 Ω, the output IP3 of the ADL5565 at 200 MHz is 46 dBm.

In situations where a 200 Ω output load may not fit the application, tradeoffs can be made between the output load of the ADL5565 and its linearity performance. Figure 3 shows a plot of third-order intermodulation (IMD3) vs. frequency for commonly used output loads.

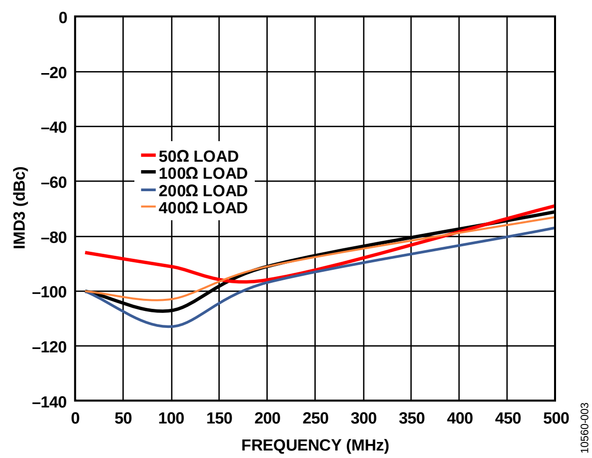

Figure 3. ADL5565 IMD3 vs. Frequency for 50 Ω, 100 Ω, 200 Ω, and 400 Ω Output Loads, 3.3 V Supply, Gain = 6 dB

Table 1. Gain, Input Impedance, and R1, R2, R3, R4, R5, and R6 Values for ADL5565

Gain (dB)	ADL5565 Input Impedance, Z_I, (Ω)	R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)	R5 (Ω)	R6 (Ω)
6	200	33	33	Open	0	0	Open
12	100	50	50	0	Open	Open	0
15.5	67	Open	Open	0	0	0	0

AD9467 Source Impedance

The AD9467 is an ideal choice for an ADC in this circuit because it is an IF sampling ADC optimized for high performance over wide bandwidths and ease of use. The AD9467 has an integrated buffer that presents a fixed input impedance to the driver amplifier. This input structure is an advantage over ADCs that use an unbuffered front end directly coupled to the sampling switches. Unbuffered ADCs present time varying input sample-and-hold impedances to the drive amplifier. The addition of the input buffer eases the drive requirements at the expense of slightly higher power consumption. The buffered source impedance of the AD9467 is modeled as a fixed impedance of a 530 Ω resistance in parallel with a 3.5 pF capacitance.

When interfacing to the ADC, it is recommended that the real input impedance be reduced from 530 Ω to a lower value within the 200 Ω to 400 Ω range. By lowering the input impedance of the ADC, the kickback due to the sample-and-hold structure settles out faster, yielding improved linearity performance. The tradeoff is increased input power because more power is required to drive the full scale of the ADC. In this circuit example, the input impedance of the AD9467 was reduced to 200 Ω to match the output impedance of the ADL5565 and also to balance the linearity vs. input power of the ADC. The input impedance of the AD9467 was reduced to 200 Ω by placing a 310 Ω resistor in parallel with the ADC differential input.

Antialiasing Filter Design

An antialising filter ahead of the ADC helps reduce signal content and noise from unwanted Nyquist zones that would otherwise alias in band and degrade the dynamic performance. Antialiasing filters are often designed using LC networks and must have well defined source and load impedances to achieve the desired stop-band and pass-band characteristics. The filter design is accomplished using software available from Nuhertz Technologies or Agilent Technologies Advanced Design Systems (ADS), for example.

In the circuit in Figure 1, the ADS program was used to design a fourth-order maximally flat (Butterworth) low-pass filter. Figure 4 shows the low-pass filter design with a source and load impedance of 200 Ω and a 3 dB cutoff frequency of 300 MHz. The 200 Ω impedance was chosen because it is the common source and load impedance of the driver amplifier and ADC. The first elements are series inductors to ease driver requirements.

In the final optimized circuit of Figure 1, the filter source impedance is equal to approximately 21.6 Ω; however, 200 Ω was chosen to design the low-pass portion of the filter because the overall filter is ultimately a resonant band-pass filter, and it is more critical that the amplifier and ADC see the correct load and source impedance for optimized linearity performance. The effect of doing this is amplitude loss due to the impedance mismatch.

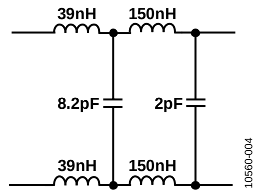

Figure 4. Low-Pass Filter Design

The low-pass filter design was further tuned by creating resonance to cause peaking at the band of interest. This resulted in a narrow-band, band-pass filter at a high IF. Placing an inductor across the ADC differential inputs nulls the input capacitance of the ADC and creates peaking. Figure 5 shows the calculation used to determine the resonant inductor value. In the case of the 3.5 pF source impedance of the AD9467, a parallel inductor of 181 nH is necessary to null the capacitive susceptance; leaving only the high impedance resistive portion of the RC parallel equivalent. The resonant frequency chosen for the calculation was 200 MHz.

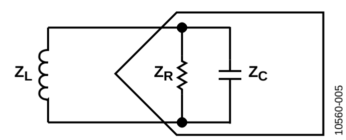

Figure 5. Resonant Match

$$Z_C = \frac{1}{j\omega C}$$

$$Z_L = j\omega L$$

$$Y_C = \frac{1}{Z_C}$$

$$Y_L = \frac{1}{Z_L}$$

$$Y_C + Y_L = 0$$

$$L = \frac{1}{\omega^2 C}$$

Measured Performance

Figure 1 shows the final circuit configuration. The outputs of the ADL5565 were padded with 5.6 Ω on each output to improve the stability of the driver amplifier. The recommended series resistance is generally between a few ohms to several tens of ohms. A larger resistor value improves on stability; however, the tradeoff is a power loss because the series resistor forms a voltage divider with the impedance at the ADC inputs, resulting in signal attenuation.

Following the series resistors at the output of the ADL5565 are 1 nF dc blocking capacitors. Following that is the antialiasing filter and then the parallel resistor of 310 Ω to reduce the input impedance of the ADC. Finally, the 15 Ω resistors in series with the ADC inputs isolate the internal switching transients from the filter and the amplifier.

Figure 6 and Figure 7 shows the resulting antialiasing filter response with a 1 dB bandwidth of 41 MHz and a 3 dB bandwidth of 89 MHz, centered at an IF of 203 MHz. Figure 8 shows the FFT spectrum for the final receiver circuit of Figure 1, where the SNR is 72.5 dBFS, and the SFDR performance approaches 90 dBc.

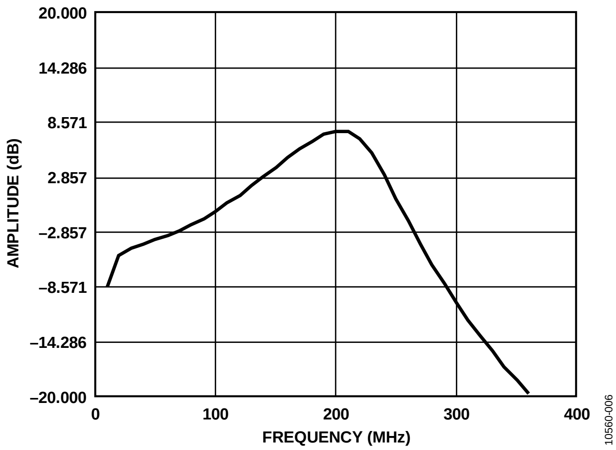

Figure 6. Antialiasing Filter Response, f_C = 203 MHz

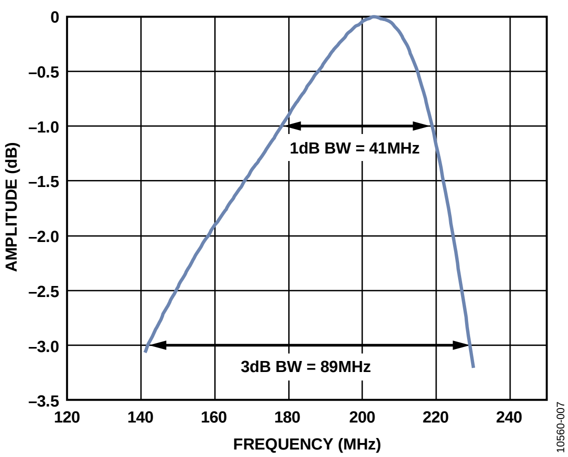

Figure 7. Antialiasing Filter Response, f_C = 203 MHz, 1 dB and 3 dB Bandwidth

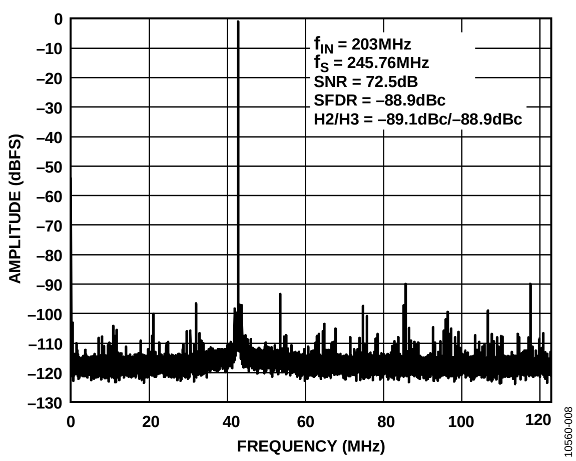

Figure 8. Single Tone FFT Plot, Input = 203 MHz, Sampling Rate = 245.76 MSPS

Using ADS as a simulation tool, the filter components can be further tuned to shift the resonant peak to the desired IF. For example, by changing the parallel 8.2 pF capacitor of the antialiasing filter to 10 pF shifts the resonance peak lower to 180 MHz. Figure 9 through Figure 11 show the filter profile and single-tone FFT performance for this condition.

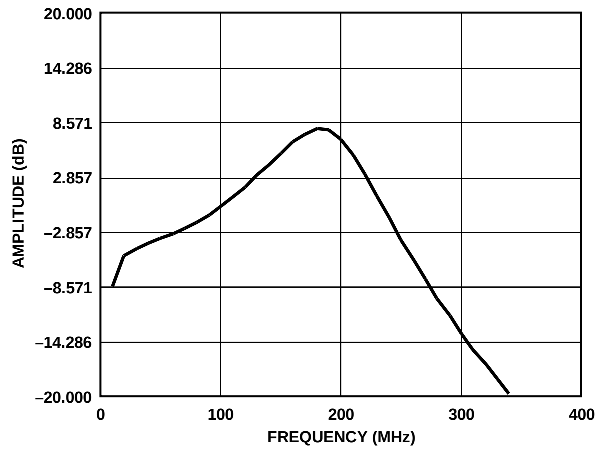

Figure 9. Antialiasing Filter Response, f_C = 183 MHz

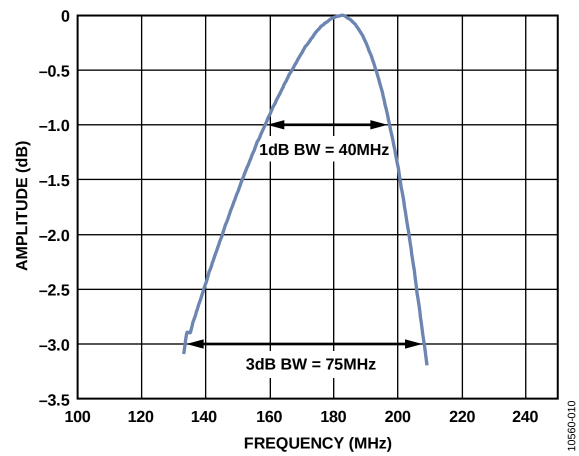

Figure 10. Antialiasing Filter Response, f_C = 183 MHz, 1 dB and 3 dB Bandwidth

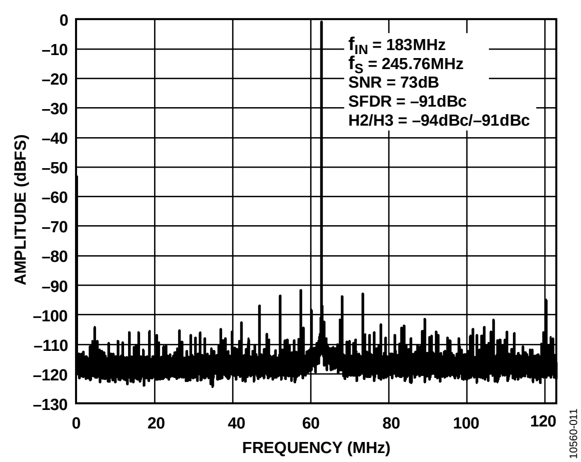

Figure 11. Single Tone FFT Plot, Input = 183 MHz, Sampling Rate = 245.76 MSPS

COMMON VARIATIONS

Quite a few combinations of drivers and high speed ADCs are available; however, for optimum performance, it is important to pay attention to the input and output impedance of the ADC driver and the input reactance of the ADC. Each device has its own unique impedance characteristic. A common variation to the Figure 1 circuit is the ADL5562 (3.3 GHz bandwidth) driving the AD9467 with a low-pass, antialiasing filter design for wideband receiver applications, as described in Circuit Note CN-0227.

Similarly, Circuit Note CN-0110 describes using the ADL5562 differential driver amplifier to drive wide bandwidth ADCs, such as the AD9445, for high IF ac-coupled applications. Another alternative where variable gain is desired, the ADL5565 can be replaced with the AD8375 variable gain amplifier. The AD8375 is a digitally controlled, variable gain, wide bandwidth amplifier that provides precise gain control across a broad 24 dB gain range with 1 dB resolution. The AD8376 is a dual version of the AD8375. Circuit Note CN-0002 describes how to use the AD8376 VGA to drive wide bandwidth ADCs for high IF, ac-coupled applications.

CIRCUIT EVALUATION AND TEST

The circuit shown in Figure 1 is implemented using the AD9467 evaluation board (AD9467-250EBZ). The bottom side of the AD9467 evaluation board includes the ADL5562 and a prototype area for a fourth-order filter. The ADL5562 was replaced with the ADL5565 because both ADC drivers are pin compatible. See User Guide UG-200 for the complete schematics, BOM, and layout for the AD9467-250EBZ board. Table 2 shows the modifications to the AD9467 evaluation board required to duplicate the circuit shown in Figure 1. Complete documentation for this circuit note can be found in the CN-0268 Design Support package located at: http://www.analog.com/CN0268-DesignSupport.

This circuit uses the modified AD9467-250EBZ circuit board and the HSC-ADC-EVALCZ FPGA-based data capture board to run the tests. The two boards have mating high speed connectors, allowing for the quick setup and evaluation of the circuit's performance. The modified AD9467-250EBZ board contains the circuit evaluated as described in this note, and the HSC-ADC-EVALCZ data capture board is used in conjunction with VisualAnalog evaluation software, as well as the SPI controller software to properly control the ADC and capture the data.

Application Note AN-835 contains complete details on how to set up the hardware and software to run the tests described in this circuit note.

Table 2. AD9467 Evaluation Board Modification for the ADL5565 Driver Option

Reference Designator	Description	Manufacturer	Part Number
R121, R122, C109, C110, C117, R103, C116, R130, C118	DNI		
R125, R110, R107, R113, R114, R119, R120	0 Ω		
T103	Balun, 1:1 impedance ratio	M/A-Com	MABA-007159-000000
R105, R106	33 Ω		
C101, C105, C106, C107	0.1 µF		
U100	ADL5565	Analog Devices	
R117, R118	5.6 Ω		
C113, C114	1 nF		
L101, L102	39 nH	Coilcraft	0805CS
C119	8.2 pF	Murata	GRM15
L103, L104	150 nH	Coilcraft	0805CS
C120	2 pF	Murata	GRM15
L100	180 nH	Coilcraft	0805CS
R111, R112	155 Ω		
R127, R128	15 Ω		

LEARN MORE

CN-0268 Design Support Package: http://www.analog.com/CN-0268-DesignSupport

UG-200 User Guide: *Evaluating the AD9467 16-Bit, 200 MSPS/250 MSPS ADC*, Analog Devices.

CN-0002 Circuit Note, *Using the AD8376 VGA to Drive Wide Bandwidth ADCs for High IF AC-Coupled Applications*. Analog Devices

CN-0110 Circuit Note, *Using the ADL5562 Differential Amplifier to Drive Wide Bandwidth ADCs for High IF AC-Coupled Applications*, Analog Devices

CN-0227 Circuit Note, *High Performance, 16-Bit, 250 MSPS Wideband Receiver with Antialiasing Fitler*, Analog Devices.

Arrants, Alex, Brad Brannon and Rob Reeder, AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, Analog Devices.

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, *Analog Dialogue* 39-09, September 2005.

Newman, Eric and Rob Reeder. AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*. Analog Devices.

Reeder, Rob. AN-742 Application Note, *Frequency Domain Response of Switched Capacitor ADCs*. Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND."* Analog Devices.

MT-073 Tutorial, *High Speed Variable Gain Amplifiers (VGAs)*. Analog Devices.

MT-075 Tutorial, *Differential Drivers for High Speed ADCs Overview.* Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

AD9467 Data Sheet

ADL5565 Data Sheet

Circuit Evaluation Board (AD9467-250EBZ)

Standard Data Capture Platform (HSC-ADC-EVALCZ)

REVISION HISTORY

4/10—Rev. 0: Initial Version

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