High Performance 65 MHz Bandwidth Quad IF Receiver with Antialiasing Filter and 184.32 MSPS Sampling Rate

EVALUATION AND DESIGN SUPPORT
Design and Integration Files
Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS
The circuit, shown in Figure 1, is a 65 MHz bandwidth receiver front end based on the ADL5565 ultrahigh dynamic range differential amplifier driver and the 11-bit, 200 MSPS AD6657A quad IF receiver.

The fourth-order Butterworth antialiasing filter is optimized based on the performance and interface requirements of the amplifier and IF receiver. The total insertion loss due to the filter network and other resistive components is only 2.0 dB. The overall circuit has a bandwidth of 65 MHz, with the low-pass filter having a 1 dB bandwidth of 190 MHz and a 3 dB bandwidth of 210 MHz. The pass-band flatness is 1 dB.

The circuit is optimized to process a 65 MHz bandwidth IF signal centered at 140 MHz with a sampling rate of 184.32 MSPS. The SNR and SFDR measured with a 140 MHz analog input across the 65 MHz band are 70.1 dBFS and 80.9 dBc, respectively.

Figure 1. Single Channel of Quad IF Receiver Front End (Simplified Schematic; All Connections and Decoupling Not Shown) Gains, Losses, and Signal Levels Measured Values at 10 MHz
CIRCUIT DESCRIPTION

The circuit shown in Figure 1 accepts a single-ended input and converts it to differential using a wide bandwidth (3 GHz) M/A-COM ECT1-1-13M 1:1 transformer. The ADL5565 6.0 GHz differential amplifier has a differential input impedance of 200 Ω when operating at a gain of 6 dB, 100 Ω when operating at a gain of 12 dB, and 67 Ω when operating at a gain of 15.5 dB. The ADL5565 is an ideal driver for the AD6657A, and the fully differential architecture through the low-pass filter and into the ADC provides good high frequency common-mode rejection, as well as minimizes second-order distortion products. The ADL5565 provides a gain of 6 dB, 12 dB, or 15.5 dB depending on the input connection. In the circuit, a gain of 6 dB was used to compensate for the insertion loss of the filter network and the transformer (approximately 2.1 dB), providing an overall signal gain of 4.0 dB. The gain also helps minimize noise impacts from the amplifier.

The AD6657A is a quad IF receiver where each ADC output is connected internally to a digital noise shaping requantizer (NSR) block. The integrated NSR circuitry allows for improved SNR performance in a smaller frequency band within the Nyquist bandwidth.

The NSR block can be programmed to provide a bandwidth of either 22%, 33%, or 36% of the sampling rate. For the data taken in this circuit note, the sampling rate was 184.32 MSPS, and the following NSR settings applied:

- NSR bandwidth = 36%
- Tuning word (TW) = 12
- Left band edge = 11.06 MHz (input = 173.26 MHz)
- Center frequency = 44.24 MHz (input = 140.08 MHz)
- Right band edge = 77.41 MHz (input = 106.91 MHz)

Details of the operation of the NSR blocks can be found in the AD6657A data sheet.

The antialiasing filter is a fourth-order Butterworth low-pass filter designed with a standard filter design program (Agilent ADS in this case). A Butterworth filter was chosen because of its flat response. A fourth-order filter yields an ac noise bandwidth ratio of 1.03. Other filter design programs are available from Nuhertz Technologies or Quite Universal Circuit Simulator (Qucs) Simulation.

To achieve best performance, load the ADL5565 with a net differential load of at least 200 Ω. The 20 Ω series resistors isolate the filter capacitance from the amplifier output and, when added with the downstream impedance, yields a net load impedance of 249 Ω.

The 15 Ω resistors in series with the ADC inputs isolate internal switching transients from the filter and the amplifier. The 110 Ω resistors in parallel with the ADC serve to reduce the input impedance of the ADC for more predictable performance.

The measured performance of the system is summarized in Table 1, where the 3 dB bandwidth is 210 MHz. The total insertion loss of the network is approximately 2 dB. The bandwidth response of the final filter circuit is shown in Figure 4, and the SNR, SFDR performance in Figure 5.
Table 1. Measured Performance of the Circuit

<table>
<thead>
<tr>
<th>Performance Specifications at 1.75 V p-p FS</th>
<th>Final Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutoff Frequency (−1 dB)</td>
<td>190 MHz</td>
</tr>
<tr>
<td>Cutoff Frequency (−3 dB)</td>
<td>210 MHz</td>
</tr>
<tr>
<td>Pass-Band Flatness (10 MHz to 190 MHz)</td>
<td>1 dB</td>
</tr>
<tr>
<td>SNRFS at 140 MHz</td>
<td>70.1 dBFS</td>
</tr>
<tr>
<td>SFDR at 140 MHz</td>
<td>80.9 dBc</td>
</tr>
<tr>
<td>H2/H3 at 140 MHz</td>
<td>97.7 dBc/80.9 dBc</td>
</tr>
<tr>
<td>Overall Gain at 10 MHz</td>
<td>3.9 dB</td>
</tr>
<tr>
<td>Input Drive at 10 MHz</td>
<td>4.9 dBm</td>
</tr>
</tbody>
</table>

Filter and Interface Design Procedure

In this section, a general approach to the design of the amplifier/ADC interface with filter is presented. To achieve optimum performance (bandwidth, SNR, SFDR, etc.), there are certain design constraints placed on the general circuit by the amplifier and the ADC, such as:

1. The amplifier should see the correct dc load recommended by the data sheet for optimum performance.
2. The correct amount of series resistance must be used between the amplifier and the load presented by the filter. This is to prevent undesired peaking in the pass band.
3. The input to the ADC should be reduced by an external parallel resistor, and the correct series resistance should be used to isolate the ADC from the filter. This series resistor also reduces peaking.

This design approach will tend to minimize the insertion loss of the filter by taking advantage of the relatively high input impedance of most high speed ADCs and the relatively low impedance of the driving source.

Details of the design procedure can be found in the CN-0227 Circuit Note and the CN-0238 Circuit Note.

Circuit Optimization Techniques and Trade-Offs

The parameters in this interface circuit are very interactive; therefore, it is almost impossible to optimize the circuit for all key specifications (bandwidth, bandwidth flatness, SNR, SFDR, gain, etc.). However, the peaking, which often occurs in the bandwidth response, can be minimized by varying RA and RKB. Select the series resistor on the ADC inputs (RKB) to minimize distortion caused by any residual charge injection from the internal sampling capacitor within the ADC. Increasing this resistor also tends to reduce bandwidth peaking.

However, increasing RKB increases signal attenuation, and the amplifier must drive a larger signal to fill the ADC input range.

Another method for optimizing the pass-band flatness is to vary the filter shunt capacitor by a small amount.

The ADC input termination resistor (2RTADC) should normally be selected to make the net ADC input impedance between 200 Ω and 400 Ω. Making it lower reduces the effect of the ADC input capacitance and may stabilize the filter design, but increases the insertion loss of the circuit. Increasing the value will also reduce peaking.

Balancing these trade-offs can be somewhat difficult. In this design, each parameter was given equal weight; therefore, the values chosen are representative of the interface performance for all the design characteristics. In some designs, different values may be chosen to optimize SFDR, SNR, or input drive level, depending on system requirements.
The SFDR performance in this design is determined by two factors: the amplifier and the ADC interface component values, as shown in Figure 1. The final SFDR performance numbers shown in Table 1 and Figure 5 were obtained after optimizing the filter design to account for the board parasitics and nonideal components used in the filter design.

Another trade-off that can be made in this particular design is the ADC full-scale setting. The full-scale ADC differential input voltage was set for 1.75 V p-p for the data obtained with this design, which optimizes SFDR. Changing the full-scale input range to 2.0 V p-p yields a small improvement in SNR, but slightly degrades the SFDR performance. Changing the full-scale input range in the opposite direction to 1.5 V p-p yields a small improvement in SFDR but slightly degrades the SNR performance.

Note that the signal in this design is ac coupled with the 0.1 µF capacitors to block the common-mode voltages between the amplifier, its termination resistors, and the ADC inputs. Refer to the AD6657A data sheet for further details regarding common-mode voltages.

**Passive Component and PC Board Parasitic Considerations**

The performance of this or any high speed circuit is highly dependent on proper PCB layout. This includes, but is not limited to, power supply bypassing, controlled impedance lines (where required), component placement, signal routing, and power and ground planes. See the MT-031 and MT-101 tutorials for more detailed information regarding PCB layout for high speed ADCs and amplifiers.

Use low parasitic surface-mount capacitors, inductors, and resistors for the passive components in the filter. The inductors chosen are from the Coilcraft 0603CS series. The surface-mount capacitors used in the filter are 5%, C0G, 0402-type for stability and accuracy.

See the CN-0259 Design Support Package (www.analog.com/CN0259-DesignSupport) for complete documentation on the system.

**COMMON VARIATIONS**

For applications that require less bandwidth and lower power, the ADL5562 differential amplifier can be used. The ADL5562 has a bandwidth of 3.3 GHz. For even lower power and bandwidth, the ADA4950-1 could also be used. This device has a 1 GHz bandwidth and only uses 10 mA of current.

**CIRCUIT EVALUATION AND TEST**

This circuit uses the EVAL-CN0259-HSCZ circuit board and the HSC-ADC-EVALCZ FPGA-based data capture board. The two boards have mating high speed connectors, allowing for the quick setup and evaluation of the circuit’s performance. The EVAL-CN0259-HSCZ board contains the circuit evaluated as described in this note, and the HSC-ADC-EVALCZ data capture board is used in conjunction with Visual Analog evaluation software, as well as the SPI Controller software to properly control the ADC and capture the data. See the CN0259 Design Support package for the schematic, BOM, and layout files for the EVAL-CN0259-HSCZ board. Application Note AN-835 contains complete details on how to set up the hardware and software to run the tests described in this circuit note.

**LEARN MORE**

CN-0259 Design Support Package:
http://www.analog.com/CN0259-DesignSupport
UG-232: Evaluating the AD6642/AD6657 Analog to Digital Converters
Alex Arrants, Brad Brannon and Rob Reeder, AN-835 Application Note: Understanding High Speed ADC Testing and Evaluation, Analog Devices.
MT-031 Tutorial, Grounding Data Converters and Solving the Mystery of “AGND” and “DGND”, Analog Devices.
MT-101 Tutorial, Decoupling Techniques, Analog Devices.
Agilent Technologies, Advanced Design System.
Reeder, Rob, Frequency Domain Response of Switched Capacitor ADCs, AN-742 Application Note, Analog Devices.
Reeder, Rob, Achieve CM Convergence between Amps and ADCs, Electronic Design, July 2010.
Reeder, Rob, Mine These High-Speed ADC Layout Nuggets For Design Gold, Electronic Design, September 15, 2011.

**Data Sheets and Evaluation Boards**

CN-0259 Circuit Evaluation Board (EVAL-CN0259-HSCZ)
Standard Data Capture Platform (HSC-ADC-EVALCZ)
AD6657A Data Sheet
ADL5565 Data Sheet
AD6657A Evaluation Board (AD6657AEBZ)
REVISION HISTORY

8/12—Rev. A to Rev. B
Changes to Circuits from the Lab Descriptive Header ...............1

2/12—Rev. 0 to Rev. A
Changes to Figure 1.................................................................1
Changes to Circuit Description Section and Figure 3..............2
Changes to Circuit Evaluation and Test Section ......................4

1/12—Revision 0: Initial Version

(Continued from first page) Circuits from the Lab circuits are intended only for use with Analog Devices products and are the intellectual property of Analog Devices or its licensors. While you may use the Circuits from the Lab circuits in the design of your product, no other license is granted by implication or otherwise under any patents or other intellectual property by application or use of the Circuits from the Lab circuits. Information furnished by Analog Devices is believed to be accurate and reliable. However, Circuits from the Lab circuits are supplied "as is" and without warranties of any kind, express, implied, or statutory including, but not limited to, any implied warranty of merchantability, noninfringement or fitness for a particular purpose and no responsibility is assumed by Analog Devices for their use, nor for any infringements of patents or other rights of third parties that may result from their use. Analog Devices reserves the right to change any Circuits from the Lab circuits at any time without notice but is under no obligation to do so.

©2012 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.

Rev. B | Page 5 of 5