FEATURES

- 300W Full Bridge Topology
- Eliminates DC blocking capacitor
- Advanced Voltage mode Control with integrated Volt-Second Balance
- Remote voltage sensing
- Line voltage feedforward
- I2C serial interface to PC
- Software GUI
- Programmable digital filters for DCM and CCM
- 7 PWM outputs including Auxiliary PWM
- Digital Trimming
- Current, voltage, and temperature sense through GUI
- Calibration and trimming

CAUTION

This evaluation board uses high voltages and currents. Extreme caution must be taken especially on the primary side, to ensure safety for the user. It is strongly advised to power down the evaluation board when not in use. A current limited power supply is recommended as input as no fuse is present on the board.

ADP1046 EVALUATION BOARD OVERVIEW

This evaluation board features the ADP1046 in a switching power supply application. With the evaluation board and software, the ADP1046 can be interfaced to any PC running Windows 2000/XP/Vista/NT via the computer's USB port. The software allows control and monitoring of the ADP1046 internal registers. The board is set up for the ADP1046 to act as an isolated switching power supply with a rated load of 12V/25A from an input voltage ranging from a 42 to 60VDC.
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# REVISION HISTORY

10/22/2011—Revision 1.0: SPM  
11/28/2011—Revision 1.1: SPM  
08/03/2012—Revision 1.2: SPM

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BOARD SPECIFICATIONS

<table>
<thead>
<tr>
<th>Specification</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_IN</td>
<td>42</td>
<td>48</td>
<td>60</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_OUT</td>
<td>10.8</td>
<td>12</td>
<td>13.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I_OUT</td>
<td>0.0</td>
<td>25</td>
<td>25</td>
<td>A</td>
<td>With 400 LFM air flow</td>
</tr>
<tr>
<td>T_Ambient</td>
<td>0</td>
<td>50</td>
<td>50</td>
<td>ºC</td>
<td>Typical reading at 48V/25A load</td>
</tr>
<tr>
<td>Efficiency</td>
<td>0</td>
<td>93.5%</td>
<td>50</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Switching frequency</td>
<td>148.8</td>
<td>100</td>
<td>KHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage Ripple</td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
<td>At 25A load</td>
</tr>
</tbody>
</table>

Table 1 - Target Specifications

TOPOLOGY AND CIRCUIT DESCRIPTION

This application note consists of the ADP1046 in a typical DC/DC switching power supply in a full bridge topology with synchronous rectification. The circuit is designed to provide a rated load of 12V/25A from an input voltage source of 42V to 60VDC. The ADP1046 is used to provide functions such as the output voltage regulation, output over voltage and current protection, primary cycle by cycle protection, and over temperature protection.

The auxiliary power supply using transformer (T3) and IC (U10) generates 12V rails on both the primary and secondary side to power the i-couplers and MOSFET drivers. This auxiliary supply starts up at approximately 30VDC.

The primary side consists of the input terminals (JP1, JP3), switches (Q1-Q4), the current sense transformer (T1) and the main transformer (T2). The ADP1046 resides on the secondary side and is powered via the auxiliary power supply or the USB connector via the LDO (U11). The gate signal for the primary switches is generated by the ADP1046 through the i-couplers (U2, U3) and fed into the MOSFET drivers (U1, U4).

The secondary side power stage consists of the synchronous rectifiers (M1, M2, M5, M6). The RCD snubber (D2, D5, C22, C23, R17, R19, R62, R63) act as snubbers for these FETs. The secondary side FETs are driven by driver (U5). Also present on the secondary side is the output filter inductor (L3) and the output capacitors (C16-C21). Capacitor (C52) provides high frequency decoupling to lower EMI.

The primary current is sensed through the CS1 pin with a small RC time constant (R25, C25) that filters the noisy signal. The secondary current is sense across resistors (R29, R21) and fed in the CS2± pins. The output voltage can be sensed locally or remotely by removing resistors R23 and R38 and connecting Vsen+ and Vsen- to the remote sensing point on connector (JP10). Fast OVP is implemented using the VS1 pin and regulation is achieved using VS3 pin. The output voltage is divided to a nominal of 1V before feeding into the appropriate pins.

Line voltage feedforward is implemented using an RCD circuit (D3, R95, R96, C62, C64) that detects the peak voltage at the synchronous FET. There are two time constants. The time constants must be matched such that it retains the peak value during the switching frequency period but also is not too long in case there is a step down change in the input voltage. This peak voltage is further ratioed and fed in the ACSNS pin of the controller (ADP1046). A thermistor (RT1) is placed on the secondary side close to synchronous FET and acts thermal protection for the power supply. A 16.5k resistor is placed in parallel with the thermistor that allows the software GUI to read the temperature directly in degrees Celsius.

Also present on the secondary is a 4 pin connector for I2C communication. This allows the PC software to communicate with the IC through the USB port of the PC. The user can easily change register settings on the ADP1046, and monitor the status registers. It is recommended that the USB dongle be connected directly to the PC, not via external hub.

Jumper JP2 acts as a hardware PS_OFF switch. When tied to ground, the voltage reference (D10) stops sinking current, turning transistor (Q5) off, and thus the optocoupler (U7) off as well. The voltage at the PSON pin is now low and the power supply is turned off.

CONNECTORS

The following table lists the connectors on the board:
The pin outs of the USB dongle are given below:

<table>
<thead>
<tr>
<th>Pin (left to right)</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5V</td>
</tr>
<tr>
<td>2</td>
<td>SCL</td>
</tr>
<tr>
<td>3</td>
<td>SDA</td>
</tr>
<tr>
<td>4</td>
<td>Ground</td>
</tr>
</tbody>
</table>

*Table 3 - I2C connector pin out descriptions*

Figure 1 – I2C connector (pin1 on left)
SETTING FILES AND EEPROM

The ADP1046 communicates with the GUI software using the I2C bus.

![Diagram: ADP1046 and GUI interaction]

The register settings (having extension .46r) and the board settings (having extension .46b) are two files that are associated with the ADP1046 software. The register settings file contains information such as the over voltage and over current limits, softstart timing, PWM settings etc. that govern the functionality of the part. The ADP1046 stores all its settings in the EEPROM.

The EEPROM on the ADP1046 does not contain any information about the board, such as current sense resistor, output inductor and capacitor values. This information is stored in board setup file (extension .46b) and is necessary for the GUI to display the correct information in the ‘Monitor’ tab as well as ‘Filter Settings’ window. The entire status of the power supply such as the ORFET and synchronous rectifiers enable/disable, primary current, output voltage and current can be thus digitally monitored and controlled using software only. Always make sure that the correct board file has been loaded for the board currently in use.

Each ADP1046 chip has trim registers for the temperature, input current and the output voltage and current, and ACSNS. These can be configured during production and are not overwritten whenever a new register settings file is loaded. This is done in order to retain the trimming of all the ADCs for that corresponding environmental and circuit condition (component tolerances, thermal drift, etc.). A guided wizard called the ‘Auto Trim’ is started which trims the above mentioned quantities so that the measurement value matches the valued displayed in the GUI to allow ease of control through software.
BOARD EVALUATION

EQUIPMENT

• DC Power Supply (40-60V, 400W)
• Electronic Load (25A/300W)
• Oscilloscope with differential probes
• PC with ADP1046 GUI installed
• Precision Digital Voltmeters (HP34401 or equivalent - 6 digits) for measuring DC current and voltage

SETUP

NOTE: DO NOT CONNECT THE USB CABLE TO THE EVALUATION BOARD UNTIL THE SOFTWARE HAS FINISHED INSTALLING

1) Install the ADP1046 software by inserting the installation CD. The software setup will start automatically and a guided process will install the software as well as the USB drivers for communication of the GUI with the IC using the USB dongle.

2) Insert the daughter card in connector J5 as shown in Figure 4

3) Ensure that the PS_ON switch (SW1 on schematic) is turned to the OFF position. It is located on the bottom left half of the board.

4) Connect one end of USB dongle to the board and the other end to the board to the USB port on the PC using the “USB to I2C interface” dongle.

5) The software should report that the ADP1046 has been located on the board. Click “Finish” to proceed to the Main Software Interface Window. The serial number reported on the side of the checkbox indicates the USB dongle serial number. The windows also displays the device I2C address.

5. If the software does not detect the part it enters into simulation mode. Ensure that the connector is connected to J10 (on main board) or J7 (on daughter card). Click on ‘Scan for ADP1046 now’ icon (magnifying glass) located on the top right hand corner of the screen.

Figure 4 - ADP1046 address of 50h in the GUI
5. Click on the “Load Board Settings” icon (fourth button from the left) and select the ADP1046_uTCA_C_xxxx.46b file. This file contains all the board information including values of shunt and voltage dividers. Note: All board setting files have an extension of .46b.

6. The IC on the board comes preprogrammed and this step is optional. The original register configuration is stored in the ADP1046_uTCA_C_xxxx.46r register file (Note: All register files have an extension of .46r). The file can be loaded using the second icon from the left in Figure 6.

7. Connect a DC power source (48VDC nominal, current limit to ~1A) and an electronic load at the output set to 1 Ampere.

8. Connect a voltmeter on test points TP8(+) and TP4(-). Ensure that the differential probes are used and the ground of the probes are isolated if oscilloscope measurements are made on the primary side of the transformer.

9. Click on the Dashboard settings (3rd icon in Figure 5 and turn on the software PS_ON)

10. The board should now up and running, and ready for evaluation. The output should now read 12 VDC.

11. Click on the ‘MONITOR’ tab and then on the Flags and readings icon. This window provides a snapshot of the entire state of the PSU in a single user friendly window.
Figure 7 - Monitor window in GUI showing entire status of the PSU
BOARD SETTINGS

The following screenshot displays the board settings.

![Board Settings Screenshot](image)

**THEORY OF OPERATION DURING STARTUP**

The following steps briefly describe the startup procedure of the ADP1046 and the power supply and the operation of the state machine for the preprogrammed set of registers that are included in the design kit.

1. After VDD (3.3V) is applied to the ADP1046 it takes approximately 20µs for VCORE to reach 2.5V. The digital core is now activated and the contents of the registers are downloaded in the EEPROM. The ADP1046 is now ready for operation.

2. PS_ON is applied. The power supply begins the programmed softstart ramp of 40ms (programmable).

3. Since the 'softstart from pre-charge' setting is active the output voltage is sensed before the softstart ramp begins. Depending upon the output voltage level of the effective softstart ramp is reduced by the proportional amount.

4. The PSU now is running in steady state. PGOOD1 turns on after the programmed debounce.

5. If a fault is activated during the softstart or steady state, the corresponding flag will be set and the programmed action will be taken such as disable PSU and re-enable after 1 sec, Disable SR and OrFET, Disable OUTAUX etc.
FLAGS SETTINGS CONFIGURATIONS

Basically when a flag is triggered, the ADP1046 state machine waits for a programmable debounce time before taking any action. The response to each flag can be programmed individually. The flags can be programmed in a single window by hitting the FLAG SETTINGS icon in the MONITOR tab in the GUI. This monitor window shows all the fault flags (if any) and the readings in one page. The ‘Get First Flag’ button determines the first flag that was set in case of a fault event.
PWM SETTINGS

The ADP1046 has a fully programmable PWM setup that controls 7 PWMs. Due to this flexibility the IC can function in several different topologies such as any isolated buck derived topology, push pull, flyback and also has the control law for resonant converters.

The integrated volt-second balance feature is used as a current balancer of the two legs of the full bridge topology.

Each PWM edge can be moved in 5ns steps to achieve the appropriate deadtime needed and the maximum modulation limit sets the maximum duty cycle.

<table>
<thead>
<tr>
<th>PWM</th>
<th>Switching element being controlled</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUTA-OUTD</td>
<td>Primary switch PWM</td>
</tr>
<tr>
<td>SR1-SR2</td>
<td>Synchronous rectifier PWMs</td>
</tr>
<tr>
<td>OUTAUX</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Table 4—PWMs and their corresponding switching element
BOARD EVALUATION AND TEST DATA

STARTUP

Figure 11 - Startup at 42V/DC, no load
Green trace: Output voltage, 2V/div, 10ms/div
Yellow trace: Load current, 5A/div, 10ms/div

Figure 12 - Startup at 60V/DC, 25A load (2A/us slew rate)
Green trace: Output voltage, 2V/div, 10ms/div
Yellow trace: Load current, 5A/div, 10ms/div

Figure 13 - Softstart from precharge at no load (zoom in)
Green trace: Output voltage, 2V/div, 50ms/div
Blue trace: Load current, 10A/div, 50ms/div

Figure 14 - Softstart from precharge at no load (zoom out)
Green trace: Output voltage, 2V/div, 500ms/div
Blue trace: Load current, 10A/div, 500ms/div
PRIMARY GATE DRIVER DEADTIME

Figure 15 – Gate voltage at OUTB and OUTD
Blue and Green trace: 1us/div, 5V/div

Figure 16 – Gate voltage at OUTB and OUTD (Zoomed In)
Blue and Green trace: 200ns/div, 5V/div
CS1 PIN VOLTAGE (PRIMARY CURRENT)

Figure 17 – CS1 pin voltage at 25A load, 42VDC, current balancing enabled
Blue trace: Voltage at CS1, 500mV/div, 2us/div

Figure 18 – CS1 pin voltage at 25A load, 350VDC, current balancing disabled
Blue trace: Voltage at CS1, 500mV/div, 2us/div

Figure 19 – CS1 pin voltage at 25A load, 48VDC, Volt-Sec balance disabled
Blue trace: Voltage at CS1, 500mV/div, 2us/div

Figure 20 – CS1 pin voltage at 25A load, 48VDC, Volt-Sec balance enabled
Blue trace: Voltage at CS1, 500mV/div, 2us/div
SYNCHRONOUS RECTIFIER PEAK INVERSE VOLTAGE

**Figure 21** – Synchronous rectifier MOSFET PIV at 25A load, 12VDC
Blue trace: Synchronous rectifier 1, 20V/div, 1us/div
Green trace: Synchronous rectifier 2, 20V/div, 1us/div

**Figure 22** – Synchronous rectifier MOSFET PIV at 25A load, 60VDC
Blue trace: Synchronous rectifier 1, 20V/div, 1us/div
Green trace: Synchronous rectifier 2, 20V/div, 1us/div

OUTPUT RIPPLE

**Figure 23** – Output voltage AC coupled (without 1000uF electrolytic capacitor)
42VDC, 25A, 50mV/div, 2us/div. High frequency component.

**Figure 24** – Output voltage AC coupled (without 1000uF electrolytic capacitor)
42VDC, 25A, 50mV/div, 2us/div. Low frequency component.
Figure 25 – Output voltage AC coupled (without 1000uF electrolytic capacitor)
60VDC, 25A, 50mV/div, 2us/div. High frequency component.

Figure 26 – Output voltage AC coupled (without 1000uF electrolytic capacitor)
60VDC, 25A, 50mV/div, 5ms/div. Low frequency component.

Figure 27 – Output voltage at no load (with pulse skipping) AC Coupled (without 1000uF electrolytic capacitor)
42VDC, 25A, 50mV/div, 20ms/div. High frequency component.

Figure 28 – Output voltage at no load (with pulse skipping) AC Coupled (without 1000uF electrolytic capacitor)
60VDC, 25A, 20mV/div, 20ms/div. High frequency component.
TRANSIENT VOLTAGE AT 48VDC (NOMINAL VOLTAGE)

LOAD STEP OF 0-25%

Figure 29 – Output voltage transient, 0-25% load (without 1000uF electrolytic capacitor)
Yellow trace: Load current, 5A/div, 100us/div
Green trace: Output voltage (AC coupled), 200mV/div, 100us/div

Figure 30 – Output voltage transient, 25-0% load (without 1000uF electrolytic capacitor)
Yellow trace: Load current, 5A/div, 100us/div
Green trace: Output voltage (AC coupled), 200mV/div, 100us/div

LOAD STEP OF 25-50%

Figure 31 – Output voltage transient, 25-50% load (without 1000uF electrolytic capacitor)
Yellow trace: Load current, 5A/div, 100us/div
Green trace: Output voltage (AC coupled), 200mV/div, 100us/div

Figure 32 – Output voltage transient, 50-25% load (without 1000uF electrolytic capacitor)
Yellow trace: Load current, 5A/div, 100us/div
Green trace: Output voltage (AC coupled), 200mV/div, 100us/div
LOAD STEP OF 50-75%

Figure 33—Output voltage transient, 50-75% load (without 1000uF electrolytic capacitor)
Yellow trace: Load current, 5A/div, 100us/div
Green trace: Output voltage (AC coupled), 200mV/div, 100us/div

Figure 34—Output voltage transient, 75-50% load (without 1000uF electrolytic capacitor)
Yellow trace: Load current, 5A/div, 100us/div
Green trace: Output voltage (AC coupled), 200mV/div, 100us/div
LOAD STEP OF 75-100%

Figure 35 – Output voltage transient, 75-100% load (without 1000uF electrolytic capacitor)
Yellow trace: Load current, 10A/div, 100us/div
Green trace: Output voltage (AC coupled), 200mV/div, 100us/div

Figure 36 – Output voltage transient, 75-100% load (without 1000uF electrolytic capacitor)
Yellow trace: Load current, 10A/div, 100us/div
Green trace: Output voltage (AC coupled), 200mV/div, 100us/div

LOAD STEP 0-25A

Figure 37 – Output voltage transient, 0-100% load (without 1000uF electrolytic capacitor)
Yellow trace: Load current, 10A/div, 100us/div
Green trace: Output voltage (AC coupled), 1V/div, 100us/div

Figure 38 – Output voltage transient, 100-0% load (without 1000uF electrolytic capacitor)
Yellow trace: Load current, 10A/div, 100us/div
Green trace: Output voltage (AC coupled), 200mV/div, 100us/div
FEEDFORWARD

Figure 39 – Line Feedforward at 0A load
Red trace: Input voltage step 42-60V, 10V/div, 200us/div
Green trace: Output voltage (AC coupled) 500mV/div, 200us/div

Figure 40 – Line Feedforward at 0A load
Red trace: Input voltage step 60-42V, 10V/div, 200us/div
Green trace: Output voltage (AC coupled), 500mV/div, 200us/div

OUTPUT OVER CURRENT PROTECTION

Figure 41 – Output short circuit protection
Response set to disable PSU and re-enable after 1 sec.
Yellow trace: Load current, 20A/div, 500mV/div
Green trace: Output Voltage, 5V/div, 500ms/div
CLOSED LOOP FREQUENCY RESPONSE

A network analyzer (AP200) was used to test the bode plots of the system. A continuous noise signal of 300mV was injected across the entire frequency range across R35 using an isolation transformer with R38 shorted. The operating condition was 48VDC input and a load condition of 25A.

<table>
<thead>
<tr>
<th>Data</th>
<th>f1</th>
<th>f2</th>
<th>f3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>19.93 kHz</td>
<td>36.22 kHz</td>
<td>16.29 kHz</td>
</tr>
<tr>
<td>Magnitude</td>
<td>-0.001 dB</td>
<td>-0.001 dB</td>
<td>-0.001 dB</td>
</tr>
<tr>
<td>Phase</td>
<td>5.1 deg</td>
<td>0.001 deg</td>
<td>-51.001 deg</td>
</tr>
</tbody>
</table>

![Bode Plot](image)

Figure 42 – Bode Plots, 48VDC input, 25A load, with 1000uF/16V electrolytic capacitor on output

- Blue trace: Gain in dB
- Red trace: Phase in degrees
- Crossover frequency = 19.93kHz
- Phase margin = 51°
- Gain Margin = 4.6dB
EFFICIENCY

Figure 43 – Efficiency vs Load

CS1 LINEARITY

Figure 44 – CS1 Linearity
ACSNS LINEARITY

![Graph of ACSNS linearity vs load](image)

Figure 45—ACSNS linearity vs load

CS2 LINEARITY

![Graph of CS2 linearity vs load](image)

Figure 46—CS2 linearity vs load
THERMAL TEST DATA

A thermal snapshot of the unit was taken after running at 25A for 1 hour of soaking time with air flow of 200LFM.

Figure 48 – Thermal data at 48V input, 12V, 25A output.
Figure 49 – Schematic – Primary side
Figure 50 – Schematic – Secondary side

Figure 51 – Schematic – Auxiliary power supply
Figure S2 – Schematic – ADP1046 controller schematic

Figure S3 – Schematic – On/Off Schematic
APPENDIX IV – LAYOUT

The layout of the board was done on 14 layers with 3 ounce copper on the external layers. Some of the layers are shown below.