

DESIGN NOTES

A Low Power, Direct-to-Digital IF Receiver with Variable Gain

Design Note 482

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Introduction

Modern communication receivers require an ADC to digitize an incoming analog signal for decoding in a suitable FPGA device. The direct-conversion method of receiver design typically performs a single frequency downconversion and an analog-to-digital conversion (ADC) near baseband. While elegant and simple, this receiver architecture has problems with in-band blockers, out-of-band interferers and LO leakage reflections within the receiver itself.

In the face of these problems, basestation receivers often require a robust solution that is achieved using tried-and-true system methods of downconversion to an intermediate frequency (IF) in the range of 70MHz to 240MHz. Demodulating and decoding the IF signal can be performed by various means, but an increasingly popular and cost-effective method is direct-to-digital IF conversion using the recent generation of high speed, low power pipeline data converters available from Linear Technology.

This design note describes a variable gain amplifier plus analog-to-digital converter (VGA + ADC) combination circuit that preserves the IF receiver dynamic range over a 31dB gain adjust range and effectively demodulates and digitizes both the I and Q information in a single step. The combination LTC®6412 VGA and LTC2261 14-bit ADC circuit subsamples a 140MHz WCDMA IF channel at 125Mps and provides an equivalent input NF and IP3 that rivals some of the best laboratory spectrum analyzers, while consuming less than 0.5W of power.

IF Receiver Performance

The performance of a demonstration receiver circuit is shown in Figure 1. The inset graph of Figure 1 shows the noise-like distribution of the WCDMA signal and is similar to CCDFs of other modern communication signals. At VGA maximum gain, the signal generator power is adjusted to $-12.5\text{dBFS}_{\text{RMS}}$ to occupy most of the ADC code range without clipping.

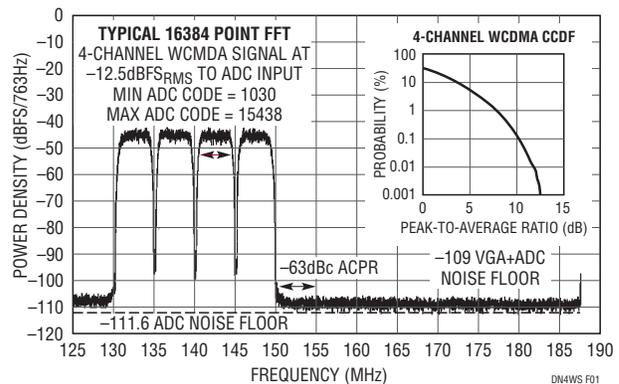


Figure 1. Typical WCDMA Performance at $-12.5\text{dBFS}_{\text{RMS}}$ over All Gain Adjust Settings. Inset Shows WCDMA CCDF

As the input signal power is adjusted higher, the VGA gain is adjusted down to maintain $-12.5\text{dBFS}_{\text{RMS}}$ and simulate the automatic gain control (AGC) response of a typical receiver. The FFT of the digitized receive signal is plotted over a full Nyquist zone and exhibits a 63dBc ACPR with no measurable spurs and only 2.6dB degradation in the ADC noise floor, over the full 31dB gain adjust range. This represents an effective input NF of 13dB and input IP3 of 23dBm for the VGA + ADC pair at 140MHz at maximum gain. The (IP3-NF) delta of 10dBm determines the effective dynamic range of the receive pair and is nearly constant over the entire gain adjust range.

Measurement Details and Receiver Circuit

An Agilent E4436B source generates the multichannel WCDMA test signal with a typical adjacent channel power ratio (ACPR) of 50dBc to 55dBc, perfectly adequate to meet the WCDMA system specifications but insufficient to demonstrate the full quality of this VGA + ADC combination. The test signal is amplified with a high linearity Triquint AH202 and sharply filtered with a SAWTEK 854920 to reduce the test signal's ACPR skirts below 65dBc.

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The WCDMA signal is representative of the wideband, noise-like signals found in modern communication systems such as LTE, 802.11g, and WiMAX to name a few. Interestingly, this convergence of statistical signal behavior was predicted over 60 years ago in Claude Shannon's communication theory. He found that the methods to increase spectral efficiency in a modulation format will, by necessity, exercise many degrees of freedom in signal space and approximate the process of additive white Gaussian noise. This was an amazing insight considering the simple AM and FM signals of Shannon's day. This is also a practical insight. One representative noise-like signal can be used to characterize an RF receiver and estimate the performance of other noise-like signals.

Figure 2 details a receiver circuit optimized for a 140MHz center frequency and a 20MHz bandwidth typical of a 4-channel WCDMA signal. The filtered test signal feeds to the VGA input balun to perform a single-ended to differential conversion at the input of the LTC6412. The LTC6412 output connects to a simple tank circuit and RC network at the input of the LTC2261. This matching circuit routes bias current to the VGA while performing a low Q impedance transformation to the 100Ω differential load. The matching circuit and RC load also serve to dissipate the differential and common mode charge injections emanating from the sampling switches at the

ADC input. This is an important consideration, as these charge impulses need to dampen to better than -85dB during a sampling window (4ns) to preserve the full spur-free dynamic range (SFDR) of the LTC2261. The better damping circuits tend to be small and tight to avoid unnecessary reflection delays and mismatch between the VGA output and ADC input. This particular matching circuit uses 0402 components for most elements and fits inside a board area of 5mm x 10mm.

The balance of connections to the VGA and ADC follow the recommendations of their respective data sheets. The LTC2261 14-bit ADC runs off 1.8V and consumes 127mW at 125Msps. The LTC6412 VGA runs off 3.3V and consumes 360mW for a total power consumption of 490mW.

Conclusion

The LTC6412 VGA drives the LTC2261 14-bit ADC with little compromise in the ADC performance. The VGA buffers the ADC sampling input and provides 31dB of gain adjust to expand the effective dynamic range of the subsampling IF receiver. The LTC2261 is part of a family of 12- and 14-bit low power data converters designed for maximum sampling rates in the range of 80Msps to 125Msps. For complete schematics of this receiver, visit the LTC6412 or LTC2261 product pages at www.linear.com.

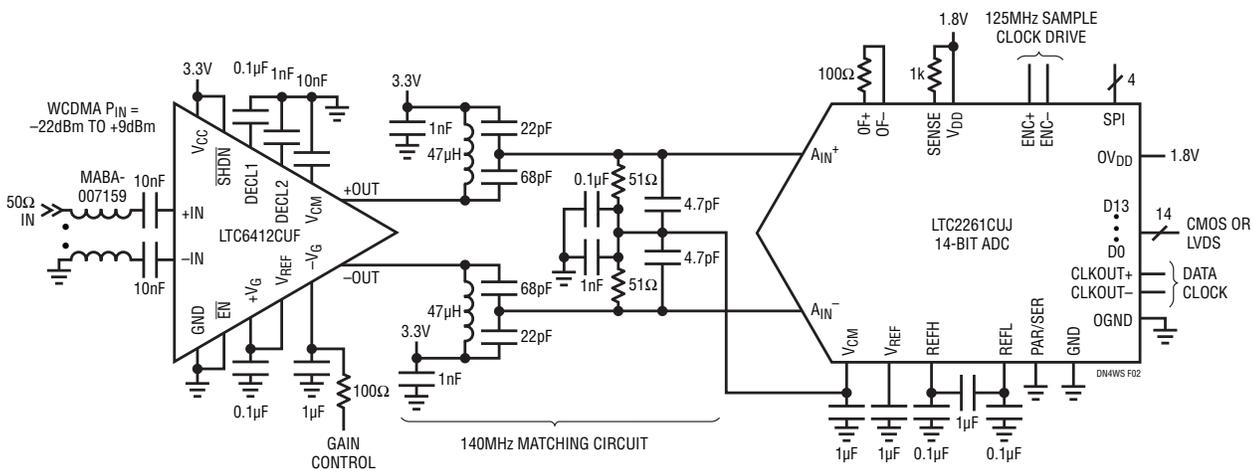


Figure 2. VGA + ADC IF Receiver Circuit. Supply Decoupling Capacitors to the VGA and ADC Omitted for Clarity. For This Measurement, the LVDS Bus Connects to Linear's Data Acquisition Board DC890B for Computer Control and Data Analysis

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