LINEAR TECHNOLOGY

DESIGN NOTES

A Single Supply RS232 Interface for Bipolar A to D Converters

Design Note 29

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Designing circuitry for single supply operation is often an attractive simplification for reducing production costs. Yet many applications call for just a few additional supplies to solve simple interface problems. The example presented here describes how an advanced RS232 interface can simplify an A to D converter which processes bipolar signals.

The LT®1180 RS232 transceiver includes a charge pump which produces low ripple supplies with sufficient surplus current to drive a CMOS A to D converter and precision voltage reference. The circuit in Figure 1 operates from a single 5V supply, and draws a total quiescent current of only 37mA. These features make the circuit ideal for applications which must process bipolar signals with minimal support electronics.

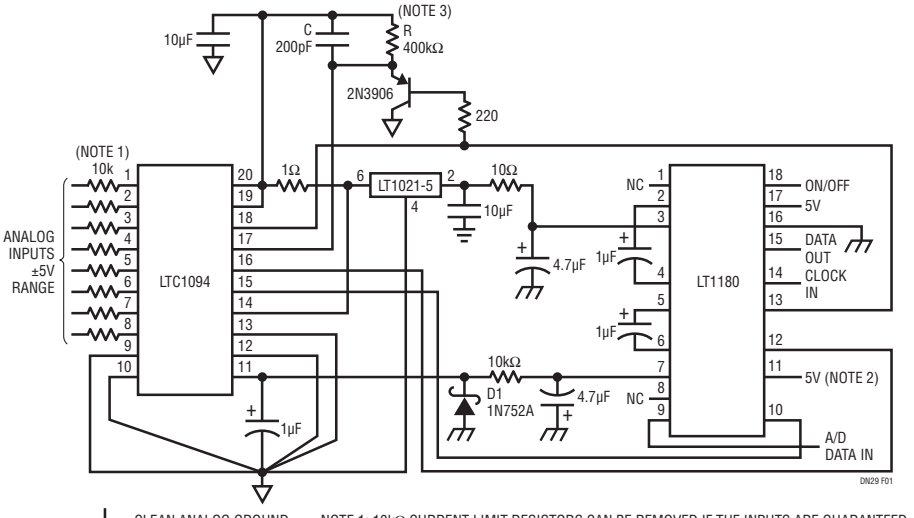
The LTC1094 serial A to D converter requires both a low noise supply and reference voltage for accurate operation.[1] These design problems are solved with an LT1021 precision reference, which delivers a stable, low noise, 5V signal from the LT1180's V+ output. Relatively large storage and filter capacitors must be used with the LT1180 to reduce the noise in the system below 1mV for a 12-bit system. Construction also requires close attention to the layout of the system grounds and other aspects of circuit board design to avoid noise problems.[2]

To accommodate bipolar inputs ($-5 < V_{IN} < 5$), the LTC1094's negative rail must be biased beyond the extreme signal swing, but below absolute maximum ratings for supplies. A 5.6V Zener diode, D1, provides a sufficient bias because the V^- pin draws very little current.

The A to D converter communicates with a remote controller via three wires, which carry the clock, the configuration word, and the output data. The chip select signal, $\overline{CS}$, is generated from the incoming clock with a peak detector, constructed with a single PNP transistor. R and C are designed to hold the $\overline{CS}$ pin low for at least one clock period.

Note 1: Refer to the data sheets for the LTC1094/LTC1294.

Note 2: An excellent reference on the subject of grounding and low noise circuit design is: "An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for A Change," by Paul Brokaw, Analog Devices Application Note.



NOTE 1: 10kΩ CURRENT LIMIT RESISTORS CAN BE REMOVED IF THE INPUTS ARE GUARANTEED NOT TO EXCEED THE LT1094's SUPPLY VOLTAGES.
NOTE 2: DRIVER OUTPUTS CAN BE PARALLEL FOR GREATER CURRENT DRIVE.
NOTE 3: SELECT RC = $4T_{CLOCK}$. MINIMIZE C.

Figure 1. A/D Converter Interface

Assuming the logic threshold in the LTC1094 is 1.4V, two useful rules of thumb for selecting R and C are: Design RC to be at least four times the clock period. And select C as small as possible to start the converter quickly. Minor aberrations in the $\overline{CS}$ signal are unimportant because the $\overline{CS}$ pin is level sensitive. The PNP is biased from the clean reference supply so very little noise is coupled into the A to D. Additional buffers are unnecessary because the peak detector drives a CMOS input.

The operating sequence for the LTC1094 is shown in Figure 2. The $\overline{CS}$ signal switches to a low state less than 1µs after receiving the system clock, and the configuration word may be transmitted after one clock cycle. After the 18 clock cycles required to complete the conversion, the clock must shut off to allow $\overline{CS}$ to switch to a high state for at least 2µs — the minimum time between conversions. The operating sequence may then be repeated.

A single conversion cycle is shown in Figure 3. The LT1180's maximum data rate limits the clock speed to 100k baud. The input voltage is 3.33V which generates a bit pattern of alternating 1's and 0's. Trace B shows the Chip Select signal, and Trace C shows the gating pulse for the system clock. The complete conversion cycle for a 12-bit converter using an LTC1294 is listed in Figure 4. For this example, the gating signals are adjusted to allow for the two extra bits of data.[3]

Note 3: The LTC1094 in Figure 1 was directly replaced with an LTC1294, with no changes to the circuit.

MSB First Data (MSPF = 1)

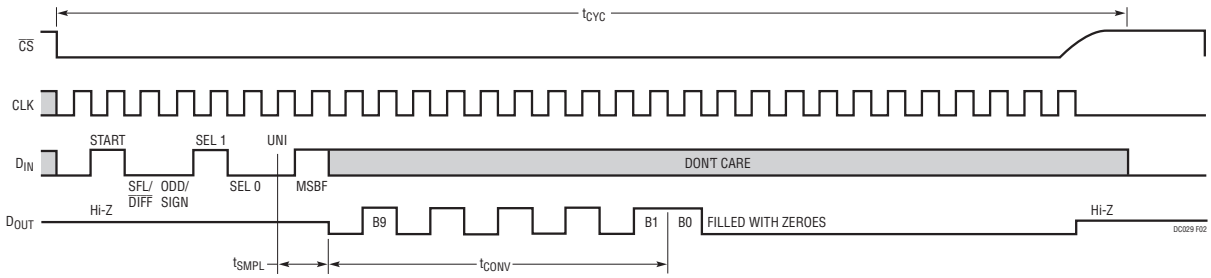


Figure 2. LTC1093/4 Operating Sequence Example: Differential Inputs (CH4+, CH5–), Bipolar Mode

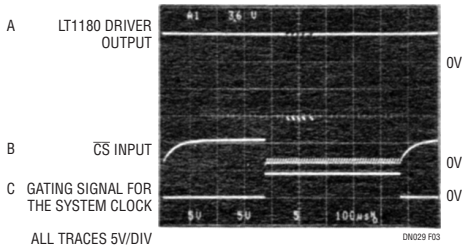


Figure 3. 10-Bit Converter Interface

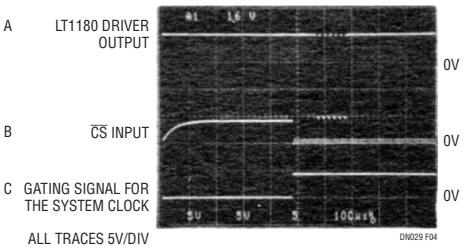


Figure 4. 12-Bit Converter Interface

Data Sheet Download

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