

DESIGN NOTES

Programming Pulse Generators for Flash Memories

Design Note 17

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Recently introduced “flash” memories add electrical chip-erase and reprogramming to established EPROM technology. These features make them a cost effective and reliable alternative for updatable non-volatile memory. Utilizing the electrical program-erase capability requires linear circuitry techniques. The Intel 28F256 flash memory, built on the ETOX process, specifies programming operation with 12V or 12.75V (faster erase/program times) amplitude pulses. These “V_{PP}” amplitudes must fall within 1.6%, and excursions beyond 14.0V will damage the device.

Providing the V_{PP} pulse requires generating and controlling high voltages within the tightly specified limits. Figure 1’s circuit does this. When the V_{PP} command pulse goes low (trace A, Figure 2) the LT[®]1072 switching regulator drives L1, producing high voltage. DC feedback occurs via R1 and R2, with AC roll-off controlled by C1 and R3-C2. The result is a smoothly rising V_{PP} pulse (trace B) which settles to the required value. The specified R1 values allow either 12V or 12.75V outputs. The 5.6V zener permits the output to return to 0V when the V_{PP} command goes high. It may be deleted in cases where a 4.5V minimum output is acceptable (see Intel 28F256 data sheet). The 0.1% resistors combine with the LT1072’s tight internal reference to eliminate circuit

trimming requirements. Additionally, this circuit will not spuriously overshoot during power-up or down.

Figure 1’s repetition rate is limited because the regulator must fully rise and settle for each V_{PP} command. Figure 3’s circuit serves cases which require higher repetition rate V_{PP} pulses. Here, the switching regulator runs continuously, with the V_{PP} pulses generated by the A1-A2 loop. If desired, the “V_{PP} Lock” line can be driven, shutting down the regulator to preclude any possibility of inadvertent V_{PP} outputs. When V_{PP} Lock goes low (trace A, Figure 4) the LT1072 loop comes on (trace B), stabilizing at about 17V. Pulsing the V_{PP} command line low causes the 74C04 (trace C) to bias the LT1004 reference. The LT1004 clamps at 1.23V with A1 and A2 giving a scaled output (trace D). The 680pF capacitor controls loop slewing, eliminating overshoots. Figure 5 details the V_{PP} output. Trace A is the 74C04 output, with trace B showing clean V_{PP} characteristics. As in Figure 1, spurious V_{PP} outputs are suppressed during power-up or down. The diode path around A2 prevents overshoot during short circuit recovery.

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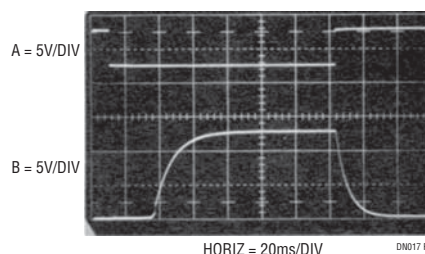
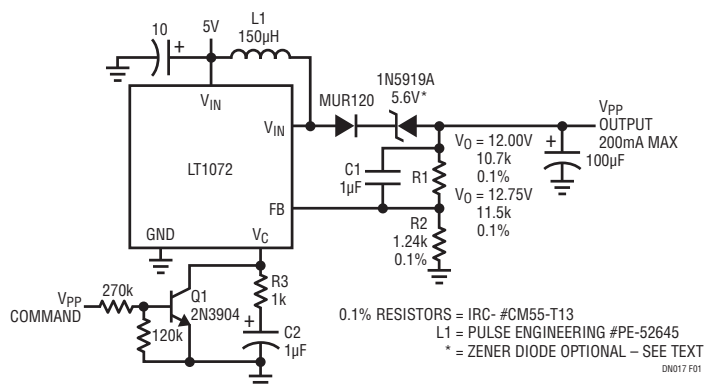


Figure 1. Basic Flash Memory V_{PP} Pulse Generator

Figure 2. Waveforms for Basic Flash Memory Pulser

A good question might be; “Why not set the switching regulator output voltage at the desired V_{PP} level and use a simple low resistance FET or bipolar switch?” Figure 6 shows that this is a potentially dangerous approach. Figure 6a shows the clean output of a low resistance switch operating directly at the V_{PP} supply. The PC trace run to the memory chip looks like a transmission line with ill-defined termination characteristics. As such, Figure 6a’s clean pulse degrades and rings badly (Figure 6b) at the memory IC’s pins. Overshoot exceeds 20V, well beyond the 14V destruction level. The controlled edge times of the circuits discussed eliminate this problem. Further discussion of these and other circuits appears in LTC Application Note 31, “Linear Circuits for Digital Systems” (Available February, 1989).

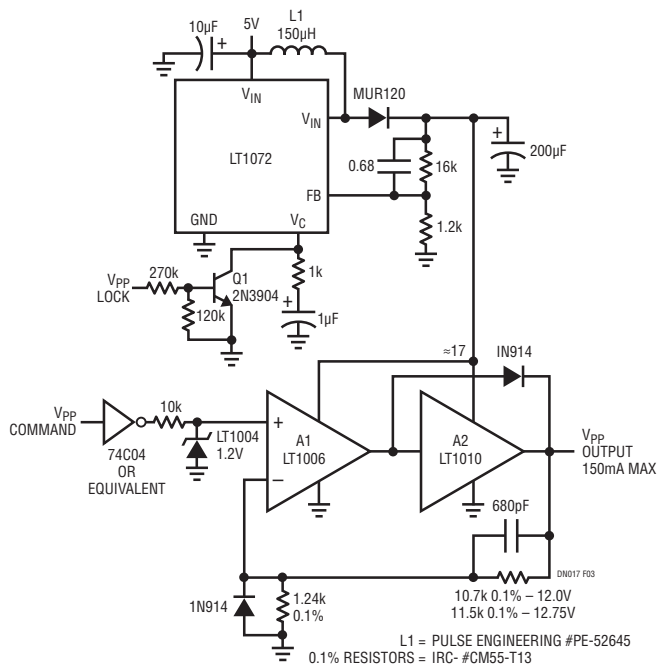


Figure 3. High Repetition Rate V_{PP} Pulse Generator

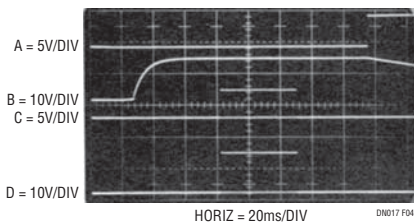


Figure 4. Operating Details of High Repetition Rate Flash Memory Pulser

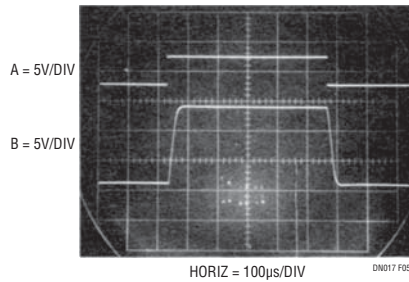


Figure 5. Expanded Scale Display of Figure 3’s V_{PP} Pulse. Controlled Risetime Eliminates Overshoots.

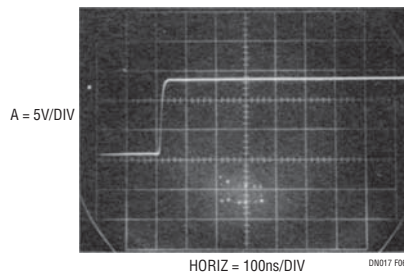


Figure 6a. An “Ideal” Flash Memory V_{PP} Pulse

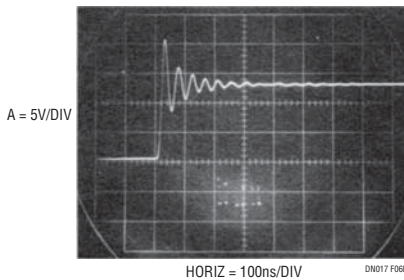


Figure 6B. Rings at Destructive Voltages After a PC Trace Run

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