

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	31MAR25	F. Gonzales

ADP1074ACCZ-1/16THBRICK-PROTO2

60W ACTIVE CLAMP FLYBACK CONVERTER

Vin Range: 48 +/- 10%

Vout Range: 30V to 60V

Solution Size: 1/16th Brick, Standard DOSA Size 33mmx22.9mmx7mm (L x W x H)

Orange highlighted notes are for the schematic reviewer
Red highlighted notes are for the PCB engineer

D

D

C

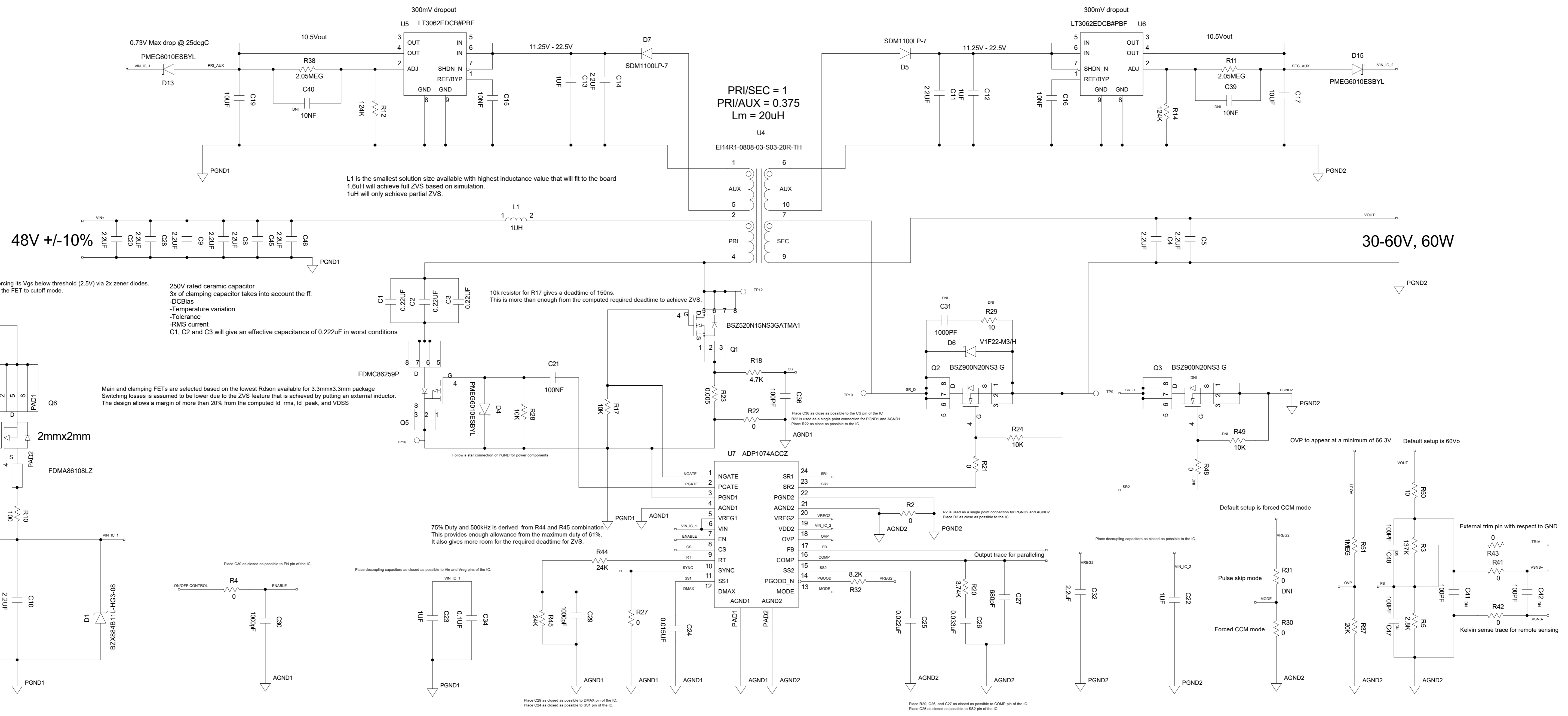
C

B

B

A

A



L1 is the smallest solution size available with highest inductance value that will fit to the board
1.6uH will achieve full ZVS based on simulation.
1uH will only achieve partial ZVS.

250V rated ceramic capacitor
3x of clamping capacitor takes into account the ff:
-DC Bias
-Temperature variation
-Tolerance
-RMS current
C1, C2 and C3 will give an effective capacitance of 0.222uF in worst conditions

Main and clamping FETs are selected based on the lowest Rds(on) available for 3.3mmx3.3mm package
Switching losses is assumed to be lower due to the ZVS feature that is achieved by putting an external inductor.
The design allows a margin of more than 20% from the computed Id_rms, Id_peak, and VDSS

75% Duty and 500kHz is derived from R44 and R45 combination
This provides enough allowance from the maximum duty of 61%.
It also gives more room for the required deadtime for ZVS.

Default setup is forced CCM mode

Pulse skip mode

Forced CCM mode

OVP to appear at a minimum of 66.3V

Default setup is 60V

External trim pin with respect to GND

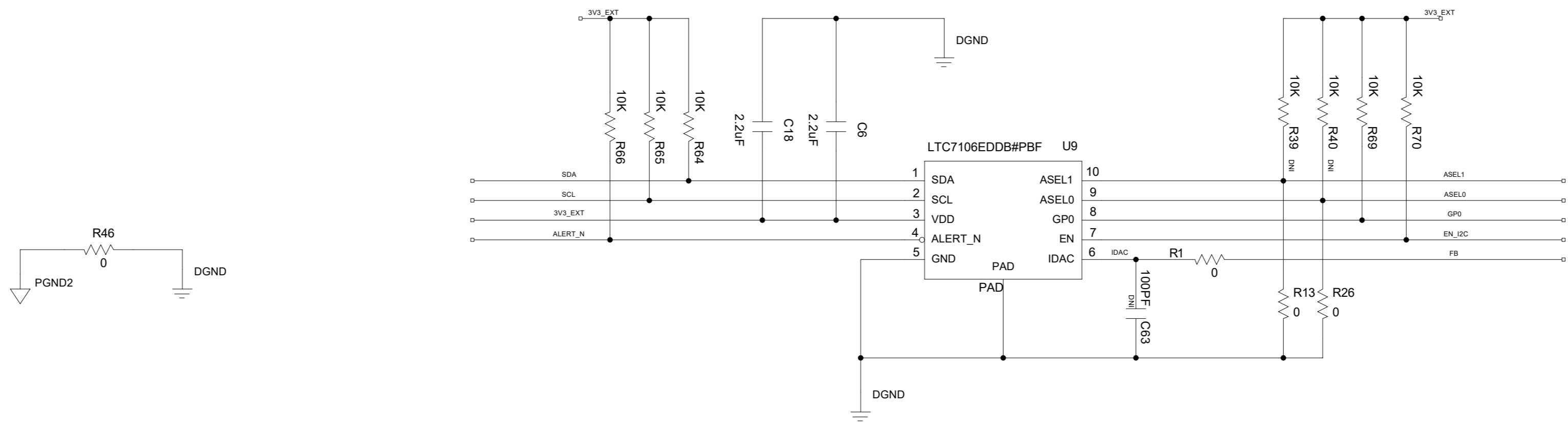
Kelvin sense trace for remote sensing



SCHEMATIC			
HW TYPE : Customer Evaluation		Product(s) : ADP1074ACCZ-1/16th BRICK-PROTO2	
DESIGN VIEW		DRAWING NO. 02_086268	
\$DESIGN_VIEW		REV A	
PTD ENGINEER		SIZE D	SCALE 1:1
		SHEET 2 OF 5	

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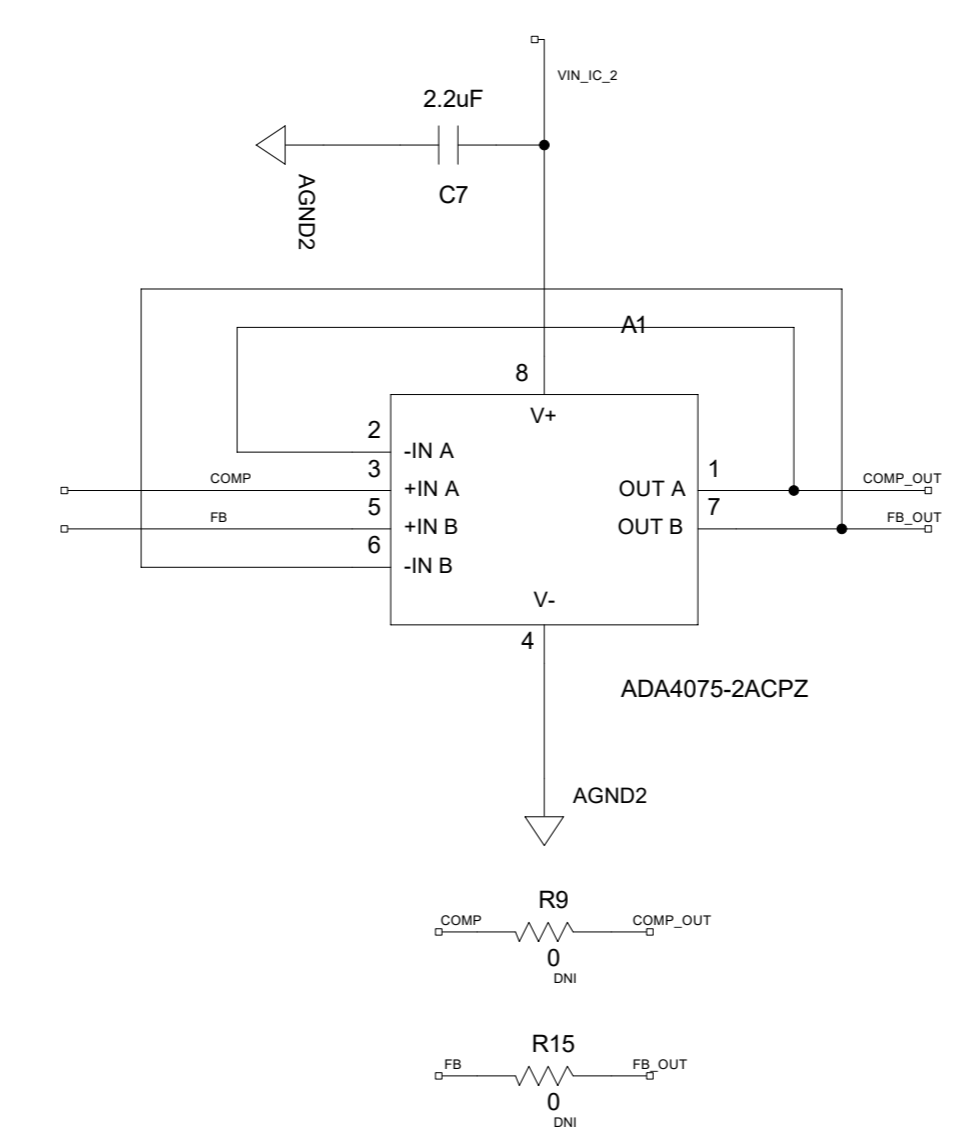
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PMBUS Interface for output voltage adjustment

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	HW TYPE : Customer Evaluation Product(s): ADP1074ACCZ-1/16th BRICK-PROTO2 : N/A		
	DESIGN VIEW \$DESIGN_VIEW	DRAWING NO. 02_086268	REV A
	PTD ENGINEER -	SIZE D	SCALE 1:1
		SHEET 3 OF 5	

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Master: A1 (P/N:ADA4075 – Do not Install)
R9 (0 OHM 0201) - Install
R15 (0 OHM 0201) - Install


Slave: A1 (P/N:ADA4075 – Install)
R9 (0 OHM 0201) - Do not Install
R15 (0 OHM 0201) - Do not Install

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	: N/A		
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\$DESIGN_VIEW	02_086268	A	
PTD ENGINEER	SIZE	SCALE	SHEET 4 OF 5
-	D	1:1	

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Other notes for the PCB engineer:

1. Allow proper creepage and clearance according to international standard specially for the 60Vdc and 120V switching rails.
2. Use short and wide traces for high current path (2Arms max for input and output).
3. Minimize the parasitic inductances on high di/dt traces. This is located on the switchng components. Use wider and shorter traces to minimize the loop inductance. You may further put GND planes over/under these traces to minimize parasitic inductance. Keep power loop as small as possible to minimize the switch node voltage ringing caused by the parasitic inductance.
4. Minimize parasitic capacitances on high dv/dt traces. This is located across VDS of power FETs. Minimize the surface area of these traces to lower the parasitic capacitance. Do not put GND plane over or underneath this node. Keep the copper area small, but large enough to handle the load current. Keep components or sensitive traces away from the high dv/dt traces.
5. Place the input ceramic capacitors as close as possible to the IC Vin and PGND pins. Place ceramic decoupling capacitors in the same side of the PCB as the IC and as close as possible to the pin.
6. Make a separate island for AGND and terminate all parts with sensitive signals on this plane (FB, SS, COMP, RT, Dmax, CS, MODE). Connect this plane in only one connection to PGND. The single point connection must be closed as possible to the AGND and PGND pins of the controller ADP1074. Make an isolation/cutout around AGND to other layers from PGND. Do not route noisy traces close to and underneath the AGND trace.
7. Place sensitive components away from the switching traces.
8. Have solid ground planes to better spread heat across the layer. Add thermal vias to thermal PGND to better spread heat to other layers. **DO NOT USE THE SWITCH NODES FOR THERMAL COOLING.**

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