

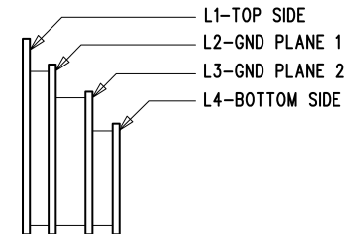
TOP SOLDER MASK  
LINEAR TECHNOLOGY  
PSRR LAB BOARD

DATE: 11-20-14

REVISION HISTORY				
ECO	REV	DESCRIPTION	APP. ENG.	DATE
-	1	1ST PROTOTYPE		11-20-14

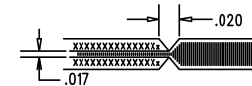
PRODUCTION


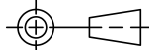
### LAYER STRUCTURE



### NOTES: UNLESS OTHERWISE SPECIFIED

- FAB PER IPC-A-600.
- MATERIAL: -EPOXY FIBERGLASS, NEMA GRADE FR-4  
-FINISHED THICKNESS TO BE 0.062" +/- .005"  
-TOTAL OF 4 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS  
AND 1 OZ. CU ON THE INNER LAYERS.  
-FLAMMABILITY RATING: 94 V-0 MINIMUM.
- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.  
0.00" ARE PRIMARY DATUMS.
- DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH  
HOLES WITH COPPER, 0.001" THICK MIN.  
-ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.  
-HOLE LOCATION TOLERANCES ARE +/-0.003"  
IN RELATION TO CENTER  
-FOR VIAS SIZE > 0.01", VIAS HOLES NEED TO BE PLUGGED  
AND COVERED WITH SOLDERMASK.
- FINISH: -SMOBC USING LPI BOTH SIDES, COLOR BLACK.  
-GOLD IMMERSION BOTH SIDES.  
(LEAD FREE SOLDER CAN BE USED FOR PROTOTYPE)  
-FOR SILKSCREEN: BOTH SIDES USE WHITE NON-CONDUCTIVE INK.
- DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE.  
PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
- PCBS ARE TO BE RoHS COMPLIANT.
- SCORING FOR PANELIZED PCB:



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: 0.XX" = ±0.01" 0.XXX" = ±0.005" INTERPRET DIM AND TOL PER ASME Y14.5M-1994 THIRD ANGLE PROJECTION	APPROVALS		 1630 MCCARTHY BLVD MILPITAS, CA 95035 PH: (408)432-1900 www.linear.com LTC CONFIDENTIAL- FOR CUSTOMER USE ONLY	
	PCB DES.			
	APP ENG.		TITLE: FABRICATION DRAWING	
			PSRR LNA	
	SIZE	IC NO.	REV	
	N/A	LAB BOARD	1	
SCALE = NONE	FILENAME:		SHT 1 OF 1	