

## Design Example Description

In this design the AD9512, 1.2GHz, 5-Channel Clock Distribution IC is used to provide clocks to analog-to-digital converters (ADCs), a digital-to-analog converters (DAC) and digital application specific integrated circuits (ASICs).

The DAC and the TX ASIC require fast clocks at 491.52MHz.

The DAC needs a fast slewing, differential LVPECL clock with broadband jitter < 400 femtoseconds rms.

The TX ASIC also needs a 491.52MHz clock, but requires an LVDS level signal.

ADC1 and ADC2 send their output data to a digital RX ASIC. All three of these chips require clocks at 122.88MHz. The ADCs require fast-slewing, differential LVPECL clocks with broadband jitter < 350 femtoseconds rms. The digital RX ASIC requires a CMOS clock at the same rate. However, the RX ASIC clock must be delayed in time relative to the ADC clocks to insure setup and hold times are met.

The AD9512 is a distribution-only chip - no jitter clean-up is done on-chip. Therefore the input clock must be low jitter to insure that output clocks meet their jitter requirements. Each of the five clock distribution channels of the AD9512 has an independent programmable divider which may be programmed to any integer 1 to 32. Each divider has a phase offset option which can be used for adding delays in integer multiples of the time period of the signal at CLK1 or CLK2 port. In this case, a 491.52 MHz "clean" clock is applied to the CLK input which corresponds to a period of ~2ns. Finally, by taking advantage of the multiple logic families available on the AD9512, the required combination of LVPECL, LVDS and CMOS output levels can be achieved.

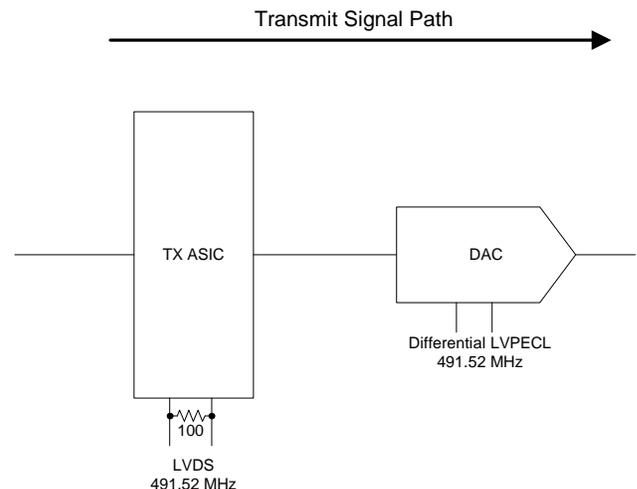
Note that ADIsimCLK allows the user to create custom input clocks. By starting with custom oscillators specified with high performance, the user can determine the jitter limitation of the AD9512 clock distribution section. This serves as a good baseline for seeing what performance is possible. The user can then change the phase noise performance of the input clock to see the impact on output clock phase noise and jitter.

The notes and diagrams below describe how to configure the AD9512 for this application. For instructions on how to navigate the ADIsimCLK page tabs and windows, please check the tutorial and help files available from the Help pulldown menu.

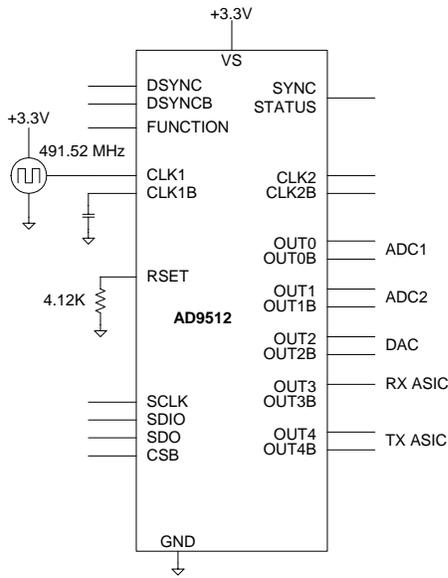
### NOTES

- 1) OUT0/OUT0B & OUT1/OUT1B differential LVPECL clocks are set to DIV=4, 780mV logic swing
- 2) OUT2/OUT2B differential LVPECL clock set to DIV=1 or divider "bypass" mode, 780mV logic swing
- 3) OUT3 LVDS/CMOS clock set to DIV=4, phase offset = 2 for ~4ns time delay; CMOS mode, OUT3B not connected
- 4) OUT4/OUT4B LVDS/CMOS clock set to DIV=1 or divider "bypass" mode, LVDS mode, 3.5mA current; optional fine delay bypassed
- 5) Input Clock is custom 491.52 MHz with PN floor at -160dBc/Hz

### CIRCUITS REQUIRING CLOCKS



### CIRCUIT



### Receive Signal Path

