

HIGH DOSE RADIATION TEST REPORT LT8650S-CSL

January 2024

Generic

Radiation Test Report	
Product:	LT8650S
Gamma:	0,50k
Gamma Source:	Co60/TM1019 Condition A
Dose Rate:	80 Rad/s
Facilities:	VPT RAD
Tested:	January 23, 2024

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		*TEMP Voltage		**FB1 Voltage (Servo)		**FB2 Voltage (Servo)	
	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	0.279	0.256	0.800	0.800	0.801	0.800
	7	0.248	0.230	0.800	0.800	0.801	0.800
	8	0.263	0.216	0.800	0.799	0.801	0.801
	9	0.248	0.199	0.800	0.802	0.801	0.802
	10	0.255	0.241	0.800	0.799	0.801	0.799
	11	0.251	0.250	0.801	0.798	0.800	0.798
	12	0.254	0.243	0.800	0.798	0.800	0.798
	Min	0.248	0.199	0.8000	0.7979	0.8004	0.7979
	Max	0.263	0.250	0.8005	0.8015	0.8013	0.8021
	Mean	0.253	0.230	0.8002	0.7992	0.8007	0.7997
	Std. Dev	0.006	0.019	0.0002	0.0013	0.0004	0.0017
	Mean - 3 Sigma	0.236	0.173	0.7995	0.7952	0.7996	0.7947
	Mean + 3 Sigma	0.270	0.287	0.8009	0.8031	0.8017	0.8047

		*I EN1(Sleep): VIN's=12.0V, EN1=2.0V(I-V)		*I EN2(Sleep): VIN's=12.0V, EN2=2.0V(I-V)		*I PG1(Sleep): VIN's=12.0V, EN1=12.0V(I-V Conv.)	
	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	0.124	0.064	0.021	0.042	0.117	-0.038
	7	0.095	0.051	-0.006	0.024	0.139	-0.067
	8	0.089	0.045	-0.020	0.063	0.134	-0.045
	9	0.087	0.067	-0.015	0.009	0.128	-0.047
	10	0.111	0.030	0.052	0.059	0.127	-0.058
	11	0.104	0.060	0.029	0.024	0.109	-0.012
	12	0.100	0.034	0.025	0.011	0.133	-0.019
	Min	0.0874	0.0299	-0.0200	0.0094	0.1087	-0.0668
	Max	0.1111	0.0674	0.0524	0.0631	0.1386	-0.0124
	Mean	0.0976	0.0478	0.0108	0.0319	0.1283	-0.0415
	Std. Dev	0.0091	0.0146	0.0289	0.0237	0.0105	0.0215
	Mean - 3 Sigma	0.0702	0.0039	-0.0758	-0.0391	0.0969	-0.1061
	Mean + 3 Sigma	0.1250	0.0917	0.0974	0.1028	0.1597	0.0231

		*I PG2(Sleep): VIN's=12.0V, EN2=12.0V(I-V Conv.)		**I VIN1(Shutdown): VIN1=VIN2=12.0V		*SS1 Pull Down R(Shutdown): SS1=0.1V	
	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	0.111	0.170	1.904	1.932	146.778	145.872
	7	0.149	0.130	1.907	1.942	149.582	147.406
	8	0.160	0.178	1.923	1.948	150.157	148.080
	9	0.108	0.167	1.948	1.982	150.607	148.434
	10	0.126	0.128	1.902	1.919	149.613	147.579
	11	0.115	0.136	2.002	2.040	148.894	146.807
	12	0.114	0.163	1.861	1.888	149.551	147.595
	Min	0.1080	0.1277	1.8614	1.8882	148.8940	146.8071
	Max	0.1595	0.1783	2.0022	2.0395	150.6073	148.4342
	Mean	0.1285	0.1504	1.9238	1.9529	149.7341	147.6502
	Std. Dev	0.0211	0.0218	0.0477	0.0526	0.5863	0.5618
	Mean - 3 Sigma	0.0650	0.0850	1.7809	1.7952	147.9753	145.9648
	Mean + 3 Sigma	0.1919	0.2157	2.0668	2.1107	151.4929	149.3355

		*SS2 Pull Down R(Shutdown): SS2=0.1V		*I SYNC(Shutdown): SYNC=6.0V		**PG1 Pull Down R(Shutdown): PG1=0.1V	
	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	171.527	170.101	94.032	93.496	504.861	500.127
	7	174.454	171.767	95.676	94.648	519.171	512.627
	8	176.941	174.369	92.678	91.729	546.858	540.751
	9	175.766	173.189	121.309	94.913	561.768	525.768
	10	176.070	173.636	121.030	119.950	567.745	557.886
	11	174.403	172.016	97.193	96.274	526.441	520.494
	12	176.637	174.226	89.735	88.824	550.561	544.617
	Min	174.4032	171.7665	89.7351	88.8236	519.1711	512.6268
	Max	176.9413	174.3688	121.3089	119.9500	567.7445	557.8861
	Mean	175.7118	173.2005	102.9367	97.7228	545.4239	533.6904
	Std. Dev	1.0765	1.1016	14.3538	11.2127	19.2009	16.9427
	Mean - 3 Sigma	172.4824	169.8958	59.8752	64.0846	487.8212	482.8622
	Mean + 3 Sigma	178.9413	176.5052	145.9982	131.3610	603.0266	584.5186

		**PG2 Pull Down R(Shutdown): PG2=0.1V		**VinQ+VccQ_VC_Internal_Comp:T1000[.6+.7+.19]		**VinQ+VccQ_VC_External_Comp: T1000[.20+.21+.22]	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	390.149	386.251	3.901	3.890	90.555	89.592
	7	403.166	397.560	3.863	11.368	89.097	95.978
	8	422.188	416.998	3.940	11.936	88.176	92.082
	9	441.789	407.530	3.996	17.362	92.968	106.402
	10	447.079	438.285	3.849	14.369	89.538	94.263
	11	407.363	402.435	4.099	18.772	89.996	99.617
	12	425.721	420.665	3.811	11.475	84.266	89.197
	Min	403.1656	397.5600	3.8108	11.3684	84.2661	89.1971
	Max	447.0795	438.2855	4.0991	18.7720	92.9684	106.4022
	Mean	424.5511	413.9123	3.9263	14.2138	89.0071	96.2566
	Std. Dev	17.6884	14.7582	0.1079	3.2092	2.8330	6.0917
	Mean - 3 Sigma	371.4858	369.6378	3.6027	4.5861	80.5081	77.9815
	Mean + 3 Sigma	477.6163	458.1868	4.2499	23.8415	97.5060	114.5317

		**VinQ+VccQ_Active: T1000[.23+.24+.25]		*SW1 Top Leakage: VIN's=42V, OUT1=0V		*SW2 Top Leakage: VIN's=42V, OUT2=0V	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	3.636	3.663	-0.828	-1.167	-0.753	-1.090
	7	3.609	3.548	-0.832	-225.433	-0.758	-302.519
	8	3.581	3.510	-0.837	-199.370	-0.755	-331.246
	9	3.636	3.574	-0.824	-307.950	-0.759	-462.679
	10	3.620	3.554	-0.818	-249.989	-0.754	-378.850
	11	3.623	3.566	-0.826	-306.456	-0.753	-470.869
	12	3.539	3.468	-0.823	-189.576	-0.757	-281.083
	Min	3.5387	3.4677	-0.8365	-307.9498	-0.7593	-470.8691
	Max	3.6355	3.5738	-0.8179	-189.5757	-0.7526	-281.0830
	Mean	3.6013	3.5367	-0.8264	-246.4623	-0.7560	-371.2077
	Std. Dev	0.0357	0.0404	0.0067	51.5529	0.0025	80.9881
	Mean - 3 Sigma	3.4941	3.4154	-0.8464	-401.1209	-0.7635	-614.1719
	Mean + 3 Sigma	3.7084	3.6580	-0.8065	-91.8036	-0.7485	-128.2435

		*SW1 Bottom Leakage: VIN's=42V, OUT1=42V		*SW2 Bottom Leakage: VIN's=42V, OUT2=42V		*IVIN1: VIN=12.0V, OUT1=-1mA	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	0.515	0.871	0.424	0.696	338.519	334.100
	7	0.582	0.794	0.487	0.636	325.768	340.972
	8	0.586	0.757	0.482	0.621	333.201	342.511
	9	0.559	0.745	0.469	0.608	321.725	339.809
	10	0.568	0.737	0.468	0.610	349.532	343.141
	11	0.571	0.744	0.467	0.605	326.175	350.393
	12	0.557	0.739	0.455	0.613	321.662	342.801
	Min	0.5566	0.7372	0.4553	0.6054	321.6618	339.8091
	Max	0.5855	0.7942	0.4869	0.6363	349.5321	350.3927
	Mean	0.5703	0.7525	0.4714	0.6156	329.6772	343.2711
	Std. Dev	0.0116	0.0216	0.0114	0.0115	10.5987	3.7096
	Mean - 3 Sigma	0.5354	0.6878	0.4371	0.5811	297.8810	332.1423
	Mean + 3 Sigma	0.6051	0.8173	0.5057	0.6501	361.4733	354.3998

		*IVIN2: VIN=12.0V, OUT2=-1mA		*IVIN1: VIN=12.0V, OUT1=-100uA		*IVIN2: VIN=12.0V, OUT2=-100uA	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	311.965	321.789	44.113	43.651	34.916	41.494
	7	321.587	324.311	42.336	42.239	42.029	37.571
	8	333.120	324.402	45.121	41.869	34.150	40.519
	9	307.128	330.267	37.025	43.010	38.461	42.451
	10	321.242	324.633	42.755	38.082	38.603	40.460
	11	327.272	326.519	42.484	36.663	38.098	42.120
	12	322.208	322.450	42.478	40.839	37.533	40.819
	Min	307.1275	322.4498	37.0253	36.6629	34.1502	37.5714
	Max	333.1203	330.2665	45.1211	43.0099	42.0293	42.4513
	Mean	322.0930	325.4302	42.0332	40.4505	38.1456	40.6567
	Std. Dev	8.6416	2.6983	2.6694	2.5247	2.5192	1.7301
	Mean - 3 Sigma	296.1682	317.3354	34.0250	32.8764	30.5880	35.4664
	Mean + 3 Sigma	348.0178	333.5251	50.0414	48.0245	45.7033	45.8470

		** SW_Min_OnTime Sync=3.4V@3A		** SW_Min_OnTime Sync=3.4V@3A		* Top_I_Lim1, dummy@hot	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	40.043	41.228	38.331	35.856	12070.694	12052.699
	7	32.390	40.557	38.061	38.398	12052.699	12790.488
	8	38.413	39.075	40.686	38.288	11764.782	12466.581
	9	42.395	31.316	34.655	37.607	11908.740	12664.524
	10	42.325	37.423	35.569	38.019	12016.709	12754.498
	11	33.553	34.397	34.882	37.995	12034.704	12754.498
	12	35.277	33.485	38.546	37.898	11710.797	12430.592
	Min	32.3898	31.3155	34.6546	37.6072	11710.7969	12430.5918
	Max	42.3949	40.5570	40.6857	38.3981	12052.6992	12790.4883
	Mean	37.3922	36.0422	37.0665	38.0341	11914.7386	12643.5303
	Std. Dev	4.3506	3.5516	2.4127	0.2826	146.9271	157.0471
	Mean - 3 Sigma	24.3404	25.3873	29.8282	37.1864	11473.9572	12172.3890
	Mean + 3 Sigma	50.4441	46.6971	44.3047	38.8819	12355.5200	13114.6715

		* Top_I_Lim2, dummy@hot		** Minimum Input Voltage1 [Min_Vin_UVLO1]		* BotRDSon 1[Pgnd-Vsw]	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	11926.735	11908.740	2.460	2.470	0.030	0.030
	7	11764.782	12538.561	2.410	2.420	0.030	0.029
	8	11818.766	12664.524	2.500	2.500	0.030	0.028
	9	12016.709	12826.478	2.460	2.450	0.030	0.028
	10	12034.704	12826.478	2.450	2.430	0.030	0.029
	11	12088.688	12880.463	2.450	2.460	0.030	0.028
	12	12124.679	12952.442	2.480	2.480	0.030	0.028
	Min	11764.7822	12538.5606	2.4100	2.4200	0.0299	0.0283
	Max	12124.6787	12952.4424	2.5000	2.5000	0.0302	0.0287
	Mean	11974.7214	12781.4909	2.4583	2.4567	0.0301	0.0285
	Std. Dev	147.8061	152.1603	0.0306	0.0301	0.0001	0.0001
	Mean - 3 Sigma	11531.3030	12325.0100	2.3665	2.3663	0.0298	0.0280
	Mean + 3 Sigma	12418.1397	13237.9718	2.5501	2.5470	0.0304	0.0289

		* BotRDSon 2[Pgnd-Vsw]		* DA_Current_Limit1 [Bot_I_Lim]		* DA_Current_Limit2 [Bot_I_Lim]	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	0.030	0.029	8716.263	8740.484	8546.713	8522.491
	7	0.030	0.028	8619.377	8498.271	8716.263	8643.599
	8	0.030	0.028	8619.377	8498.271	8692.041	8619.377
	9	0.030	0.028	8934.256	8788.927	8619.377	8498.271
	10	0.030	0.028	8861.592	8692.041	8522.491	8474.049
	11	0.030	0.028	8934.256	8716.263	8813.148	8667.820
	12	0.030	0.028	8716.263	8546.713	8328.720	8256.056
	Min	0.0298	0.0279	8619.3770	8498.2705	8328.7197	8256.0557
	Max	0.0300	0.0282	8934.2559	8788.9268	8813.1484	8667.8203
	Mean	0.0299	0.0280	8780.8534	8623.4141	8615.3400	8526.5285
	Std. Dev	0.0001	0.0001	148.2596	124.8438	170.8713	154.2711
	Mean - 3 Sigma	0.0297	0.0277	8336.0745	8248.8827	8102.7261	8063.7153
	Mean + 3 Sigma	0.0301	0.0283	9225.6322	8997.9455	9127.9539	8989.3417

		* Vintvcc_0mA_no_bias		* Vintvcc_0mA_with_bias		* Intvcc_UVLO_Threshold RampDown	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	3.465	3.464	3.258	3.259	2.245	2.249
	7	3.397	3.404	3.255	3.256	2.237	2.213
	8	3.430	3.429	3.256	3.258	2.321	2.305
	9	3.438	3.448	3.256	3.258	2.277	2.257
	10	3.415	3.412	3.256	3.257	2.273	2.253
	11	3.421	3.411	3.257	3.257	2.281	2.253
	12	3.419	3.410	3.255	3.257	2.305	2.281
	Min	3.3966	3.4045	3.2551	3.2564	2.2369	2.2129
	Max	3.4376	3.4478	3.2566	3.2576	2.3213	2.3052
	Mean	3.4198	3.4190	3.2559	3.2570	2.2825	2.2604
	Std. Dev	0.0141	0.0164	0.0006	0.0005	0.0290	0.0310
	Mean - 3 Sigma	3.3775	3.3698	3.2541	3.2556	2.1954	2.1672
	Mean + 3 Sigma	3.4620	3.4683	3.2576	3.2584	2.3696	2.3535

		**EN1_Threshold RampDown		* EN1_Threshold Hysteresis		**EN2_Threshold RampDown	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	0.733	0.733	0.030	0.030	0.735	0.733
	7	0.735	0.731	0.026	0.028	0.737	0.735
	8	0.731	0.727	0.030	0.030	0.737	0.733
	9	0.733	0.731	0.028	0.028	0.735	0.733
	10	0.733	0.729	0.028	0.028	0.731	0.727
	11	0.737	0.733	0.030	0.030	0.733	0.729
	12	0.733	0.729	0.028	0.030	0.733	0.729
	Min	0.7309	0.7269	0.0261	0.0281	0.7309	0.7269
	Max	0.7369	0.7329	0.0301	0.0301	0.7369	0.7349
	Mean	0.7336	0.7299	0.0284	0.0291	0.7343	0.7309
	Std. Dev	0.0021	0.0021	0.0015	0.0011	0.0024	0.0031
	Mean - 3 Sigma	0.7274	0.7236	0.0239	0.0258	0.7270	0.7216
	Mean + 3 Sigma	0.7398	0.7362	0.0330	0.0324	0.7416	0.7403

		* EN2_Threshold Hysteresis		** PG1 Lower Threshold Offset from VFB		* PG1 Low Hysteresis	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	0.026	0.028	-7.907	-7.930	0.315	0.304
	7	0.028	0.028	-7.779	-7.807	0.337	0.281
	8	0.030	0.030	-7.721	-7.796	0.348	0.270
	9	0.028	0.030	-7.724	-7.785	0.348	0.324
	10	0.028	0.028	-7.673	-7.734	0.314	0.315
	11	0.030	0.028	-7.881	-7.912	0.326	0.317
	12	0.028	0.030	-7.769	-7.654	0.303	0.361
	Min	0.0281	0.0281	-7.8814	-7.9118	0.3028	0.2700
	Max	0.0301	0.0301	-7.6732	-7.6537	0.3480	0.3610
	Mean	0.0288	0.0291	-7.7579	-7.7812	0.3293	0.3114
	Std. Dev	0.0010	0.0011	0.0714	0.0853	0.0185	0.0326
	Mean - 3 Sigma	0.0257	0.0258	-7.9723	-8.0372	0.2738	0.2137
	Mean + 3 Sigma	0.0319	0.0324	-7.5436	-7.5252	0.3848	0.4091

		** PG2 Lower Threshold Offset from VFB		* PG2 Low Hysteresis		** PG1 Upper Threshold Offset from VFB	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	-7.667	-7.672	0.314	0.303	7.046	7.041
	7	-7.228	-7.143	0.312	0.312	6.884	6.782
	8	-7.890	-7.957	0.337	0.315	6.661	6.679
	9	-7.753	-7.792	0.303	0.324	6.748	6.683
	10	-7.636	-7.711	0.325	0.326	7.012	6.977
	11	-7.658	-7.665	0.359	0.350	6.921	6.851
	12	-7.833	-7.776	0.326	0.328	6.967	7.024
	Min	-7.8897	-7.9574	0.3029	0.3122	6.6610	6.6790
	Max	-7.2275	-7.1427	0.3592	0.3502	7.0123	7.0245
	Mean	-7.6661	-7.6739	0.3269	0.3260	6.8655	6.8326
	Std. Dev	0.2361	0.2787	0.0197	0.0135	0.1349	0.1460
	Mean - 3 Sigma	-8.3744	-8.5101	0.2677	0.2855	6.4609	6.3948
	Mean + 3 Sigma	-6.9578	-6.8378	0.3861	0.3665	7.2701	7.2705

		* PG1 HI Hysteresis		** PG2 Upper Threshold Offset from VFB		* PG2 HI Hysteresis	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	0.308	0.278	7.064	7.079	0.308	0.316
	7	0.301	0.324	7.189	7.196	0.286	0.301
	8	0.301	0.279	7.072	7.033	0.286	0.301
	9	0.361	0.338	6.940	6.810	0.286	0.315
	10	0.278	0.316	6.900	6.893	0.293	0.324
	11	0.286	0.309	7.121	7.122	0.301	0.279
	12	0.316	0.324	6.616	6.671	0.308	0.317
	Min	0.2783	0.2786	6.6161	6.6709	0.2855	0.2792
	Max	0.3611	0.3378	7.1887	7.1964	0.3085	0.3240
	Mean	0.3071	0.3150	6.9729	6.9543	0.2933	0.3062
	Std. Dev	0.0295	0.0202	0.2059	0.1989	0.0096	0.0161
	Mean - 3 Sigma	0.2186	0.2544	6.3553	6.3575	0.2645	0.2578
	Mean + 3 Sigma	0.3957	0.3756	7.5906	7.5511	0.3221	0.3546

		* SYNC_Threshold RampDown		* SYNC_Threshold RampUp		*Source I_Vc1 at FB-200mV @ Vin=6V Vc=1.25V	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	0.934	0.934	1.181	1.181	-158.008	-157.611
	7	0.916	0.898	1.141	1.133	-152.493	-150.898
	8	0.886	0.867	1.108	1.084	-150.195	-149.163
	9	0.916	0.898	1.149	1.133	-161.200	-161.928
	10	0.898	0.880	1.116	1.100	-152.806	-151.060
	11	0.910	0.892	1.141	1.124	-155.154	-153.007
	12	0.904	0.880	1.133	1.116	-144.536	-140.517
	Min	0.8855	0.8675	1.1084	1.0843	-161.2000	-161.9278
	Max	0.9157	0.8976	1.1486	1.1325	-144.5361	-140.5167
	Mean	0.9046	0.8855	1.1312	1.1151	-152.7306	-151.0954
	Std. Dev	0.0117	0.0120	0.0156	0.0193	5.4999	6.8801
	Mean - 3 Sigma	0.8695	0.8494	1.0844	1.0573	-169.2303	-171.7356
	Mean + 3 Sigma	0.9397	0.9217	1.1780	1.1730	-136.2309	-130.4553

		*Sink I_Vc1 at FB+200mV @ Vin=6V Vc=1.25V		*Gm Error Amp1 @ Vin=6V Vc=1.25V		*VC-SW1Gain[(T2300.1+T2300.3)/T4400.0], dummy@hot	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	156.337	156.557	785.863	785.418	6.225	6.211
	7	149.342	148.272	754.587	747.924	6.234	6.699
	8	146.556	147.498	741.877	741.654	6.181	6.649
	9	157.998	156.307	797.995	795.587	6.135	6.617
	10	150.247	150.954	757.632	755.036	6.237	6.725
	11	150.953	152.601	765.267	764.019	6.191	6.681
	12	140.629	140.748	712.912	703.161	6.074	6.562
	Min	140.6286	140.7477	712.9118	703.1611	6.0743	6.5623
	Max	157.9982	156.3070	797.9953	795.5871	6.2367	6.7250
	Mean	149.2874	149.3966	755.0450	751.2301	6.1752	6.6555
	Std. Dev	5.6923	5.2938	27.9454	30.1956	0.0621	0.0592
	Mean - 3 Sigma	132.2105	133.5152	671.2087	660.6434	5.9889	6.4779
	Mean + 3 Sigma	166.3643	165.2781	838.8812	841.8168	6.3616	6.8332

		*Source I_Vc2 at FB-200mV @ Vin=6V Vc=1.25V		*Sink I_Vc2 at FB+200mV @ Vin=6V Vc=1.25V		*Gm Error Amp2 @ Vin=6V Vc=1.25V	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	-158.121	-157.623	156.387	156.488	786.269	785.278
	7	-152.137	-150.898	149.060	148.403	752.994	748.251
	8	-150.313	-149.064	146.818	147.454	742.829	741.295
	9	-161.412	-161.934	158.036	156.532	798.620	796.164
	10	-153.037	-151.141	150.659	151.297	759.240	756.096
	11	-155.323	-152.994	150.940	152.720	765.658	764.285
	12	-144.380	-140.373	140.697	140.635	712.693	702.522
	Min	-161.4123	-161.9341	140.6973	140.6354	712.6932	702.5216
	Max	-144.3800	-140.3732	158.0357	156.5316	798.6199	796.1641
	Mean	-152.7671	-151.0673	149.3686	149.5068	755.3391	751.4354
	Std. Dev	5.6232	6.9313	5.6753	5.4224	28.1978	30.6366
	Mean - 3 Sigma	-169.6367	-171.8611	132.3426	133.2398	670.7456	659.5256
	Mean + 3 Sigma	-135.8974	-130.2736	166.3945	165.7739	839.9325	843.3453

		*VC-SW2Gain[(T2350.1+T2350.3)/T4450.0], dummy@hot		* Feedback Voltage Line Regulation 1		* Feedback Voltage Line Regulation 2	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	6.336	6.322	0.002	0.002	0.002	0.002
	7	6.258	6.743	0.002	0.002	0.002	0.002
	8	6.355	6.899	0.001	0.001	0.001	0.001
	9	6.397	6.912	0.002	0.002	0.002	0.002
	10	6.417	6.939	0.002	0.002	0.001	0.001
	11	6.407	6.934	0.002	0.002	0.002	0.002
	12	6.503	7.057	0.001	0.001	0.001	0.001
	Min	6.2577	6.7433	0.0012	0.0012	0.0010	0.0011
	Max	6.5032	7.0565	0.0021	0.0022	0.0020	0.0021
	Mean	6.3894	6.9140	0.0017	0.0018	0.0015	0.0016
	Std. Dev	0.0808	0.1007	0.0004	0.0004	0.0004	0.0005
	Mean - 3 Sigma	6.1471	6.6119	0.0006	0.0006	0.0002	0.0002
	Mean + 3 Sigma	6.6317	7.2161	0.0029	0.0030	0.0028	0.0030

		* BIAS_pin_Current_Consumption		** SS1_Pin_Current		** SS2_Pin_Current	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	5.385	5.405	-1.877	-1.883	-1.882	-1.880
	7	5.584	5.739	-1.788	-1.859	-1.793	-1.851
	8	5.496	5.692	-1.617	-1.687	-1.679	-1.744
	9	5.469	5.639	-1.875	-1.953	-1.868	-1.924
	10	5.497	5.673	-1.724	-1.798	-1.762	-1.821
	11	5.514	5.735	-1.874	-1.935	-1.843	-1.911
	12	5.524	5.705	-1.647	-1.699	-1.664	-1.719
	Min	5.4690	5.6393	-1.8748	-1.9528	-1.8681	-1.9240
	Max	5.5841	5.7386	-1.6173	-1.6865	-1.6644	-1.7186
	Mean	5.5140	5.6970	-1.7541	-1.8217	-1.7683	-1.8282
	Std. Dev	0.0392	0.0378	0.1107	0.1143	0.0835	0.0845
	Mean - 3 Sigma	5.3965	5.5834	-2.0862	-2.1645	-2.0188	-2.0817
	Mean + 3 Sigma	5.6315	5.8105	-1.4221	-1.4788	-1.5177	-1.5747

		** Datasheet_Osc_High [Rt=15K]		** Datasheet_Osc_Low [Rt=35.7K]		** Datasheet_Osc_Low [Rt=133K]	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	1992.141	1994.838	990.601	991.302	303.871	303.899
	7	2026.768	2013.871	1000.510	996.492	300.326	299.625
	8	2006.120	1994.633	995.972	993.391	302.679	302.812
	9	2017.171	2010.194	998.412	998.521	304.620	305.583
	10	2019.775	2004.370	993.232	988.602	296.681	296.135
	11	2022.316	2011.346	998.555	996.071	301.518	301.339
	12	2018.515	2003.221	998.923	993.052	300.920	299.341
	Min	2006.1196	1994.6326	993.2317	988.6015	296.6812	296.1351
	Max	2026.7682	2013.8711	1000.5104	998.5212	304.6197	305.5826
	Mean	2018.4441	2006.2725	997.6006	994.3550	301.1239	300.8056
	Std. Dev	6.9220	7.0324	2.5894	3.4814	2.6537	3.2398
	Mean - 3 Sigma	1997.6781	1985.1752	989.8323	983.9109	293.1629	291.0861
	Mean + 3 Sigma	2039.2101	2027.3697	1005.3689	1004.7991	309.0850	310.5251

		* Spread_Spectrum_Threshold [1Mhz] CH1		* Spread_Spectrum_Modulation_Pct[At threshold] CH1		* Spread_Spectrum_Threshold [1Mhz] CH2	
Wafer	SN	PRE	50k	PRE	50k	PRE	50k
CTRL	40	2.550	2.550	16.804	16.844	2.550	2.550
	7	2.500	2.500	17.874	17.710	2.500	2.500
	8	2.500	2.500	17.845	18.595	2.500	2.500
	9	2.500	2.500	17.758	18.080	2.500	2.500
	10	2.500	2.500	18.231	18.591	2.500	2.500
	11	2.500	2.500	17.053	18.205	2.500	2.500
	12	2.500	2.500	17.614	17.979	2.500	2.500
	Min	2.5000	2.5000	17.0534	17.7103	2.5000	2.5000
	Max	2.5000	2.5000	18.2310	18.5952	2.5000	2.5000
	Mean	2.5000	2.5000	17.7293	18.1933	2.5000	2.5000
	Std. Dev	0.0000	0.0000	0.3891	0.3497	0.0000	0.0000
	Mean - 3 Sigma	2.5000	2.5000	16.5619	17.1442	2.5000	2.5000
	Mean + 3 Sigma	2.5000	2.5000	18.8967	19.2424	2.5000	2.5000

		* Spread_Spectrum_Modulation_Pct[At threshold] CH2		* Spread_Spectrum_3kHz CH2	
Wafer	SN	PRE	50k	PRE	50k
CTRL	40	16.667	16.667	6.757	6.757
	7	17.313	18.010	5.556	5.814
	8	18.002	18.513	5.319	6.098
	9	18.248	17.662	6.757	6.410
	10	18.089	19.075	4.310	6.250
	11	18.219	18.210	5.952	2.232
	12	18.211	18.119	6.098	7.813
	Min	17.3134	17.6622	4.3103	2.2321
	Max	18.2477	19.0753	6.7568	7.8125
	Mean	18.0137	18.2649	5.6653	5.7694
	Std. Dev	0.3555	0.4840	0.8280	1.8675
	Mean - 3 Sigma	16.9472	16.8129	3.1811	0.1669
	Mean + 3 Sigma	19.0802	19.7169	8.1494	11.3719

















