

HIGH DOSE RADIATION TEST REPORT LT8650S-CSL

January 2024
Generic

Radiation Test Report	
Product:	LT8650S-CSL
Gamma:	0,30k
Gamma Source:	Co60/TM1019 Condition A
Dose Rate:	80 Rad/s
Facilities:	VPT RAD
Tested:	January 23, 2024

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		*TEMP Voltage		**FB1 Voltage (Servo)		**FB2 Voltage (Servo)	
	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	0.279	0.256	0.800	0.800	0.801	0.800
	1	0.261	0.235	0.801	0.800	0.801	0.801
	2	0.235	0.223	0.801	0.802	0.801	0.801
	3	0.262	0.253	0.800	0.799	0.801	0.799
	4	0.248	0.220	0.800	0.799	0.800	0.800
	5	0.243	0.218	0.800	0.799	0.801	0.801
	6	0.247	0.209	0.801	0.800	0.800	0.800
	Min	0.235	0.209	0.7995	0.7986	0.8001	0.7991
	Max	0.262	0.253	0.8010	0.8018	0.8013	0.8012
	Mean	0.249	0.226	0.8003	0.7997	0.8008	0.8003
	Std. Dev	0.010	0.016	0.0006	0.0011	0.0005	0.0008
	Mean - 3 Sigma	0.218	0.180	0.7985	0.7964	0.7993	0.7978
	Mean + 3 Sigma	0.281	0.273	0.8021	0.8031	0.8023	0.8028

		*I EN1(Sleep): VIN's=12.0V, EN1=2.0V(I-V)		*I EN2(Sleep): VIN's=12.0V, EN2=2.0V(I-V)		*I PG1(Sleep): VIN's=12.0V, EN1=12.0V(I-V Conv.)	
	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	0.124	0.064	0.021	0.042	0.117	-0.038
	1	0.136	0.065	0.025	0.037	0.116	-0.030
	2	0.087	0.055	0.022	0.001	0.120	-0.026
	3	0.090	0.095	-0.005	0.024	0.128	-0.071
	4	0.086	0.026	-0.009	0.004	0.109	-0.019
	5	0.097	0.011	0.027	0.009	0.111	-0.048
	6	0.082	0.027	-0.023	0.021	0.107	-0.061
	Min	0.0824	0.0111	-0.0225	0.0007	0.1068	-0.0715
	Max	0.1361	0.0948	0.0275	0.0369	0.1283	-0.0190
	Mean	0.0965	0.0465	0.0064	0.0161	0.1151	-0.0427
	Std. Dev	0.0200	0.0309	0.0212	0.0137	0.0081	0.0209
	Mean - 3 Sigma	0.0365	-0.0462	-0.0571	-0.0251	0.0907	-0.1053
	Mean + 3 Sigma	0.1566	0.1392	0.0700	0.0572	0.1394	0.0199

		*I PG2(Sleep): VIN's=12.0V, EN2=12.0V(I-V Conv.)		**I VIN1(Shutdown): VIN1=VIN2=12.0V		*SS1 Pull Down R(Shutdown): SS1=0.1V	
	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	0.111	0.170	1.904	1.932	146.778	145.872
	1	0.099	0.117	1.952	1.943	148.628	146.721
	2	0.119	0.152	1.981	1.990	152.036	150.113
	3	0.156	0.165	1.964	1.971	149.796	148.003
	4	0.170	0.172	1.906	1.908	149.237	147.515
	5	0.115	0.131	1.850	1.856	153.020	151.183
	6	0.107	0.169	1.938	1.945	151.669	149.837
	Min	0.0986	0.1174	1.8496	1.8555	148.6279	146.7209
	Max	0.1698	0.1717	1.9806	1.9904	153.0195	151.1826
	Mean	0.1275	0.1511	1.9316	1.9356	150.7308	148.8952
	Std. Dev	0.0286	0.0222	0.0475	0.0481	1.7521	1.7339
	Mean - 3 Sigma	0.0418	0.0846	1.7891	1.7913	145.4746	143.6937
	Mean + 3 Sigma	0.2132	0.2177	2.0741	2.0799	155.9870	154.0968

		*SS2 Pull Down R(Shutdown): SS2=0.1V		*I SYNC(Shutdown): SYNC=6.0V		**PG1 Pull Down R(Shutdown): PG1=0.1V	
	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	171.527	170.101	94.032	93.496	504.861	500.127
	1	173.294	171.021	97.853	123.155	512.338	534.313
	2	177.510	175.142	94.573	118.969	539.955	559.272
	3	175.008	172.912	95.561	94.803	533.449	527.528
	4	177.140	174.993	116.361	115.530	580.505	572.026
	5	178.942	176.719	92.234	116.420	549.902	568.188
	6	175.877	173.727	95.975	120.690	535.167	555.815
	Min	173.2939	171.0211	92.2343	94.8031	512.3381	527.5278
	Max	178.9421	176.7187	116.3606	123.1552	580.5055	572.0255
	Mean	176.2952	174.0855	98.7595	114.9279	541.8861	552.8569
	Std. Dev	2.0018	1.9884	8.8171	10.2452	22.5781	18.0987
	Mean - 3 Sigma	170.2897	168.1203	72.3081	84.1924	474.1520	498.5608
	Mean + 3 Sigma	182.3007	180.0507	125.2108	145.6633	609.6203	607.1530

		**PG2 Pull Down R(Shutdown): PG2=0.1V		**VinQ+VccQ_VC_Internal_Comp:T1000[.6+.7+.19]		**VinQ+VccQ_VC_External_Comp: T1000[.20+.21+.22]	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	390.149	386.251	3.901	3.890	90.555	89.592
	1	398.182	419.144	3.969	7.116	91.445	90.471
	2	419.754	439.289	4.032	7.265	86.642	88.536
	3	413.391	408.570	4.002	6.406	92.386	92.507
	4	453.773	446.509	3.858	6.103	87.771	86.222
	5	427.617	445.923	3.753	6.836	86.585	89.928
	6	416.921	438.563	3.932	6.307	90.317	89.764
	Min	398.1820	408.5701	3.7534	6.1031	86.5848	86.2225
	Max	453.7728	446.5093	4.0323	7.2654	92.3861	92.5073
	Mean	421.6062	432.9998	3.9244	6.6724	89.1911	89.5716
	Std. Dev	18.5061	15.5487	0.1033	0.4697	2.5245	2.0919
	Mean - 3 Sigma	366.0879	386.3537	3.6144	5.2632	81.6177	83.2960
	Mean + 3 Sigma	477.1246	479.6458	4.2344	8.0816	96.7645	95.8473

		**VinQ+VccQ_Active: T1000[.23+.24+.25]		*SW1 Top Leakage: VIN's=42V, OUT1=0V		*SW2 Top Leakage: VIN's=42V, OUT2=0V	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	3.636	3.663	-0.828	-1.167	-0.753	-1.090
	1	3.668	3.642	-0.864	-122.044	-0.793	-185.348
	2	3.590	3.550	-0.831	-113.190	-0.760	-192.397
	3	3.629	3.595	-0.831	-101.693	-0.761	-159.617
	4	3.577	3.541	-0.835	-77.665	-0.763	-140.467
	5	3.563	3.521	-0.834	-110.973	-0.753	-171.078
	6	3.625	3.589	-0.839	-107.479	-0.754	-167.528
	Min	3.5625	3.5208	-0.8636	-122.0441	-0.7931	-192.3968
	Max	3.6681	3.6424	-0.8312	-77.6651	-0.7527	-140.4668
	Mean	3.6087	3.5730	-0.8391	-105.5075	-0.7640	-169.4058
	Std. Dev	0.0392	0.0443	0.0123	15.2052	0.0148	18.5600
	Mean - 3 Sigma	3.4912	3.4401	-0.8761	-151.1231	-0.8085	-225.0856
	Mean + 3 Sigma	3.7262	3.7058	-0.8020	-59.8919	-0.7196	-113.7259

		*SW1 Bottom Leakage: VIN's=42V, OUT1=42V		*SW2 Bottom Leakage: VIN's=42V, OUT2=42V		*IVIN1: VIN=12.0V, OUT1=-1mA	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	0.515	0.871	0.424	0.696	338.519	334.100
	1	0.770	0.782	0.635	0.636	332.131	344.819
	2	0.671	0.751	0.551	0.611	321.727	337.895
	3	0.619	0.740	0.520	0.619	334.520	338.551
	4	0.596	0.738	0.505	0.618	329.323	351.223
	5	0.611	0.764	0.494	0.619	328.435	338.646
	6	0.592	0.749	0.485	0.612	349.148	322.832
	Min	0.5923	0.7382	0.4850	0.6113	321.7272	322.8318
	Max	0.7702	0.7821	0.6348	0.6356	349.1480	351.2231
	Mean	0.6432	0.7541	0.5316	0.6191	332.5474	338.9942
	Std. Dev	0.0683	0.0165	0.0556	0.0087	9.2090	9.4469
	Mean - 3 Sigma	0.4383	0.7047	0.3648	0.5929	304.9205	310.6535
	Mean + 3 Sigma	0.8481	0.8036	0.6985	0.6453	360.1744	367.3350

		*IVIN2: VIN=12.0V, OUT2=-1mA		*IVIN1: VIN=12.0V, OUT1=-100uA		*IVIN2: VIN=12.0V, OUT2=-100uA	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	311.965	321.789	44.113	43.651	34.916	41.494
	1	330.410	319.924	51.551	43.261	36.109	38.139
	2	322.484	314.100	40.344	40.835	32.956	36.394
	3	320.677	319.861	42.689	48.354	38.449	38.379
	4	322.933	321.424	49.620	43.853	37.942	38.135
	5	318.031	302.593	44.137	40.290	37.130	37.201
	6	319.927	320.312	42.562	45.412	37.915	38.450
	Min	318.0306	302.5930	40.3436	40.2902	32.9564	36.3937
	Max	330.4104	321.4241	51.5511	48.3544	38.4491	38.4500
	Mean	322.4104	316.3692	45.1505	43.6677	36.7501	37.7828
	Std. Dev	4.3042	7.2231	4.4235	2.9880	2.0303	0.8148
	Mean - 3 Sigma	309.4976	294.6999	31.8800	34.7038	30.6591	35.3383
	Mean + 3 Sigma	335.3231	338.0386	58.4210	52.6316	42.8412	40.2273

		** SW_Min_OnTime Sync=3.4V@3A		** SW_Min_OnTime Sync=3.4V@3A		* Top_I_Lim1, dummy@hot	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	40.043	41.228	38.331	35.856	12070.694	12052.699
	1	36.558	34.014	36.324	40.955	11926.735	12304.627
	2	41.770	38.675	36.187	30.730	12016.709	12466.581
	3	41.833	35.382	41.884	36.807	11998.715	12430.592
	4	42.274	31.227	39.840	33.831	11872.750	12322.622
	5	42.620	35.777	39.599	34.651	11854.756	12268.638
	6	31.790	37.500	31.644	35.811	11800.771	12160.668
	Min	31.7902	31.2268	31.6442	30.7297	11800.7705	12160.6680
	Max	42.6198	38.6747	41.8840	40.9548	12016.7090	12466.5811
	Mean	39.4744	35.4290	37.5796	35.4640	11911.7393	12325.6213
	Std. Dev	4.3845	2.6310	3.6457	3.4004	84.7226	111.1710
	Mean - 3 Sigma	26.3209	27.5361	26.6424	25.2629	11657.5714	11992.1083
	Mean + 3 Sigma	52.6279	43.3220	48.5168	45.6650	12165.9071	12659.1342

		* Top_I_Lim2, dummy@hot		** Minimum Input Voltage1 [Min_Vin_UVLO1]		* BotRDSon 1[Pgnd-Vsw]	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	11926.735	11908.740	2.460	2.470	0.030	0.030
	1	12160.668	12646.529	2.440	2.450	0.030	0.029
	2	11890.745	12430.592	2.450	2.450	0.030	0.029
	3	12178.663	12682.519	2.440	2.440	0.030	0.029
	4	12052.699	12556.555	2.440	2.450	0.030	0.029
	5	12106.684	12592.545	2.440	2.450	0.030	0.029
	6	11854.756	12340.617	2.450	2.450	0.030	0.029
	Min	11854.7559	12340.6172	2.4400	2.4400	0.0300	0.0286
	Max	12178.6631	12682.5186	2.4500	2.4500	0.0302	0.0288
	Mean	12040.7025	12541.5594	2.4433	2.4483	0.0301	0.0287
	Std. Dev	137.8301	131.4566	0.0052	0.0041	0.0001	0.0001
	Mean - 3 Sigma	11627.2123	12147.1898	2.4278	2.4361	0.0298	0.0284
	Mean + 3 Sigma	12454.1927	12935.9291	2.4588	2.4606	0.0304	0.0290

		* BotRDSon 2[Pgnd-Vsw]		* DA_Current_Limit1 [Bot_I_Lim]		* DA_Current_Limit2 [Bot_I_Lim]	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	0.030	0.029	8716.263	8740.484	8546.713	8522.491
	1	0.030	0.028	8740.484	8498.271	8498.271	8280.277
	2	0.030	0.028	8837.370	8643.599	8716.263	8546.713
	3	0.030	0.028	8910.034	8692.041	8667.820	8498.271
	4	0.030	0.028	8183.391	7989.619	8304.499	8183.391
	5	0.030	0.028	8788.927	8546.713	8619.377	8449.827
	6	0.030	0.028	8813.148	8546.713	8813.148	8619.377
	Min	0.0298	0.0281	8183.3906	7989.6191	8304.4990	8183.3906
	Max	0.0300	0.0283	8910.0342	8692.0410	8813.1484	8619.3770
	Mean	0.0299	0.0283	8712.2257	8486.1592	8603.2297	8429.6426
	Std. Dev	0.0001	0.0001	265.0747	253.4588	179.7395	165.9951
	Mean - 3 Sigma	0.0296	0.0280	7917.0018	7725.7829	8064.0111	7931.6574
	Mean + 3 Sigma	0.0302	0.0285	9507.4497	9246.5355	9142.4482	8927.6278

		* Vintvcc_0mA_no_bias		* Vintvcc_0mA_with_bias		* Intvcc_UVLO_Threshold RampDown	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	3.465	3.464	3.258	3.259	2.245	2.249
	1	3.426	3.428	3.257	3.258	2.229	2.213
	2	3.405	3.408	3.257	3.257	2.273	2.265
	3	3.428	3.425	3.256	3.258	2.269	2.249
	4	3.443	3.443	3.256	3.257	2.273	2.269
	5	3.398	3.400	3.256	3.258	2.253	2.233
	6	3.414	3.415	3.256	3.257	2.273	2.257
	Min	3.3980	3.4003	3.2557	3.2572	2.2289	2.2129
	Max	3.4434	3.4427	3.2569	3.2585	2.2731	2.2691
	Mean	3.4192	3.4197	3.2563	3.2576	2.2617	2.2477
	Std. Dev	0.0167	0.0152	0.0005	0.0005	0.0179	0.0214
	Mean - 3 Sigma	3.3692	3.3740	3.2549	3.2563	2.2081	2.1836
	Mean + 3 Sigma	3.4693	3.4654	3.2576	3.2590	2.3153	2.3117

		**EN1_Threshold RampDown		* EN1_Threshold Hysteresis		**EN2_Threshold RampDown	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	0.733	0.733	0.030	0.030	0.735	0.733
	1	0.735	0.733	0.028	0.028	0.741	0.739
	2	0.739	0.739	0.030	0.028	0.735	0.733
	3	0.731	0.727	0.028	0.030	0.733	0.731
	4	0.731	0.729	0.030	0.030	0.731	0.729
	5	0.727	0.725	0.030	0.030	0.737	0.735
	6	0.737	0.735	0.028	0.028	0.733	0.733
	Min	0.7269	0.7249	0.0281	0.0281	0.7309	0.7289
	Max	0.7390	0.7390	0.0301	0.0301	0.7410	0.7390
	Mean	0.7333	0.7313	0.0291	0.0291	0.7349	0.7333
	Std. Dev	0.0045	0.0053	0.0011	0.0011	0.0036	0.0035
	Mean - 3 Sigma	0.7198	0.7154	0.0258	0.0258	0.7242	0.7229
	Mean + 3 Sigma	0.7467	0.7472	0.0324	0.0324	0.7457	0.7436

		* EN2_Threshold Hysteresis		** PG1 Lower Threshold Offset from VFB		* PG1 Low Hysteresis	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	0.026	0.028	-7.907	-7.930	0.315	0.304
	1	0.028	0.030	-7.831	-7.782	0.348	0.337
	2	0.030	0.030	-7.508	-7.601	0.324	0.323
	3	0.028	0.028	-8.009	-8.067	0.293	0.294
	4	0.028	0.028	-7.519	-7.543	0.336	0.325
	5	0.030	0.030	-8.340	-8.350	0.306	0.295
	6	0.028	0.028	-7.446	-7.402	0.279	0.313
	Min	0.0281	0.0281	-8.3404	-8.3504	0.2787	0.2945
	Max	0.0301	0.0301	-7.4465	-7.4019	0.3476	0.3370
	Mean	0.0288	0.0291	-7.7756	-7.7910	0.3142	0.3147
	Std. Dev	0.0010	0.0011	0.3529	0.3573	0.0263	0.0172
	Mean - 3 Sigma	0.0257	0.0258	-8.8343	-8.8630	0.2352	0.2632
	Mean + 3 Sigma	0.0319	0.0324	-6.7169	-6.7190	0.3932	0.3662

		** PG2 Lower Threshold Offset from VFB		* PG2 Low Hysteresis		** PG1 Upper Threshold Offset from VFB	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	-7.667	-7.672	0.314	0.303	7.046	7.041
	1	-7.157	-7.175	0.299	0.289	7.030	7.106
	2	-7.664	-7.645	0.325	0.336	7.149	7.131
	3	-7.859	-7.788	0.337	0.350	6.743	6.755
	4	-7.905	-7.932	0.349	0.338	6.836	6.827
	5	-7.188	-7.187	0.334	0.323	6.363	6.327
	6	-7.416	-7.427	0.268	0.347	7.356	7.382
	Min	-7.9055	-7.9316	0.2679	0.2888	6.3633	6.3267
	Max	-7.1572	-7.1748	0.3493	0.3498	7.3557	7.3823
	Mean	-7.5317	-7.5256	0.3187	0.3305	6.9127	6.9215
	Std. Dev	0.3274	0.3147	0.0299	0.0225	0.3472	0.3690
	Mean - 3 Sigma	-8.5138	-8.4696	0.2289	0.2628	5.8712	5.8145
	Mean + 3 Sigma	-6.5496	-6.5816	0.4084	0.3981	7.9541	8.0286

		* PG1 HI Hysteresis		** PG2 Upper Threshold Offset from VFB		* PG2 HI Hysteresis	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	0.308	0.278	7.064	7.079	0.308	0.316
	1	0.331	0.301	7.256	7.210	0.293	0.308
	2	0.308	0.330	7.093	7.095	0.293	0.323
	3	0.324	0.317	6.972	7.025	0.308	0.309
	4	0.354	0.324	6.617	6.562	0.278	0.331
	5	0.286	0.339	7.014	6.990	0.301	0.316
	6	0.323	0.301	7.366	7.328	0.263	0.279
	Min	0.2860	0.3008	6.6171	6.5618	0.2634	0.2786
	Max	0.3537	0.3389	7.3656	7.3281	0.3082	0.3312
	Mean	0.3209	0.3186	7.0530	7.0349	0.2895	0.3110
	Std. Dev	0.0226	0.0155	0.2602	0.2632	0.0161	0.0181
	Mean - 3 Sigma	0.2529	0.2721	6.2723	6.2454	0.2411	0.2566
	Mean + 3 Sigma	0.3888	0.3651	7.8337	7.8244	0.3378	0.3653

		* SYNC_Threshold RampDown		* SYNC_Threshold RampUp		*Source I_Vc1 at FB-200mV @ Vin=6V Vc=1.25V	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	0.934	0.934	1.181	1.181	-158.008	-157.611
	1	0.916	0.910	1.157	1.149	-158.433	-157.523
	2	0.904	0.892	1.133	1.116	-147.003	-146.805
	3	0.904	0.892	1.124	1.116	-160.407	-158.534
	4	0.892	0.880	1.108	1.100	-154.742	-154.242
	5	0.892	0.880	1.108	1.100	-149.277	-149.051
	6	0.904	0.898	1.133	1.124	-152.069	-151.185
	Min	0.8916	0.8795	1.1084	1.1004	-160.4067	-158.5340
	Max	0.9157	0.9096	1.1566	1.1486	-147.0032	-146.8053
	Mean	0.9016	0.8916	1.1272	1.1178	-153.6550	-152.8901
	Std. Dev	0.0091	0.0114	0.0181	0.0179	5.2063	4.6865
	Mean - 3 Sigma	0.8744	0.8573	1.0729	1.0641	-169.2740	-166.9496
	Mean + 3 Sigma	0.9288	0.9259	1.1814	1.1715	-138.0360	-138.8305

		*Sink I_Vc1 at FB+200mV @ Vin=6V Vc=1.25V		*Gm Error Amp1 @ Vin=6V Vc=1.25V		*VC-SW1Gain[(T2300.1+T2300.3)/T4400.0], dummy@hot	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	156.337	156.557	785.863	785.418	6.225	6.211
	1	154.719	155.496	782.880	782.548	6.189	6.443
	2	141.840	141.097	722.109	719.756	6.192	6.473
	3	157.823	158.528	795.575	792.655	6.225	6.515
	4	153.045	153.400	769.468	769.104	6.246	6.534
	5	146.425	147.386	739.253	741.092	6.135	6.412
	6	148.092	148.608	750.402	749.483	6.109	6.350
	Min	141.8403	141.0971	722.1088	719.7560	6.1090	6.3501
	Max	157.8233	158.5280	795.5751	792.6549	6.2456	6.5335
	Mean	150.3242	150.7525	759.9479	759.1064	6.1827	6.4543
	Std. Dev	5.9181	6.3107	27.7020	27.3516	0.0522	0.0678
	Mean - 3 Sigma	132.5698	131.8204	676.8420	677.0517	6.0261	6.2508
	Mean + 3 Sigma	168.0785	169.6846	843.0539	841.1611	6.3394	6.6578

		*Source I_Vc2 at FB-200mV @ Vin=6V Vc=1.25V		*Sink I_Vc2 at FB+200mV @ Vin=6V Vc=1.25V		*Gm Error Amp2 @ Vin=6V Vc=1.25V	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	-158.121	-157.623	156.387	156.488	786.269	785.278
	1	-158.321	-157.604	154.457	155.172	781.944	781.940
	2	-147.216	-146.730	142.134	140.791	723.374	718.805
	3	-160.076	-158.440	157.623	158.472	794.248	792.281
	4	-154.704	-154.335	152.845	153.300	768.874	769.088
	5	-149.708	-149.057	146.537	147.504	740.612	741.404
	6	-152.531	-151.360	148.355	148.839	752.214	750.497
	Min	-160.0757	-158.4404	142.1338	140.7914	723.3735	718.8046
	Max	-147.2156	-146.7304	157.6234	158.4718	794.2478	792.2806
	Mean	-153.7591	-152.9213	150.3252	150.6797	760.2108	759.0024
	Std. Dev	4.9465	4.6923	5.6924	6.3089	26.4988	27.3247
	Mean - 3 Sigma	-168.5987	-166.9981	133.2480	131.7531	680.7143	677.0283
	Mean + 3 Sigma	-138.9195	-138.8444	167.4024	169.6063	839.7073	840.9766

		*VC-SW2Gain[(T2350.1+T2350.3)/T4450.0], dummy@hot		* Feedback Voltage Line Regulation 1		* Feedback Voltage Line Regulation 2	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	6.336	6.322	0.002	0.002	0.002	0.002
	1	6.509	6.825	0.002	0.002	0.002	0.002
	2	6.330	6.665	0.002	0.002	0.002	0.002
	3	6.499	6.831	0.002	0.002	0.001	0.002
	4	6.534	6.855	0.001	0.001	0.001	0.001
	5	6.481	6.807	0.002	0.002	0.002	0.001
	6	6.321	6.639	0.002	0.002	0.001	0.002
	Min	6.3212	6.6389	0.0014	0.0011	0.0010	0.0010
	Max	6.5343	6.8553	0.0022	0.0021	0.0020	0.0018
	Mean	6.4458	6.7705	0.0019	0.0018	0.0015	0.0015
	Std. Dev	0.0948	0.0935	0.0003	0.0004	0.0003	0.0003
	Mean - 3 Sigma	6.1614	6.4900	0.0010	0.0007	0.0005	0.0006
	Mean + 3 Sigma	6.7301	7.0510	0.0028	0.0029	0.0024	0.0025

		* BIAS_pin_Current_Consumption		** SS1_Pin_Current		** SS2_Pin_Current	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	5.385	5.405	-1.877	-1.883	-1.882	-1.880
	1	5.475	5.597	-1.863	-1.907	-1.845	-1.880
	2	5.470	5.594	-1.830	-1.883	-1.793	-1.854
	3	5.504	5.626	-1.851	-1.898	-1.833	-1.870
	4	5.461	5.588	-1.651	-1.695	-1.646	-1.685
	5	5.514	5.645	-1.784	-1.824	-1.757	-1.793
	6	5.512	5.627	-1.895	-1.938	-1.871	-1.907
	Min	5.4607	5.5876	-1.8948	-1.9383	-1.8709	-1.9071
	Max	5.5138	5.6449	-1.6514	-1.6945	-1.6459	-1.6853
	Mean	5.4892	5.6129	-1.8124	-1.8575	-1.7908	-1.8317
	Std. Dev	0.0233	0.0229	0.0871	0.0882	0.0816	0.0811
	Mean - 3 Sigma	5.4193	5.5443	-2.0735	-2.1222	-2.0355	-2.0751
	Mean + 3 Sigma	5.5591	5.6816	-1.5512	-1.5929	-1.5460	-1.5883

		** Datasheet_Osc_High [Rt=15K]		** Datasheet_Osc_Low [Rt=35.7K]		** Datasheet_Osc_Low [Rt=133K]	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	1992.141	1994.838	990.601	991.302	303.871	303.899
	1	2033.869	2031.552	1000.696	1002.023	300.071	301.573
	2	2003.063	1998.961	987.135	987.983	297.800	298.861
	3	1996.636	1989.923	991.893	989.829	304.537	304.117
	4	2012.234	2002.135	998.092	994.263	302.650	301.861
	5	2019.776	2011.803	1000.603	997.833	300.133	299.149
	6	2038.231	2028.188	1004.499	999.712	301.186	299.205
	Min	1996.6356	1989.9233	987.1351	987.9825	297.8000	298.8609
	Max	2038.2308	2031.5522	1004.4989	1002.0233	304.5373	304.1173
	Mean	2017.3015	2010.4270	997.1531	995.2738	301.0629	300.7943
	Std. Dev	16.5778	16.6390	6.4394	5.5792	2.3282	2.0860
	Mean - 3 Sigma	1967.5681	1960.5101	977.8350	978.5363	294.0783	294.5364
	Mean + 3 Sigma	2067.0348	2060.3440	1016.4713	1012.0113	308.0474	307.0523

		* Spread_Spectrum_Threshold [1Mhz] CH1		* Spread_Spectrum_Modulation_Pct[At threshold] CH1		* Spread_Spectrum_3kHz CH1	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	2.550	2.550	16.804	16.844	5.435	5.102
	1	2.500	2.500	17.260	17.394	5.556	5.682
	2	2.500	2.500	18.287	17.916	4.717	4.808
	3	2.500	2.450	17.566	17.384	5.102	5.102
	4	2.550	2.550	17.874	18.112	4.902	5.556
	5	2.500	2.450	17.279	17.489	4.545	4.717
	6	2.500	2.450	17.330	17.415	5.814	1.908
	Min	2.5000	2.4500	17.2602	17.3837	4.5455	1.9084
	Max	2.5500	2.5500	18.2866	18.1121	5.8140	5.6818
	Mean	2.5083	2.4833	17.5995	17.6183	5.1060	4.6287
	Std. Dev	0.0204	0.0408	0.4096	0.3148	0.4920	1.3880
	Mean - 3 Sigma	2.4471	2.3609	16.3707	16.6737	3.6299	0.4649
	Mean + 3 Sigma	2.5696	2.6058	18.8283	18.5628	6.5821	8.7926

		* Spread_Spectrum_Threshold [1Mhz] CH2		* Spread_Spectrum_Modulation_Pct[At threshold] CH2		* Spread_Spectrum_3kHz CH2	
Wafer	SN	PRE	30k	PRE	30k	PRE	30k
CTRL	40	2.550	2.550	16.667	17.508	6.757	6.757
	1	2.500	2.500	17.272	17.646	6.250	5.319
	2	2.500	2.500	18.436	18.780	6.757	6.944
	3	2.500	2.450	17.851	18.012	5.814	7.143
	4	2.550	2.500	18.094	18.105	2.212	5.556
	5	2.500	2.450	17.567	17.581	1.953	6.098
	6	2.500	2.450	17.456	17.376	2.155	2.252
	Min	2.5000	2.4500	17.2724	17.3760	1.9531	2.2523
	Max	2.5500	2.5000	18.4361	18.7799	6.7568	7.1429
	Mean	2.5083	2.4750	17.7794	17.9167	4.1902	5.5520
	Std. Dev	0.0204	0.0274	0.4339	0.5036	2.3032	1.7726
	Mean - 3 Sigma	2.4471	2.3928	16.4776	16.4060	-2.7194	0.2343
	Mean + 3 Sigma	2.5696	2.5572	19.0812	19.4274	11.0999	10.8697

















