

SINGLE EVENT EFFECTS TEST REPORT ADA4084-4S

February 2016

Radiation Test Report	
Product:	ADA4084-4S
Die Type:	ADA4084-4
Facilities:	RADEF, Univ. of Jyvaskyla, Finland
Tested:	Sept 2015 - Feb 2016

The RADTEST® DATA SERVICE is a compilation of radiation test results on Analog Devices' Space grade products. It is designed to assist customers in selecting the right product for applications where radiation is a consideration. Many products manufactured by Analog Devices, Inc. have been shown to be radiation tolerant to most tactical radiation environments. Analog Devices, Inc. does not make any claim to maintain or guarantee these levels of radiation tolerance without lot qualification test.

It is the responsibility of the Procuring Activity to screen products from Analog Devices, Inc. for compliance to Nuclear Hardness Critical Items (HCI) specifications.

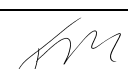
Warning:

Analog Devices, Inc. does not recommend use of this data to qualify other product grades or process levels. Analog Devices, Inc. is not responsible and has no liability for any consequences, and all applicable Warranties are null and void if any Analog Devices product is modified in any way or used outside of normal environmental and operating conditions, including the parameters specified in the corresponding data sheet. Analog Devices, Inc. does not guarantee that wafer manufacturing is the same for all process levels.

SINGLE EVENT EFFECTS TEST REPORT

Test Type:	Heavy ion
Test facility:	RADEF, University of Jyvaskyla, Finland
Test Date:	September 2015, February 2016
Part Type:	AD4084-4
Part Description:	Quad 30 V, Low Noise, Rail-to-Rail Input/Output, Low Power Operational Amplifiers
Part Manufacturer:	Analog Devices

Analog Devices PO No 45516080 dated 22/06/2015

Hirex reference :	HRX/SEE/0539	Issue : 03	Date :	February 18, 2016
Written by :	Mehdi Kaddour	Design Engineer		
Authorized by:	F.X. Guerre	Study Manager		

RESULTS SUMMARY**Facility**

RADEF, University of Jyväskylä, Finland

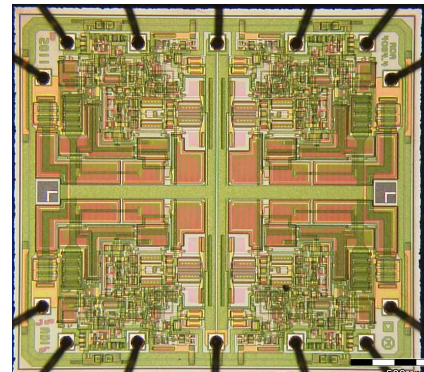
Test date

September 2015, February 2016, February 2016

Device description

Quad 30 V, Low Noise, Rail-to-Rail Input/Output, Low Power Operational Amplifiers

<u>Part type:</u>	AD4084-4
<u>Part number:</u>	ADA4084 – 4ARUZ
<u>Manufacturer:</u>	Analog Devices
<u>Package:</u>	TSSOP-14
<u>Samples used:</u>	6
<u>Top marking:</u>	logo 4084-4 A#313 1268
<u>Bottom marking:</u>	-
<u>Date code:</u>	1313
<u>Die dimensions:</u>	1.856 mm X 1.656 mm

**September 2015 SEL Results**

Device degradation (current supply increase and loss of functionality) have been observed during RUN019 and RUN021 when tested with $V_{+/-}$ set to 16.5V and Krypton (Eff. LET =32.1) at 125°C. Devices (2) passed when tested with $V_{+/-}$ set to 15V and tilted Krypton (Eff. LET =50) at 125°C. After RUN031, before changing from board n°4 to board n°3, the functional test of the samples (Dut7 and Dut8) on board n°4 provided that outputs OUTB of Dut7 and OUTD of Dut8 have been degraded. The other outputs were all functional. Devices have been also degraded (RUN052) when tested with $V_{+/-}$ set to +/-15V and Xenon (Eff. LET = 60) at 125°C. Partially working devices (2) of board n°4 passed when tested with $V_{+/-}$ set to 5V and tilted Xenon (Eff. LET =80) at 125°C.

February 2016 SEL Results

No SEL nor degradation has been observed when tested with $V_d = +/-5V$ at a case temperature of 125°C with effective LETs of 60, 75 and 93MeV/(mg/cm²) on 4 samples.

DOCUMENTATION CHANGE NOTICE

Issue	Date	Page	Change Item	
01	28/10/2015	All	Original issue	
02	28/10/2015	10,11	Section 6 (SEE test results) : additional runs added	
03	18/02/2016		Results from additional testing (February 2016) added	

Contributors to this work:

Bendy Tanios
Mehdi Kaddour

Hirex Engineering
Hirex Engineering

SEE TEST REPORT

TABLE OF CONTENTS

1	INTRODUCTION	5
2	APPLICABLE AND REFERENCE DOCUMENTS.....	5
2.1	APPLICABLE DOCUMENTS.....	5
2.2	REFERENCE DOCUMENTS	5
3	DEVICE INFORMATION	6
3.1	DEVICE DESCRIPTION.....	6
3.2	SAMPLE IDENTIFICATION.....	6
3.3	SAMPLE PREPARATION AND EVALUATION OF DEAD LAYER THICKNESS	6
4	RADEF FACILITY	7
5	TEST SET-UP.....	8
5.1	AD4084-4 TEST PRINCIPLE AND CONDITIONS.....	8
6	SEE TEST RESULTS.....	10
6.1	SEL RESULTS	10
6.2	ADDITIONAL TESTING (FEBRUARY 2016) RESULTS	11
7	GLOSSARY	15

LIST OF FIGURES

Figure 1 – AD4084-4 device identification	6
Figure 2 - Heavy ion test set-up.....	8
Figure 3 – AD4084-4 bias condition.....	9
Figure 4 – Photo of test board	9

LIST OF TABLES

Table 1 – Ion beam setting	7
Table 2 - Voltage bias conditions applied to the 2 DUTs.....	8
Table 3 - Tester supply channel affectation.....	8
Table 4 - Run table for the AD4084-4, RADEF September 2015.....	10
Table 5 - Run table for the AD4084-4, RADEF February 2016	11

1 Introduction

This report presents the results of SEL Heavy Ions test program carried out on Analog Devices AD4084-4. On September 2015, February 2016, 6 samples were used for heavy ions testing at RADEF, University of Jyväskylä, Finland .This work was performed for Analog Devices, Greensboro under PO n° 45516080 dated 22/06/2015.

Additional testing was performed in February 2016 with +/-5V test configuration at a case temperature of 125°C.

2 Applicable and Reference Documents

2.1 Applicable Documents

AD-1. Datasheet: http://www.analog.com/media/en/technical-documentation/data-sheets/ADA4084-1_4084-2_4084-4.pdf

2.2 Reference Documents

RD-1. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100

3 **DEVICE INFORMATION**

3.1 **Device description**

AD4084-4 is a Quad 30 V, Low Noise, Rail-to-Rail Input/Output, Low Power Operational Amplifiers.

<u>Part type:</u>	AD4084-4
<u>Part number:</u>	ADA4084 – 4ARUZ
<u>Manufacturer:</u>	Analog Devices
<u>Package:</u>	TSSOP-14
<u>Samples used:</u>	6
<u>Top marking:</u>	logo 4084-4 A#313 1268
<u>Bottom marking:</u>	-
<u>Date code:</u>	1313
<u>Die dimensions:</u>	1.856 mm X 1.656 mm

3.2 **Sample identification**

16 AD4084-4 parts were delivered by Analog Devices, Greensboro. Samples were prepared and opened chemically to be tested to heavy ions. 6 samples were verified fully functional before the test campaign, and 6 were tested under irradiation.

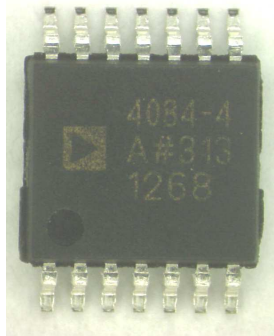


Photo 1 – Device top view

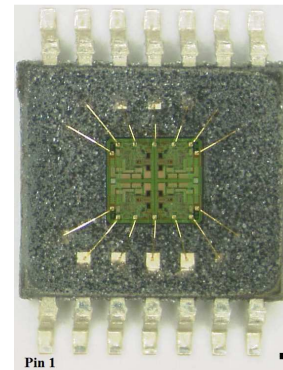


Photo 2 – Device delidded

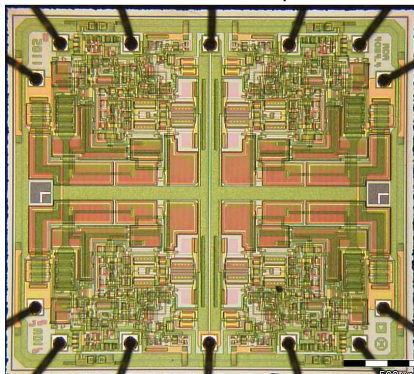


Photo 3 – die, full view

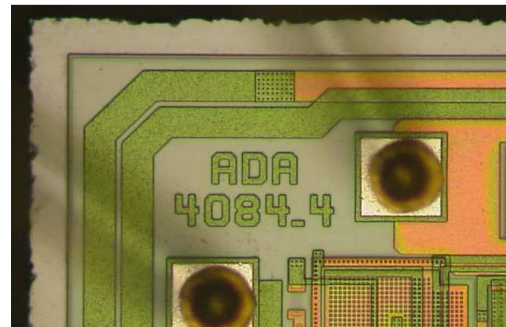


Photo 4 – Die marking #1

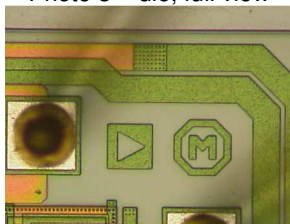


Photo 5 – Die marking #2

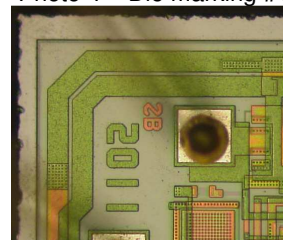


Photo 6 – Die marking #3

Figure 1 – AD4084-4 device identification

3.3 **Sample preparation and evaluation of dead layer thickness**

Samples were opened chemically.

Die micro-section results are given in appendix. Overall dead layer thickness on top of active zone is less or equal to 10 microns of equivalent silicon.

4 RADEF Facility

Test at the cyclotron accelerator was performed at University of Jyväskylä (JYFL) (Finland) under HIREX Engineering responsibility.

The facility includes a special beam line dedicated to irradiation studies of semiconductor components and devices. It consists of a vacuum chamber including component movement apparatus and the necessary diagnostic equipment required for the beam quality and intensity analysis.

The cyclotron is a versatile, sector-focused accelerator of beams from hydrogen to xenon equipped with three external ion sources: two electron cyclotron resonance (ECR) ion sources designed for high-charge-state heavy ions, and a multicusp ion source for intense beams of protons. The ECR's are especially valuable in the study of single event effects (SEE) in semiconductor devices. For heavy ions, the maximum energy attainable can be determined using the formula,

$$130 Q^2/M,$$

where Q is the ion charge state and M is the mass in Atomic Mass Units.

Test chamber

Irradiation of components is performed in a vacuum chamber with an inside diameter of 75 cm and a height of 81 cm.

The vacuum in the chamber is achieved after 15 minutes of pumping, and the inflation takes only a few minutes. The position of the components installed in the linear movement apparatus inside the chamber can be adjusted in the X, Y and Z directions. The possibility of rotation around the Y-axis is provided by a round table. The free movement area reserved for the components is 25 cm x 25 cm, which allows one to perform several consecutive irradiations for several different components without breaking the vacuum.

The assembly is equipped with a standard mounting fixture. The adapters required to accommodate the special board configurations and the vacuum feed-throughs can also be made in the laboratory's workshops. The chamber has an entrance door, which allows rapid changing of the circuit board or individual components.

A CCD camera with a magnifying telescope is located at the other end of the beam line to determine accurate positioning of the components. The coordinates are stored in the computer's memory allowing fast positioning of various targets during the test.

Beam quality control

For measuring beam uniformity at low intensity, a CsI(Tl) scintillator with a PIN-type photodiode readout is fixed in the mounting fixture. The uniformity is measured automatically before component irradiation and the results can be plotted immediately for more detailed analysis.

A set of four collimated PIN-CsI(Tl) detectors is located in front of the beam entrance. The detectors are operated with step motors and are located at 90 degrees with respect to each other. During the irradiation and uniformity scan they are set to the outer edge of the beam in order to monitor the stability of the homogeneity and flux.

Two beam wobblers and/or a 0.5 microns diffusion Gold foil can be used to achieve good beam homogeneity. The foil is placed 3 m in front of the chamber. The wobbler-coils vibrate the beam horizontally and vertically, the proper sweeping area being attained with the adjustable coil-currents.

Dosimetry

The flux and intensity dosimeter system contains a Faraday cup, several collimators, a scintillation counter and four PIN-CsI(Tl) detectors. Three collimators of different size and shape are placed 25 cm in front of the device under test. They can be used to limit the beam to the active area to be studied.

At low fluxes a plastic scintillator with a photomultiplier tube is used as an absolute particle counter. It is located behind the vacuum chamber and is used before the irradiation to normalize the count rates of the four PIN-CsI(Tl) detectors.

Ion	LET ^{SRIM} at surface [MeV.cm ² .mg ⁻¹]	Range [μm]	Beam energy [MeV]
²⁰ Ne ⁶⁺	3.63	146	186
⁴⁰ Ar ¹²⁺	10.2	118	372
⁵⁶ Fe ¹⁵⁺	18.5	97	523
⁸² Kr ²²⁺	32.1	94	768
¹³¹ Xe ³⁵⁺	60.0	89	1217

SRIM-2003.26

Table 1 – Ion beam setting

5 Test Set-up

Test system Figure 2 shows the principle of the Heavy Ion test system.

The test system is based on a Virtex5 FPGA (Xilinx). It runs at 50 MHz. The test board has 168 I/Os which can be configured using several I/O standards.

The test board includes the voltage/current monitoring and the latch-up management of the DUT power supplies up to 24 independent channels.

The communication between the test chamber and the controlling computer is effectively done by a 100 Mbit/s Ethernet link which safely enables high speed data transfer.

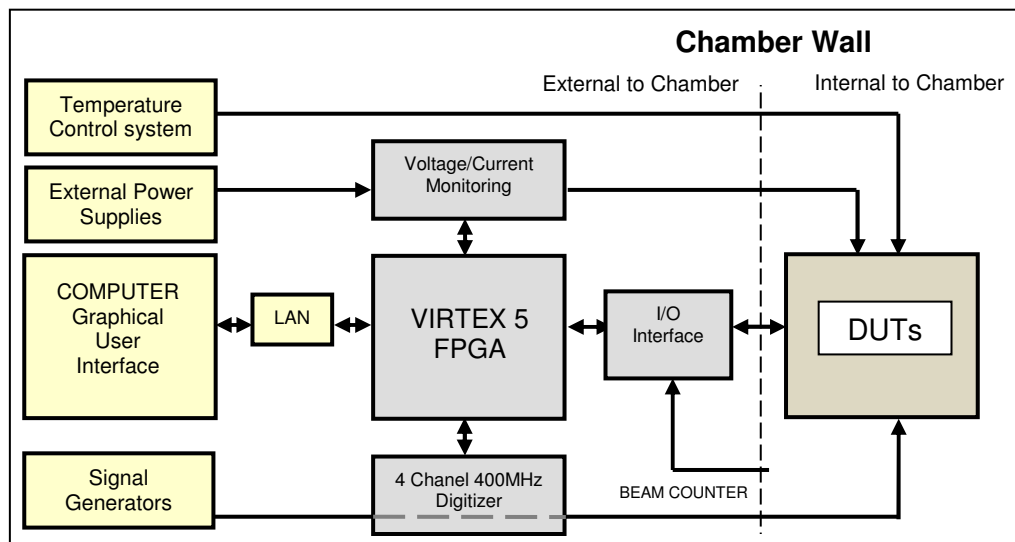


Figure 2 - Heavy ion test set-up

5.1 AD4084-4 test principle and conditions

In order to test the AD4084-4, one daughter board was designed. 2 DUTs were mounted on this board (Dut7 and Dut8 positions) and bias conditions are given in Figure 3 and Table 2. Table 3 gives the tester supply channel number used in the tester report.

DUT heating is performed with a thermal resistor in contact with daughter board back side using a thermal conductive paste. The temperature is regulated thanks to a thermocouple sensor put on top of the DUT package.

SEL event is detected when the supply current is over a configurable threshold (in the present case set to 100 mA for V+ and -100mA for V-) and processed (the power supplies are cut off during a configurable wait time, in the present case set to 1s).

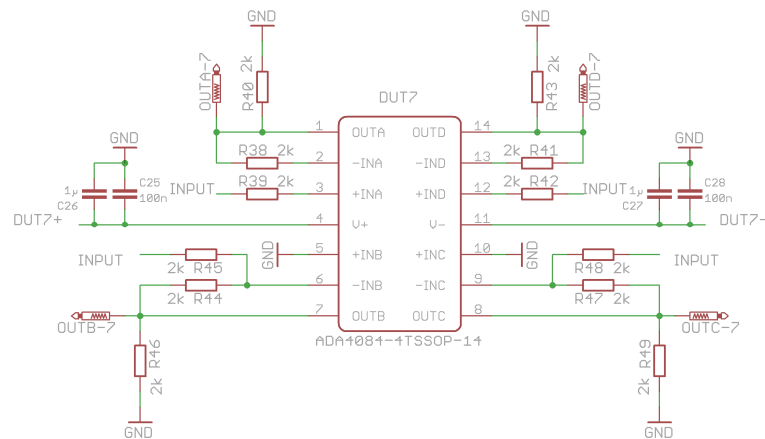
The tester monitors independently the 2 DUTs supplies at the same time. If an SEL is detected on 1 supply channel, the tester system records current/voltage on all channels.

Supply name	voltage
DUT_V+	+16.5V/15V/5V/3V
DUT_V-	-16.5V/-15V/-5V/-3V
INPUT	Sine wave $\pm 1V$ at 100 KHz

Table 2 - Voltage bias conditions applied to the 2 DUTs

Supply name	Tester supply channel #
DUT7_V+	13
DUT7_V-	14
DUT8_V+	15
DUT8_V-	16
INPUT	17

Table 3 - Tester supply channel affectation



Input: Sine wave $\pm 1V$ at 100 KHz

Supply voltage: $\pm 16.5V$ max and ± 15.0 and $\pm 5.0V$ and $\pm 3V$ if SEL events are monitored

Load resistance = 2 k Ω

Channel A gain set to +1

Channel B gain set to -1

Channel C gain set to -1

Channel D gain set to +1

Figure 3 – AD4084-4 bias condition

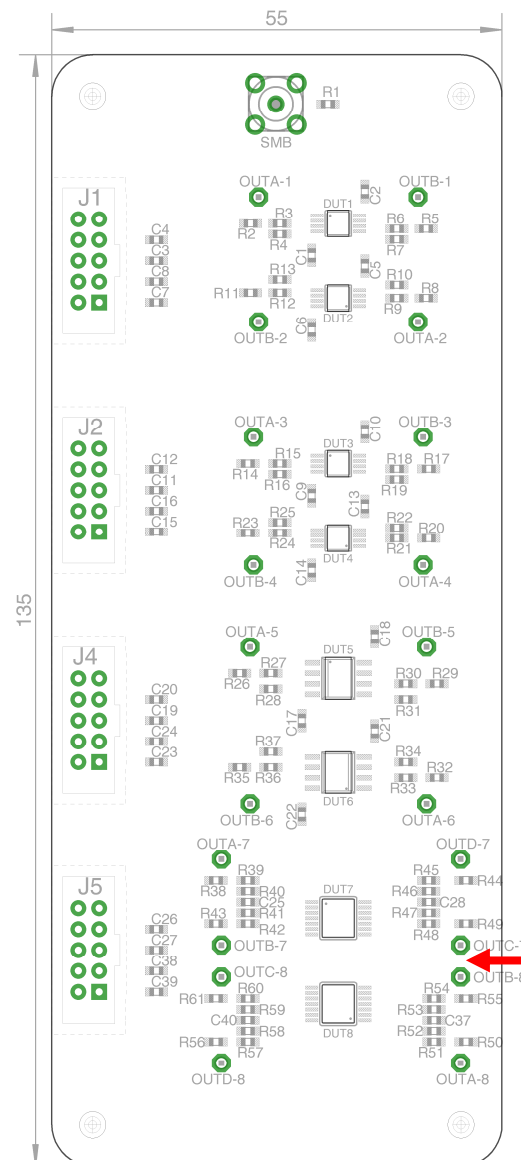
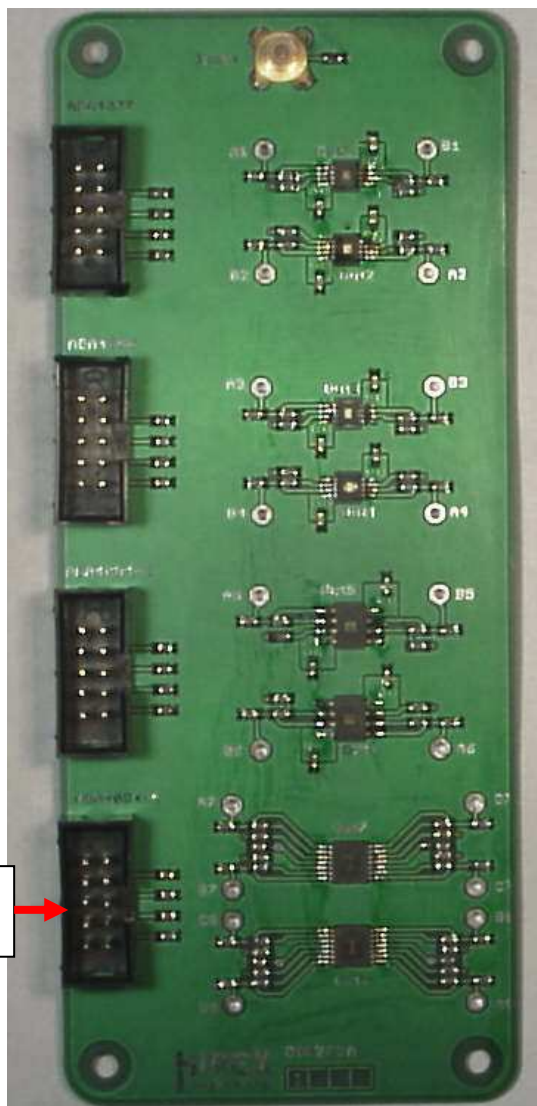


Figure 4 – Photo of test board

6 SEE test results

Runs performed are listed in Table 4.

3 boards have been tested with 2 AD4084-4 samples mounted on each board (Dut7 and Dut8 positions). Each time before changing board under test, an additional functional test (not required in the specifications) of the samples was performed to check the device functionality. This functional test consists in driving the input with a sine wave and checking with an oscilloscope the outputs of the device.

6.1 SEL Results

Facility	medium	hirex_run_number	Facility_run_number	board_id	dut_part_number under test	power_config	test_mode	temperature (° C)	Ion	LET (MeV/(mg/cm2))	roll	tilt	run_duration (s)	achieved fluence (ions/cm2)	eff. LET (MeV/(mg/cm2))	dut_comment
RADEF	vacuum	2	2	2	7,8	16.5V	SEL	105	Ar	10.2	0	0	273	1.00E+07	10.2	No SEL
RADEF	vacuum	8	8	2	7,8	16.5V	SEL	125	Ar	10.2	0	0	282	1.00E+07	10.2	No SEL
RADEF	vacuum	9	9	3	7,8	16.5V	SEL	125	Ar	10.2	0	0	328	1.00E+07	10.2	No SEL
RADEF	vacuum	12	12	3	7,8	16.5V	SEL	125	Fe	18.5	0	0	433	1.00E+07	18.5	No SEL
Functional test of board 3 : OK																
RADEF	vacuum	15	15	4	7,8	16.5V	SEL	125	Fe	18.5	0	0	346	1.00E+07	18.5	No SEL
RADEF	vacuum	19	19	4	7,8	16.5V	SEL	125	Kr	32.1	0	0	304	4.58E+06	32.1	SEL, board4, dut8 degraded
RADEF	vacuum	20	20	4	7,8	16.5V	SEL	125	Kr	32.1	0	0	345	1.00E+07	32.1	board4, dut8 degraded
RADEF	vacuum	21	21	4	7,8	16.5V	SEL	125	Kr	32.1	0	0	109	3.84E+06	32.1	SEL, board4, dut7 degraded
RADEF	vacuum	22	22	4	7,8	15V	SEL	125	Kr	32.1	0	0	305	1.00E+07	32.1	No SEL
RADEF	vacuum	25	25	4	7,8	15V	SEL	125	Kr	32.1	0	37	346	1.00E+07	40.2	No SEL
RADEF	vacuum	31	31	4	7,8	15V	SEL	125	Kr	32.1	0	50	133	1.01E+07	49.9	No SEL
Functional test of board 4: OUTB of Dut7 (OUTB7) and OUTD of Dut8 (OUTD8) are not functional. All the other outputs are functional.																
RADEF	vacuum	32	32	3	7,8	15V	SEL	125	Kr	32.1	0	0	130	1.00E+07	32.1	No SEL
RADEF	vacuum	33	33	3	7,8	15V	SEL	125	Kr	32.1	0	37	160	1.00E+07	40.2	No SEL
RADEF	vacuum	34	34	3	7,8	15V	SEL	125	Kr	32.1	0	50	196	1.01E+07	49.9	No SEL
RADEF	vacuum	52	52	3	7,8	15V	SEL	125	Xe	60	0	0	50	2.48E+06	60	SEL, board3, dut7 & 8 degraded
Functional test of board 3: Dut7 and Dut8 not functional																
RADEF	vacuum	65	65	4	7,8	5V	SEL	125	Xe	60	0	0	446	1.00E+07	60	No SEL
RADEF	vacuum	66	66	4	7,8	5V	SEL	125	Xe	60	0	42	595	1.00E+07	80.74	No SEL

Table 4 - Run table for the AD4084-4, RADEF September 2015

Device degradation (current supply increase and loss of functionality) have been observed during RUN019, RUN020 and RUN021 when tested with V_{+/-} set to 16.5V and Krypton (Eff. LET =32.1) at 125°C.

Devices (2) passed when tested with V_{+/-} set to 15V and tilted Krypton (Eff. LET =50) at 125°C.

After RUN031, before changing from board n°4 to board n°3, the functional test of the samples (Dut7 and Dut8) on board n°4 provided that outputs OUTB of Dut7 and OUTD of Dut8 have been degraded. The other outputs were all functional.

Devices have been also degraded (RUN052) when tested with V_{+/-} set to +/-15V and Xenon (Eff. LET = 60) at 125°C.

Partially working devices (2) of board n°4 passed when tested with V_{+/-} set to 5V and tilted Xenon (Eff. LET =80) at 125°C.

6.2 Additional testing (February 2016) results

Detailed results on the runs performed with VD =+/-5V at a case temperature of 125°C and with effective LET of 60,75 and 93 MeV/(mg/cm²) are presented in Table 5.

2 DUT samples are tested at the same time. 4 samples (2 times 2 samples) in total have been tested using 2 boards A and B.

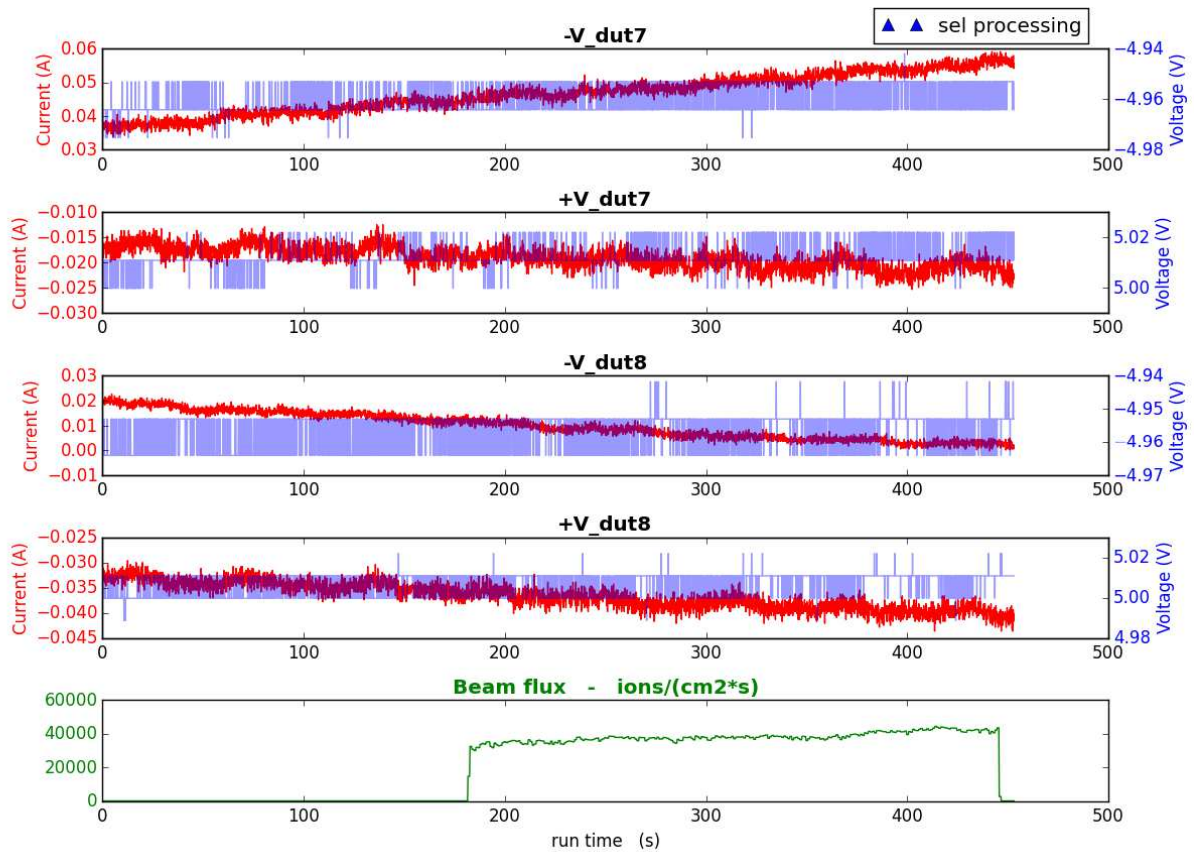
For each run, Vd+ and Vd- UI plots for the 2 samples together with the beam flux are shown in the next pages.

For both voltage and current records, a potential offset can be present but what is important to look at is the variation that is assumed to be constant. In any case, UI sources voltages are checked with a multimeter before starting the test runs.

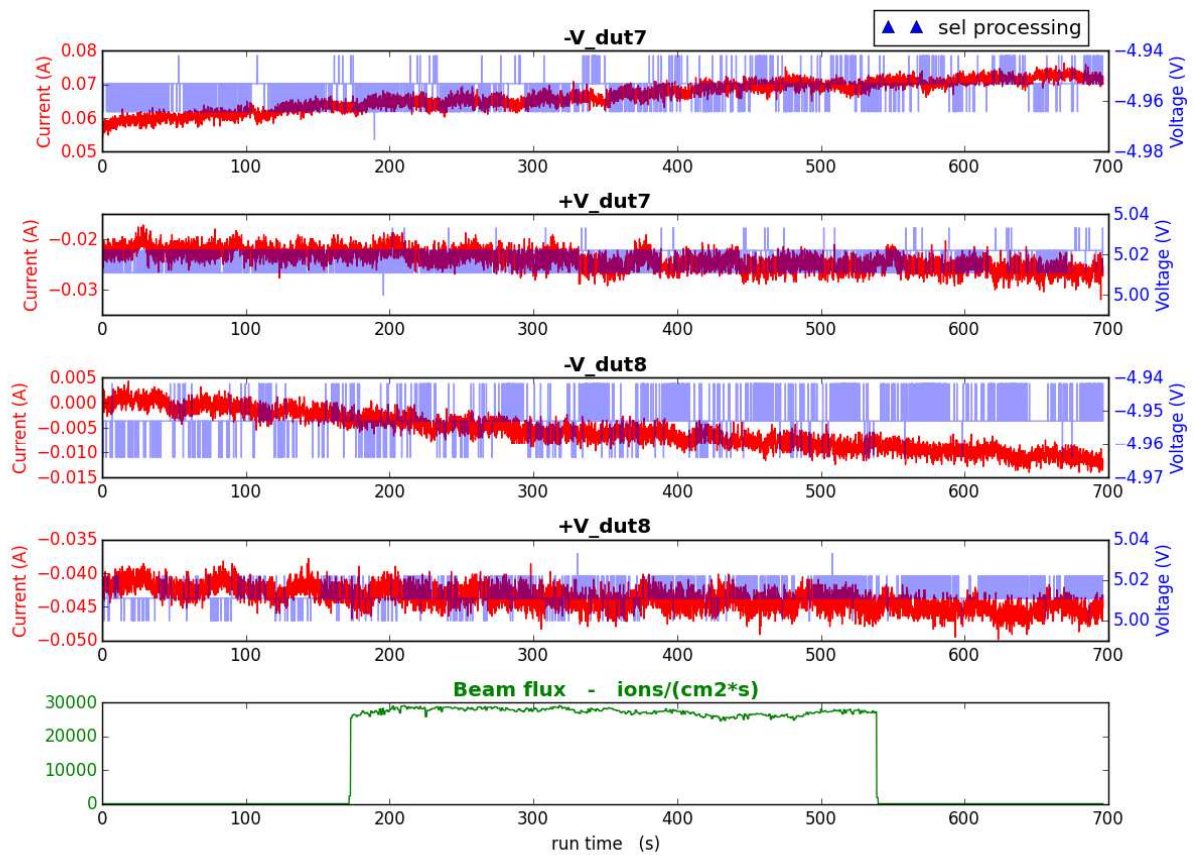
No SEL nor part degradation has been observed in this configuration.

Facility	medium	run_number	Facility_run_number	board_id	dut_part_id	dut_partnumber	power_config	temperature	Ion	LET	roll	tilt	eff. LET	run_duration	entered_fluence	SEL
RADEF	vacuum	1	24	A	ADA4084-4	7,8	5V	125	Xe	60	0	0	60	264	1.00E+07	0
RADEF	vacuum	2	25	A	ADA4084-4	7,8	5V	125	Xe	60	0	37	75	366	1.00E+07	0
RADEF	vacuum	3	26	A	ADA4084-4	7,8	5V	125	Xe	60	0	50	93	419	1.00E+07	0
RADEF	vacuum	8	30	B	ADA4084-4	7,8	5V	125	Xe	60	0	0	60	209	1.00E+07	0
RADEF	vacuum	9	31	B	ADA4084-4	7,8	5V	125	Xe	60	0	37	75	273	1.00E+07	0
RADEF	vacuum	10	32	B	ADA4084-4	7,8	5V	125	Xe	60	0	50	93	302	1.00E+07	0

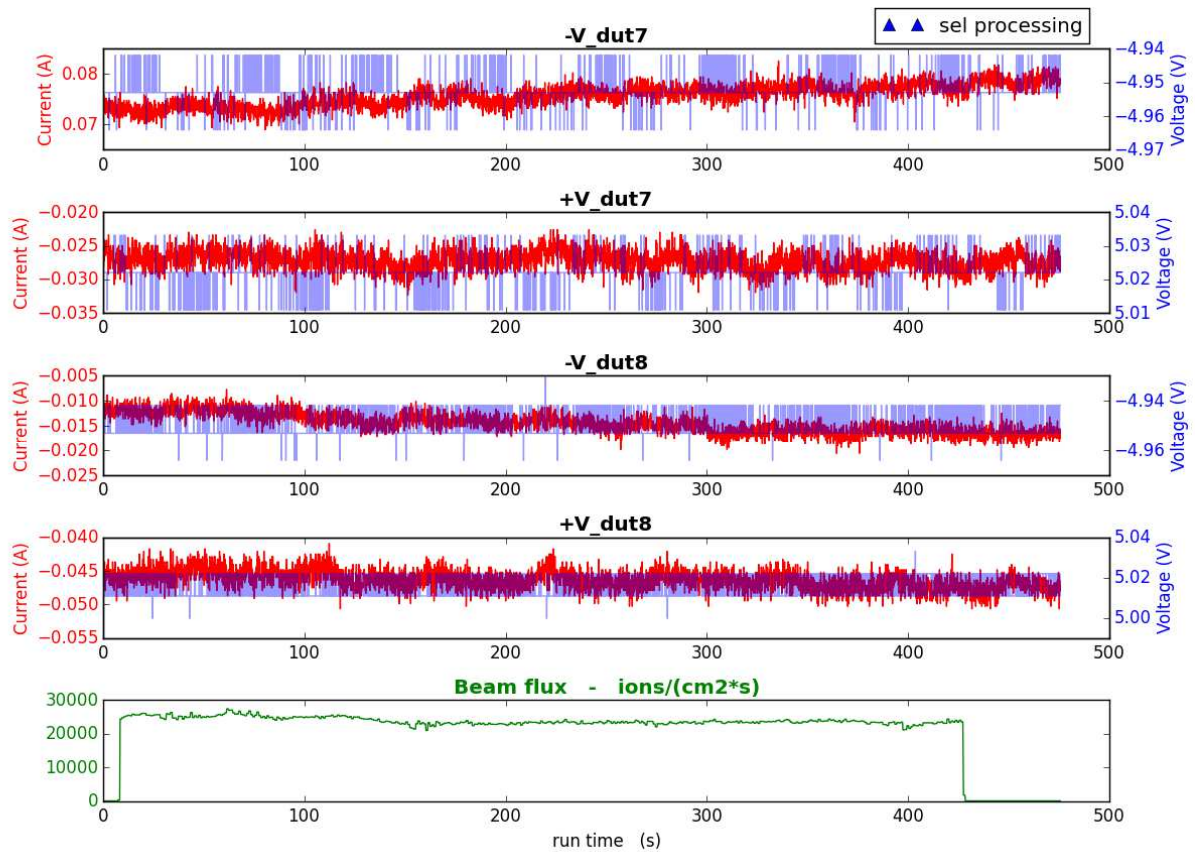
Table 5 - Run table for the AD4084-4, RADEF February 2016



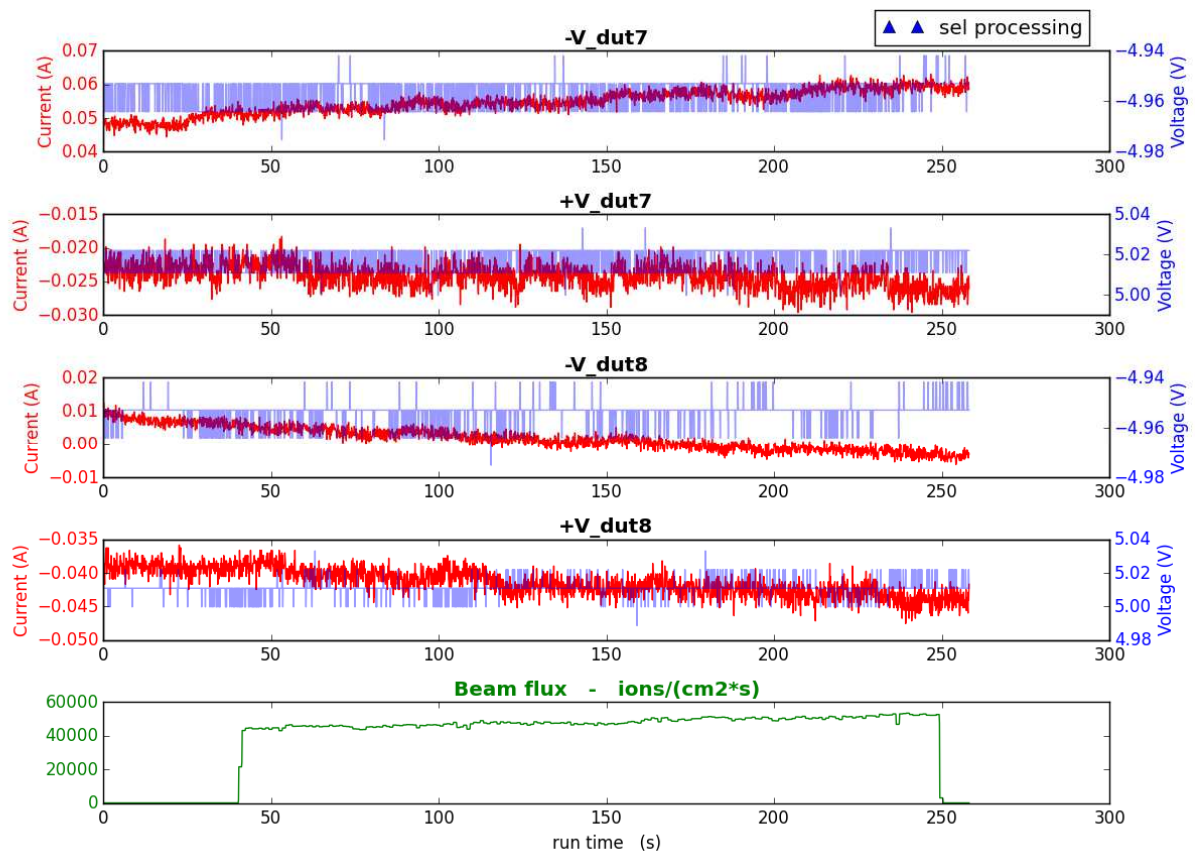
RUN001



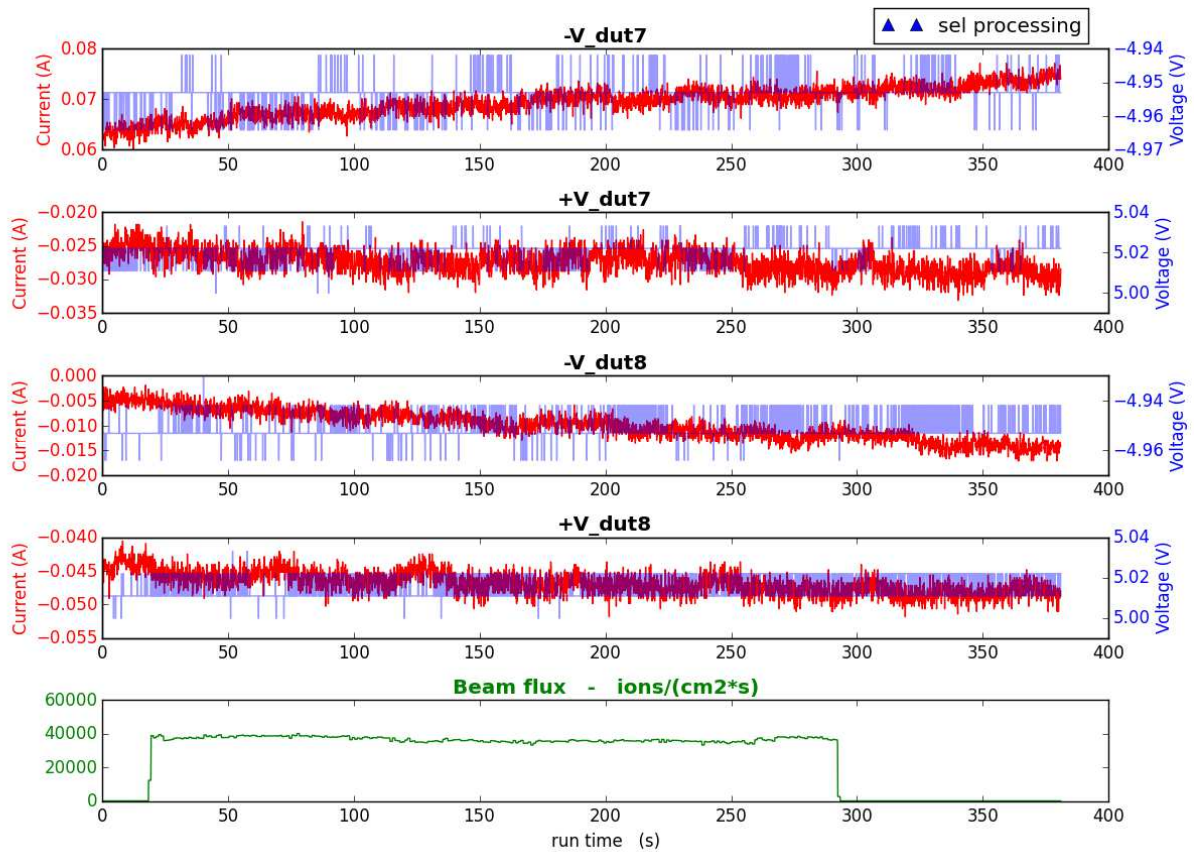
RUN002



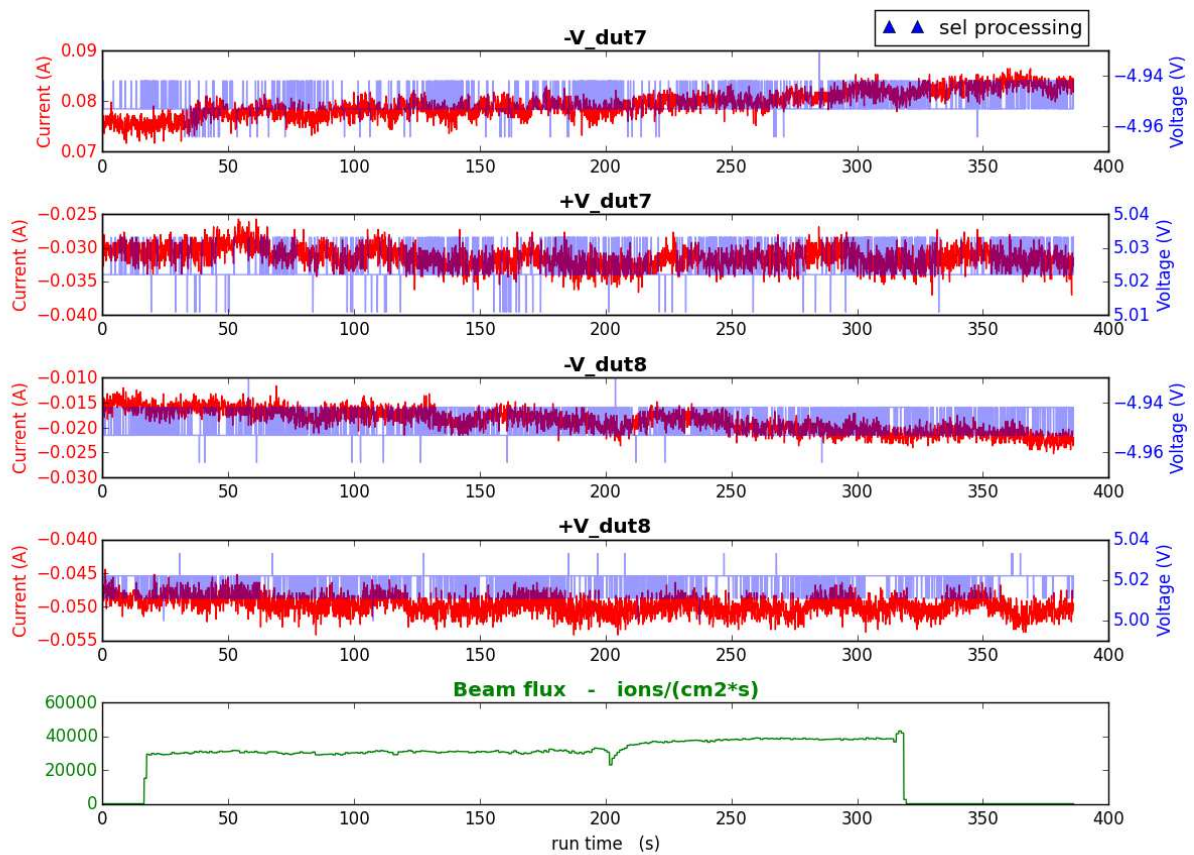
RUN003



RUN008



RUN009



RUN010

7 Glossary

Most of the definitions here below are from JEDEC standard JESD89A

DUT: Device under test.

Fluence (of particle radiation incident on a surface): The total amount of particle radiant energy incident on a surface in a given period of time, divided by the area of the surface.
In this document, Fluence is expressed in ions per cm².

Flux: The time rate of flow of particle radiant energy incident on a surface, divided by the area of that surface.
In this document, Flux is expressed in ions per cm²*s.

Single-Event Effect (SEE): Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike.

Single-event effects include single-event upset (SEU), multiple-bit upset (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL).

Single-Event Transient (SET): A soft error caused by the transient signal induced by a single energetic particle strike.

Single-Event Latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality.

SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.

An example of SEL in a CMOS device is when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.

Single-Event Latch-up (SEL) cross-section: the number of events per unit fluence. For chip SEL cross-section, the dimensions are cm² per chip.

Error cross-section: the number of errors per unit fluence. For device error cross-section, the dimensions are cm² per device. For bit error cross-section, the dimensions are cm² per bit.

Tilt angle: tilt angle, rotation axis of the DUT board is perpendicular to the beam axis; roll angle, board rotation axis is parallel to the beam axis