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SINGLE EVENT LATCHUP TEST REPORT AD9254S

July 2012

Radiation Test Report	
Product:	AD9254S
Effective LET:	9.7 - 86 MeV-cm^2/mg
Fluence:	1E7 Ions/cm^2
Facilities:	Lawrence Berkeley National Laboratories
Tested:	December 7, 2011 February 16, 2012 April 5, 2012

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Single Event Latch-up Testing of the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter for Analog Devices

Customer: Analog Devices (PO# 45360761)

RAD Job Number: 11-630

Part Types Tested: Analog Devices AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The units were tested on December 7th, 2011, February 16th, 2012, and April 5th, 2012. All references to tests a, b, and c refer to these dates, respectively.

Traceability Information: Lot Date Code: N/A, parts arrived unmarked from Analog Devices; see a photograph of sample unit-under-test in Appendix A.

Quantity of Parts for Testing: Four units were exposed to 10^7 ion/cm^2 at a maximum LET of approximately 86MeV-cm^2/mg using worst case bias conditions and a variety of device temperatures

Pre-Irradiation Burn-In: Units-under-test were not burned-in prior to the SEL testing.

Referenced Test Standard(s): ASTM F1192, EIA/JESD57

Electrical Test Conditions: Supply current monitored during exposure.

Test Software / Hardware: ICC.XLS, See Appendix C, Table C.1 for a list of test equipment and calibration dates.

Bias Conditions: All units-under-test were biased during heavy ion irradiation using supply potentials in-line with Analog Devices burn-in conditions. These conditions were in general accordance with ASTM F1192 and EIA/JESD57. See Appendix B for the details of the bias conditions and schematics of the test boards.

Ion Energy and LET Ranges: Effective LETs of approximately of between 9.7 and 86 MeV-cm^2/mg using the 10MeV/n beam at LBNL. Minimum range for all LETs is 50µm in silicon to the Bragg Peak.

Heavy Ion Flux and Maximum Fluence Levels: Flux of approximately 1 to 2x10^5 ions/cm^2. All devices were exposed to a minimum 10^7 ions/cm^2 at each LET.

Facility and/or Radiation Source: Lawrence Berkeley National Laboratories (LBNL) Berkeley, CA (10MeV/n beam).

Irradiation Temperature: A maximum of 110°C case temperature was used in testing, but lower temperatures were used as well.

SEL Test Result: The AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter latched up at LETs of 37 MeV-cm^2/mg and above at room temperature. The AD9254 latched up at LETs of 30 MeV-cm^2/mg and above at 110°C. SEFIs were observed at all LETs and temperatures.

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1.0. Overview and Background

It is well known that heavy ion exposure can cause temporary and/or permanent damage in electronic devices. The damage can occur through various mechanisms including single event latch-up (SEL), single event burnout (SEB) and single event gate rupture (SEGR). An SEL event occurs when a parasitic npnp feedback latch structure becomes biased into the on state due to a dense track of electron-hole pairs created along the heavy ion path in silicon. This latch-up is self-sustaining since there is a positive feedback path created and requires a power cycle to reset. A single event latch-up can lead to single event burnout if the current draw from the SEL event is sufficient to damage the junction and/or bond wire. The damage is worse and/or becomes evident with increasing linear energy transfer (LET) and fluence. The two test standards usually used to govern this testing are ASTM F1192 and EIA/JESD57. This destructive testing is usually performed at the maximum datasheet voltage and temperature to a total fluence of not less than 1E7ion/cm^2.

2.0. Single Event Latch-Up Test Apparatus

The single event latch-up testing described in this final report was performed at the Lawrence Berkeley National Laboratories (LBNL) using the 88-Inch Cyclotron. The 88-Inch Cyclotron is operated by the University of California for the US Department of Energy (DOE) and is a K=140 sector-focused cyclotron with both light- and heavy-ion capabilities. Protons and other light-ions are available at high intensities (10-20pμA) up to maximum energies of 55 MeV (protons), 65 MeV (deuterons), 135 MeV (3He) and 140 MeV (4He). Most heavy ions through uranium can be accelerated to maximum energies, which vary with the mass and charge state.

For the SEL testing described in this final report the units-under-test were be placed in the Cave 4B vacuum chamber aligned with the heavy ion beam line. The test platter in the vacuum chamber has full x and y alignment capabilities along with 2-dimensional rotation, allowing for a variety of effective LETs for each ion. For SEE testing Lawrence Berkeley Laboratories provides the dosimetry via a local control computer running a Lab View based program. Each ion is calibrated just prior to use using five photomultiplier tubes (PMTs). Four of the five PMTS are used during the test to provide the beam statistics, while the center PMT is removed following calibration. Figure 2.1 shows an illustration of the LBL facility; including the location of Cave 4B, where the heavy ion SEE testing takes place.

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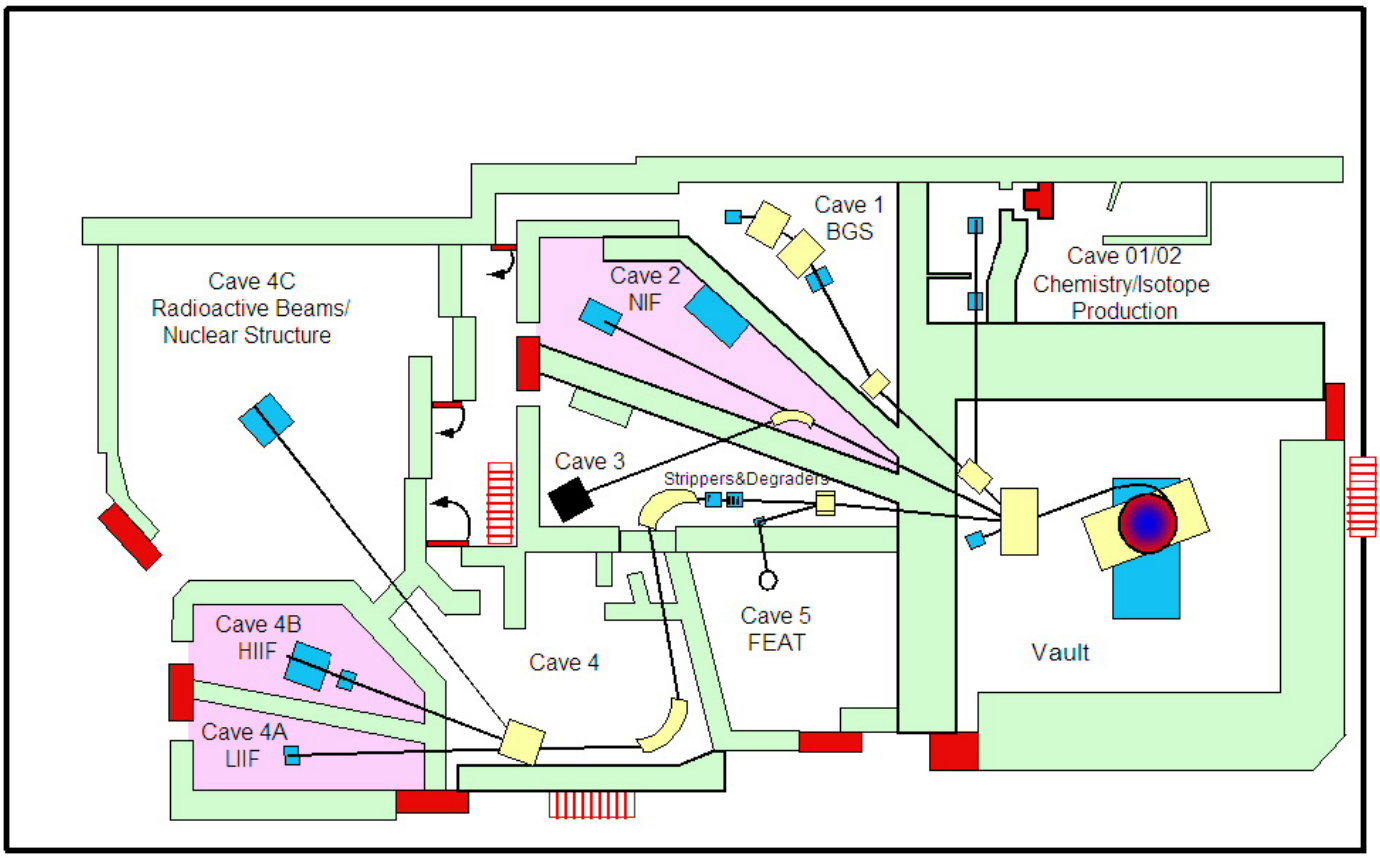

Figure 2.1. Map of 88-Inch Cyclotron Facility showing the location of Cave 4B, where the SEE testing was performed.

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3.0. Radiation Test Conditions

The AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter described in this final report was irradiated using Kr and Xe with a supply voltage of +3.6V and +1.9V and with a 120MHz signal on the clock. Figure 3.1 shows the test board (mother board and daughter card) used for the SEL testing described in this final report (See the test circuit schematic in Appendix B for the additional details of the bias conditions). The test board was mounted on the test stage at Berkeley and provided 3-axis of motion plus rotation. The board had multiple units-under-test that allowed for sequential testing of the units without having to enter the exposure room or breaking vacuum during testing.

The 10MeV/n beam was used to provide sufficient range in silicon while meeting the maximum LET requirements of the program. The other beams available at Berkeley are the 4.5MeV/n beam and the 16MeV/n beam. The 4.5MeV/n beam does not provide sufficient range for destructive SEE testing while the 16MeV/n beam provides a much smaller selection of ions. Figure 3.2 shows the 10MeV/n beam characteristics for krypton and xenon calculated using SRIM. As seen in the figure, the range to the Bragg Peak for xenon (the shortest range particle used) is approximately 60µm while the surface LET is approximately 58MeV-cm2/mg.

Figure 3.3 shows the characteristics for all the beams available at Berkeley. Note that the units were de-encapsulated prior to testing and all exposures took place from the top surface providing a distance to the active layer in Silicon of approximately 5 to 10µm.

As noted above, the devices were irradiated to a minimum fluence of 1E7ion/cm^2. The flux varied during the testing, but was consistently targeted to approximately 1E5ion/cm^2-s to 2E5ion/cm^2-s. The irradiation of the units-under-test continued until either the minimum fluence was reached or a latchup event was observed.

For the elevated temperature required for single event latch-up testing an aluminum plate heater fixed to the back of the board and was used to heat the device-under-test (DUT) with an RTD used to monitor the temperature. The case temperature of the DUT was calibrated prior to the testing to the RTD with a thermocouple, allowing the RTD to provide feedback and maintain a calibrated 85°C case temperature throughout the testing. The data monitored during the test (case temperature, supply voltage and supply current) was routed to the control room (approximately 20-feet away) using shielded coaxial cable.

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Figure 3.1. Single event test board prepared for mounting on the test stage at Berkeley. The board has two units-under-test mounted simultaneously to minimize vacuum breaks during testing. There is also a heater plate mounted to the backside of the board to provide the elevated temperature required for this testing.

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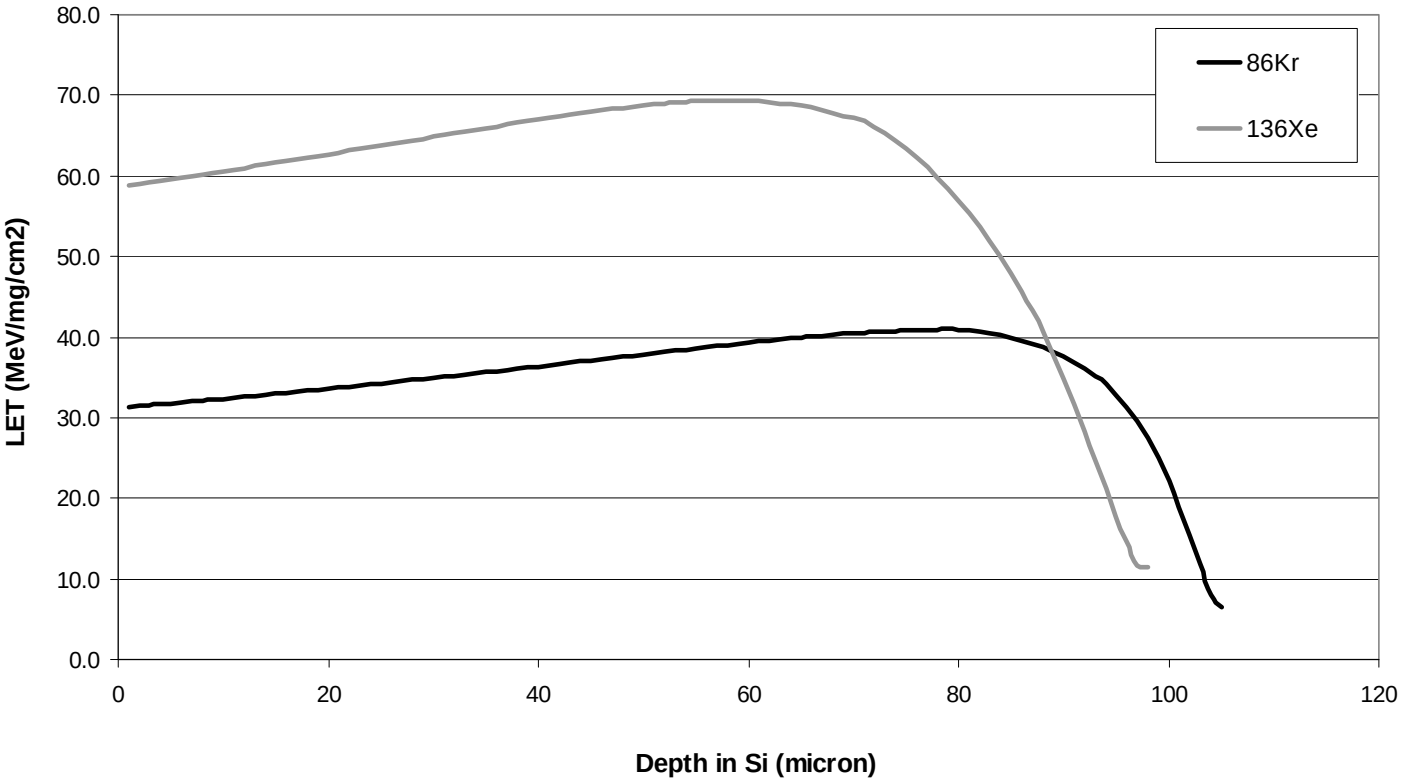

Figure 3.2. Range of the 10MeV/n Kr and Xe beams into silicon. The range to the Bragg Peak for Xe (the shorter of the two particles) is approximately 60µm while the surface LET is approximately 58 MeV-cm^2/mg.

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Ion	Cocktail (MeV/nuc)	Energy (MeV)	Z	A	Chg. State	% Nat. Abund.	LET 0° (MeV/(mg/cm^2))	LET 60° (MeV/(mg/cm^2))	Range (µm)	Method
B	4.5	44.90	5	10	+2	19.9	1.65	3.30	78.5	MIVOC
N	4.5	67.44	7	15	+3	0.37	3.08	6.16	67.8	Gas
Ne	4.5	89.95	10	20	+4	90.48	5.77	11.54	53.1	Gas
Si[1]	4.5	139.61	14	29	+6	4.67	9.28	18.56	52.4	Gas
Ar	4.5	180.00	18	40	+8	99.6	14.32	28.64	48.3	Gas
V	4.5	221.00	23	51	+10	99.75	21.68	43.36	42.5	Probe
Cu	4.5	301.79	29	63	+13	69.17	29.33	58.66	45.6	Probe
Kr	4.5	387.08	36	84	+17	17.3	38.96	77.92	48.0	Gas
Y	4.5	409.58	39	89	+18	100	45.58	91.16	45.8	Probe
Ag	4.5	499.50	47	109	+22	48.161	58.18	116.36	46.3	Probe
Xe	4.5	602.90	54	136	+27	8.9	68.84	137.68	48.3	Gas
Tb	4.5	724.17	65	159	+32	100	77.52	155.04	52.4	Probe
Ta	4.5	805.02	73	181	+36	99.988	87.15	174.30	53.0	Probe
Bi	4.5	904.16	83	209	+41	100	99.74	199.48	52.9	Oven
B	10	108.01	5	11	+3	80.1	0.89	1.78	305.7	MIVOC
O	10	183.47	8	18	+5	0.2	2.19	4.38	226.4	Gas
Ne	10	216.28	10	22	+6	9.25	3.49	6.98	174.6	Gas
Si[1]	10	291.77	14	29	+8	4.67	6.09	12.18	141.7	Gas
Ar	10	400.00	18	40	+11	99.6	9.74	19.48	130.1	Gas
V	10	508.27	23	51	+14	99.75	14.59	29.18	113.4	Probe
Cu	10	659.19	29	65	+18	30.83	21.17	42.34	108.0	Probe
Kr	10	906.45	36	84	+24	57	30.23	60.46	113.1	Gas
Y	10	928.49	39	89	+25	100	34.73	69.46	102.2	Probe
Ag	10	1039.42	47	107	+29	51.839	48.15	96.30	90.0	Probe
Xe	10	1232.55	54	124	+34	0.1	58.78	117.56	90.0	Gas
N	16	233.75	7	14	+5	99.63	1.16	2.32	505.9	Gas
O	16	277.33	8	17	+6	0.04	1.54	3.08	462.4	Gas
Ne	16	321.00	10	20	+7	90.48	2.39	4.78	347.9	Gas
Si[1]	16	452.10	14	29	+10	4.67	4.56	9.12	274.3	Gas
Cl	16	539.51	17	35	+12	75.77	6.61	13.22	233.6	Natural
Ar	16	642.36	18	40	+14	99.600	7.27	14.54	255.6	Gas
V	16	832.84	23	51	+18	99.750	10.90	21.80	225.8	Probe
Cu	16	1007.34	29	63	+22	69.17	16.53	33.06	190.3	Probe
Kr	16	1225.54	36	78	+27	0.35	24.98	49.96	165.4	Gas
Xe	16	1954.71	54	124	+43	0.1	49.29	98.58	147.9	Gas
N	30	425.45	7	15	+7	0.37	0.76	1.52	1370.0	Gas
O	30	490.22	8	17	+8	0.04	0.98	1.96	1220.0	Gas
Ne	30	620.00	10	21	+10	0.27	1.48	2.96	1040.0	Gas
Ar	30	1046.11	18	36	+17	0.337	4.87	9.74	578.1	Gas

[1]By Special request

Figure 3.3. Characteristics of all the beams available at Berkeley. For the testing discussed in this report the 10MeV/n beam was used exclusively.

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4.0. Tested Parameters

During the heavy ion exposure, the supply currents to the unit-under-test was measured and recorded in approximately 1-second increments. A plot of supply current versus time/fluence for each of the heavy ion exposures is included in this final report. Figure 4.1 shows the test board used for the SEL testing described in this final report. The test board was mounted on the test stage at Berkeley and provided 3-axis of motion plus rotation. The board had multiple units-under-test that allowed for sequential testing of the units without vacuum breaks during testing.

In general the following minimum criteria must be met for a device to pass SEL testing: During the heavy ion exposure the DUT's supply current must remain within the unit's specification limit without cycling power. If this condition is not satisfied following the heavy ion testing, then the SEL testing could be logged as a failure. Note that during heavy ion testing a substantial amount of total dose can be absorbed by the units-under-test. If a functional failure occurs during or following the testing, it is important to separate TID failures from destructive single event effects. Also, a single event latch-up may not be a "destructive" event since it is still functional, however a unit which experiences an SEL (i.e., a high sustained supply current requiring a power cycle to recover) is considered to have failed this test even if the units are functional and meet parametric limits following the testing.

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5.0. Single Event Latch-Up Test Results

Using the criteria established for pass/fail of this single event latchup test, the Analog Devices AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter (of the lot date code TBA) FAILED. The units-under-test latched up at an LET of 31 MeV-cm^2/mg (at a case temperature of 110°C). The units-under-test did not latch-up, but did suffer SEFI events at an LETs below 31 MeV-cm^2/mg.

Table 5.1 lists a summary of the single event latch-up data acquired. The table lists the run number, serial number of the part irradiated, test date, case temperature during testing, the ion species, effective LET, effective fluence, angle of exposure, and general comments describing the test results (i.e., SEFIs or latch-up in the analog and/or digital portions of the DUT).

Figures 5.1 through 5.4 show plots of the final current in each of the digital and analog supplies after the ion beam has shut off. The plots are separated in to the lower temperature regime (40°C and below) and the higher temperature regime (85°C and 110°C). Although the higher temperature is worst-case, room temperature is only slightly better in terms of latch-up cross-section.

Figures 5.5 through 5.xx show the total board current (including the unit-under-test digital supply current, analog supply current and board current) and the digital supply current only versus time/fluence during all of the runs. The odd number figures (5.1, 5.3, 5.5, etc) show the total board current while the even numbered figures (5.2, 5.4, 5.6, etc) show only the digital supply current.

As seen in these figures, the units-under-test exhibit SEL in the analog supply within a few seconds of heavy ion exposure for all runs except during exposure with Kr (LET of 30.9MeV-cm^2/mg). The digital supply also shows SEL, however it appears to have a smaller cross-section than the analog supply. The units-under-test also show significant changes in the digital supply current during exposure. It is reasonable to assume that SEFI events are causing the changes (both positive and negative) to the digital supply current.

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Table 5.1. Summary of the SEL test runs and results for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter.

Run #	Test Date	SN	Temp (C)	Ion	LET	Total Fluence	Angle	Comments
72	12/6/11	2a	40	Xe	86.2	2.96E+06	47	Analog and Digital Latch-up
73	12/6/11	2a	40	Xe	58.8	1.01E+07	0	Analog and Digital Latch-up
74	12/6/11	2a	40	Kr	30.9	1.01E+07	0	SEFIs
75	12/6/11	1a	29	Kr	30.9	1.01E+07	0	SEFIs
76	12/6/11	1a	35	Xe	58.8	1.02E+07	0	Analog Latch-up
77	12/6/11	1a	43	Xe	86.2	1.01E+07	47	Analog and Digital Latch-up
78	12/6/11	1a	85	Xe	86.2	1.02E+07	47	Analog and Digital Latch-up
41	2/16/12	4b	110	Kr	45.3	1.02E+07	47	Analog Latch-up
42	2/16/12	4b	110	Ar	14.3	1.01E+07	47	SEFIs
43	2/16/12	4b	110	Cu	31.0	1.01E+07	47	Analog Latch-up
44	2/16/12	5b	110	Cu	31.0	1.01E+07	47	Analog Latch-up
45	2/16/12	5b	110	Ar	14.3	1.02E+07	47	SEFIs
46	2/16/12	5b	110	Kr	45.3	1.01E+07	47	Analog and Digital Latch-up
29	4/6/12	1c	25	Ar	9.7	1.02E+07	0	SEFIs
30	4/6/12	2c	25	Ar	9.7	1.01E+07	0	SEFIs
31	4/6/12	2c	25	Cu	21.2	1.02E+07	0	SEFIs
32	4/6/12	2c	25	Kr	30.9	1.01E+07	0	SEFIs
33	4/6/12	2c	25	Xe	58.8	1.00E+07	0	Analog Latch-up
34	4/6/12	2c	25	Kr	45.3	1.01E+07	47	Analog Latch-up
35	4/6/12	2c	25	Kr	51.3	1.01E+07	53	Analog Latch-up
36	4/6/12	2c	25	Kr	36.8	1.01E+07	33	Analog Latch-up
37	4/6/12	4c	25	Kr	33.5	1.01E+07	23	SEFIs
38	4/6/12	4c	25	Kr	47.0	1.01E+07	49	SEFIs and small latch
39	4/6/12	4c	25	Xe	60.1	1.01E+07	12	Analog Latch-up
40	4/6/12	4c	25	Cu	21.6	1.02E+07	12	SEFIs

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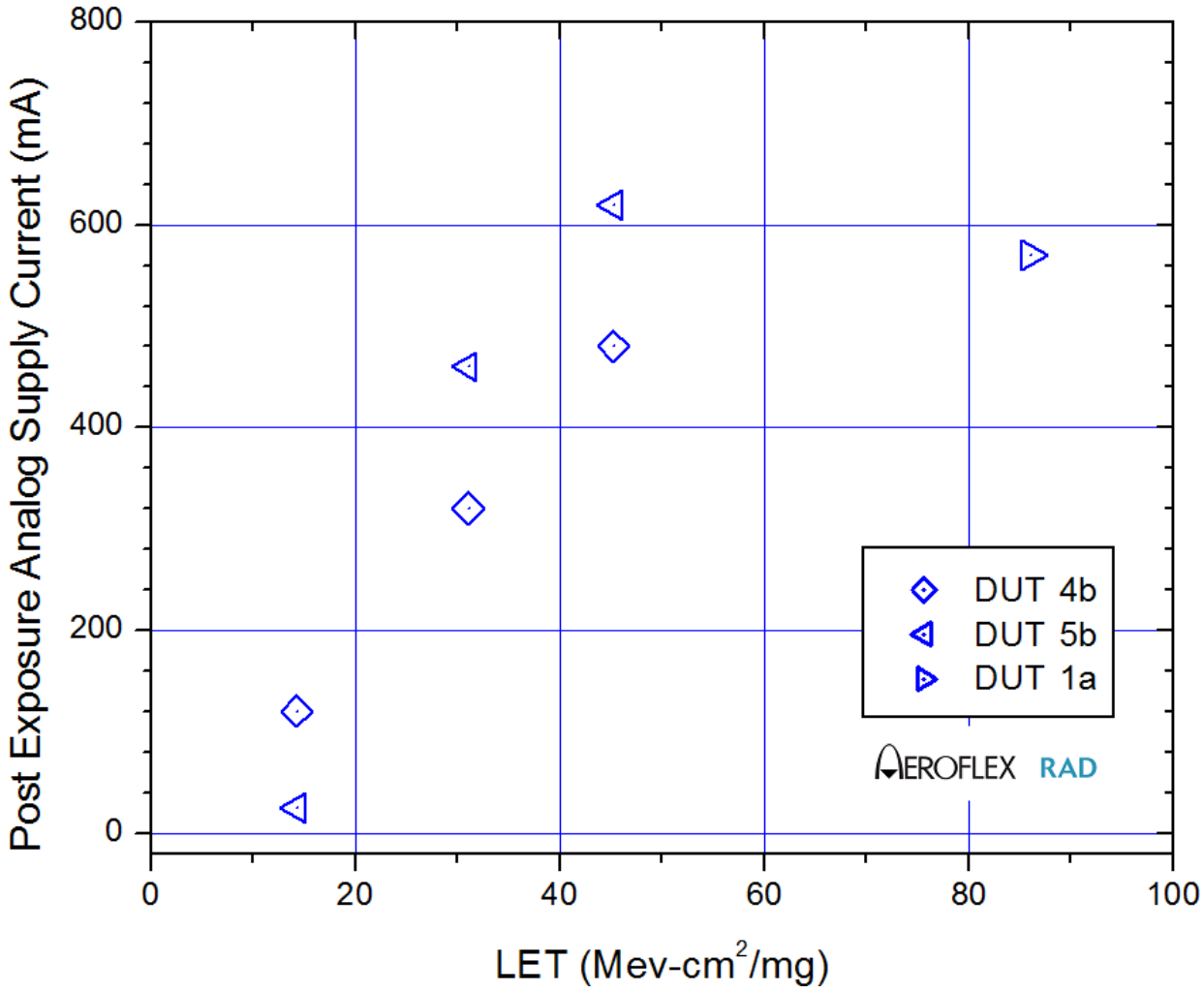

Figure 5-1. High temperature post exposure analog current vs. LET.

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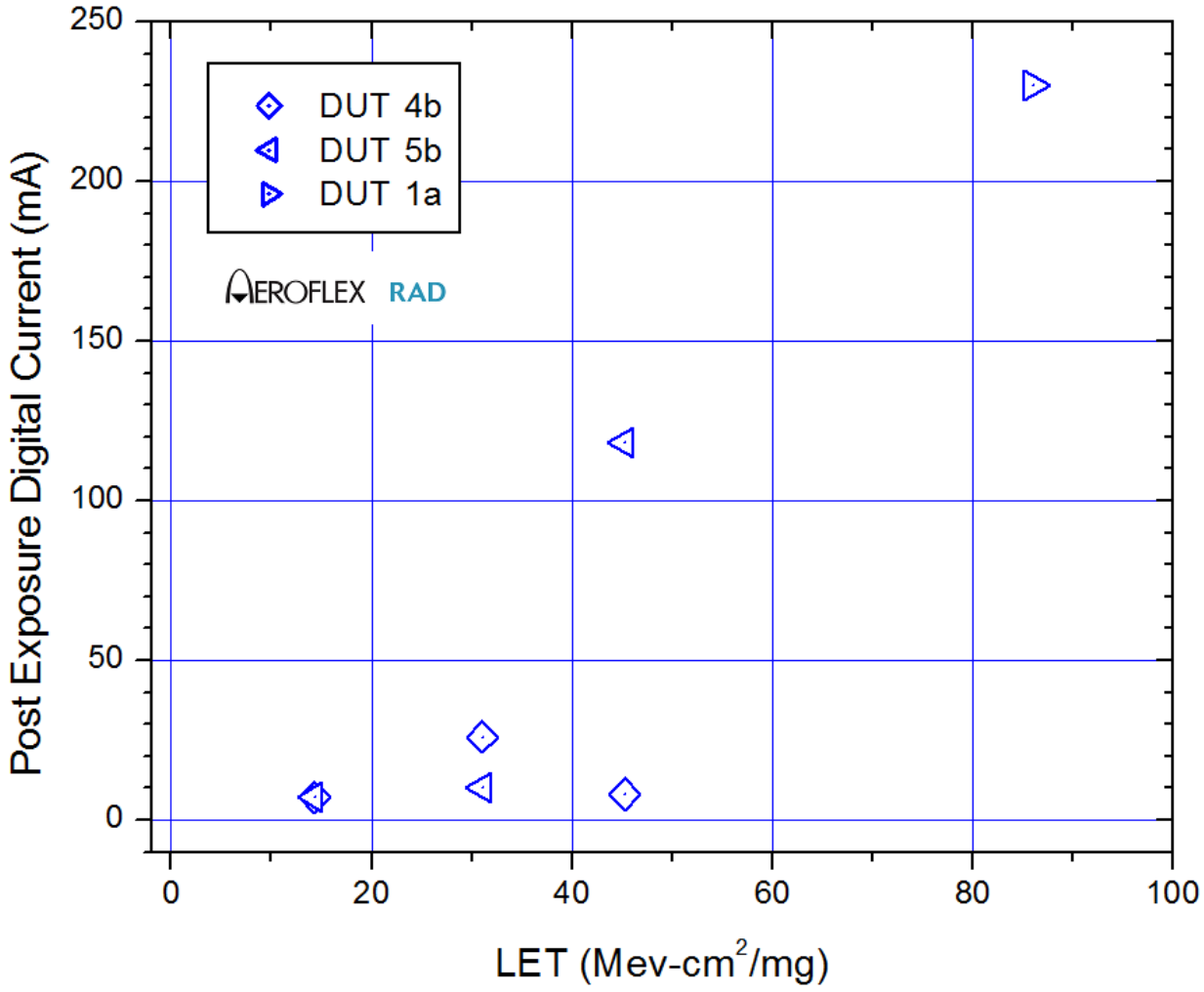

Figure 5-2. High temperature post exposure digital current vs. LET.

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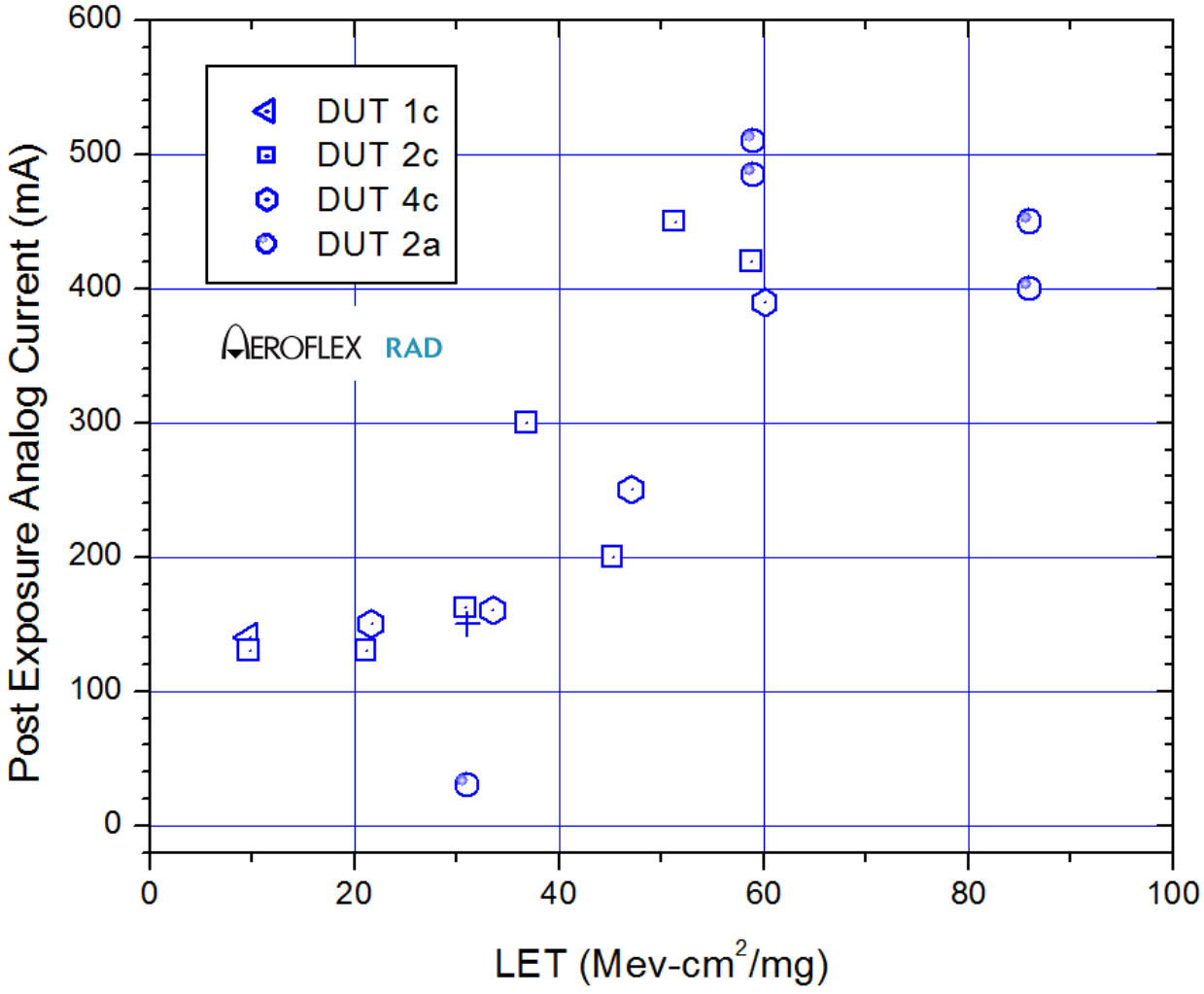

Figure 5-3. Low temperature post exposure analog current vs. LET.

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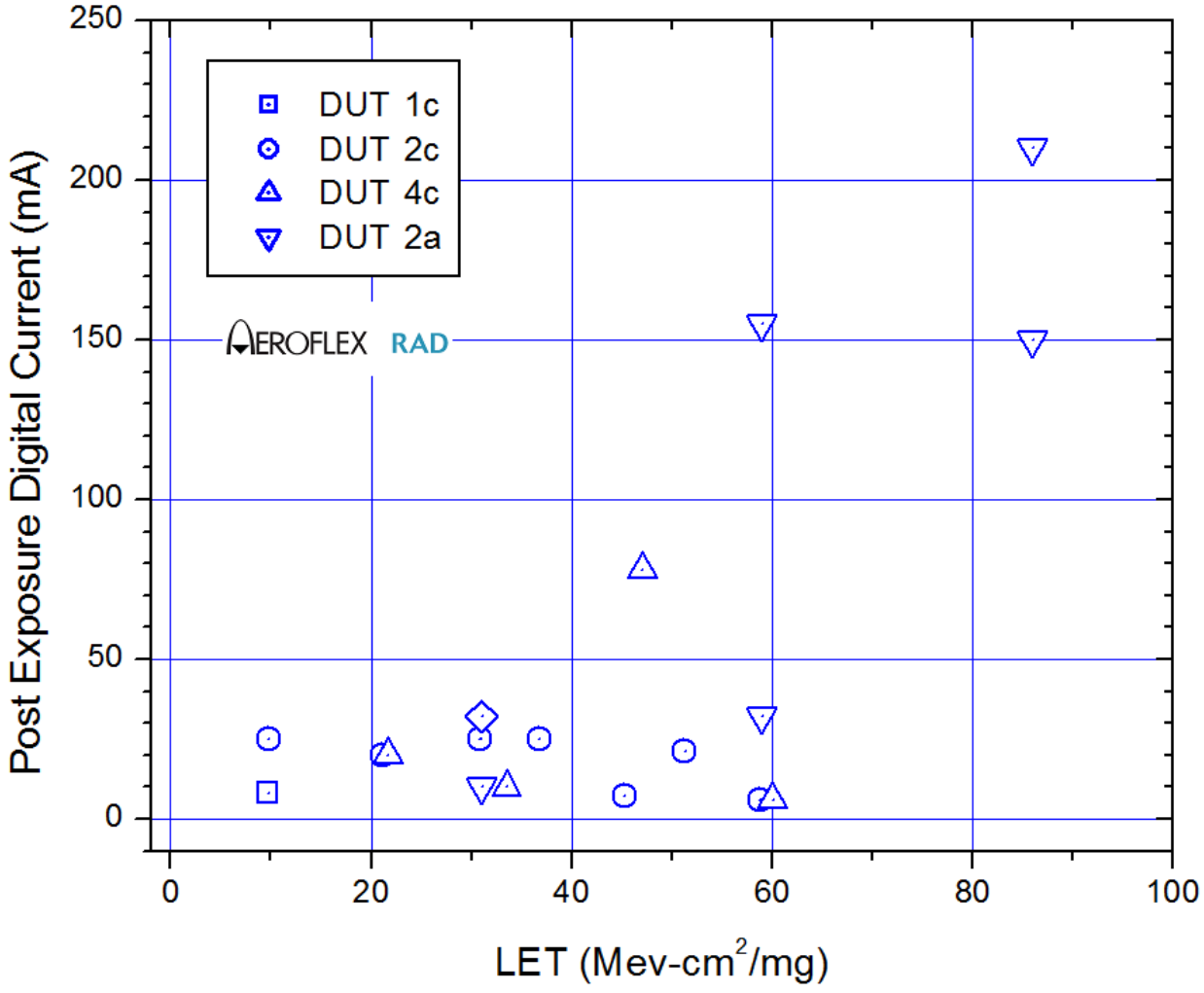

Figure 5-4. Low temperature post exposure digital current vs. LET.

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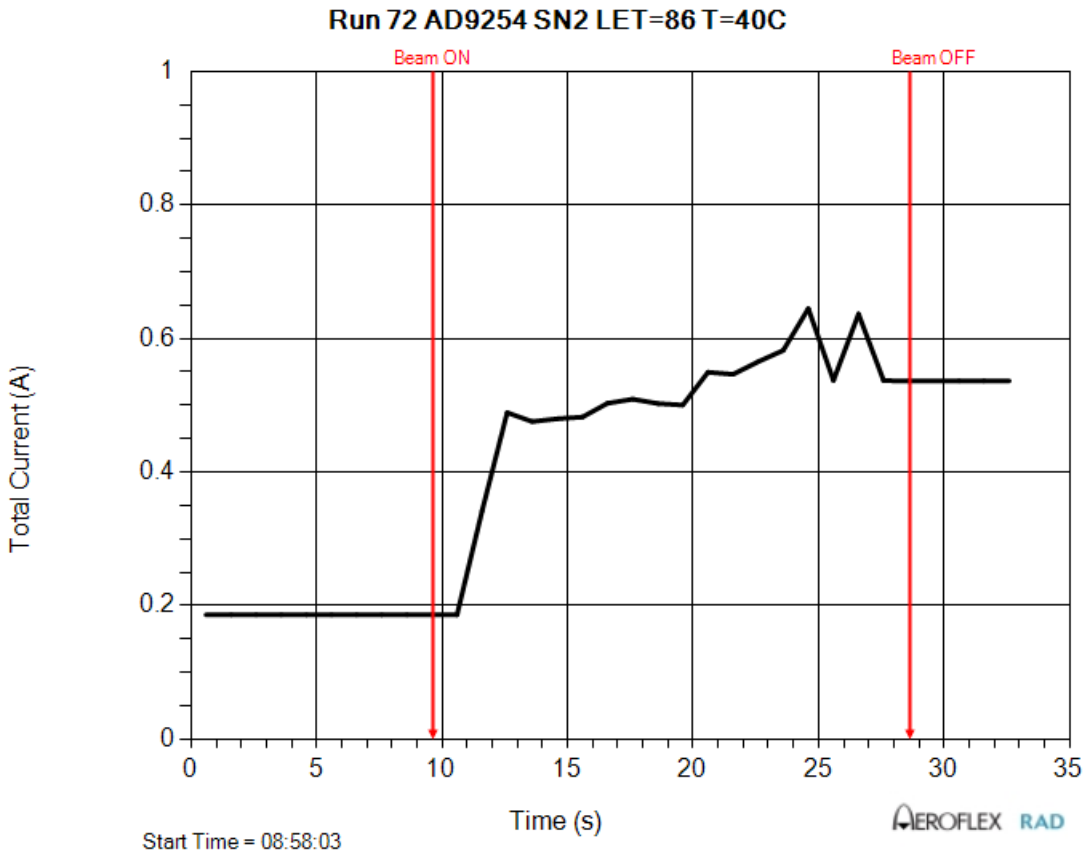

Figure 5.5. Total board current (including the digital supply, analog supply and board current) versus time/fluence during Run 72 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event within a few seconds of heavy ion exposure. See Table 5.1 for the details about the run.

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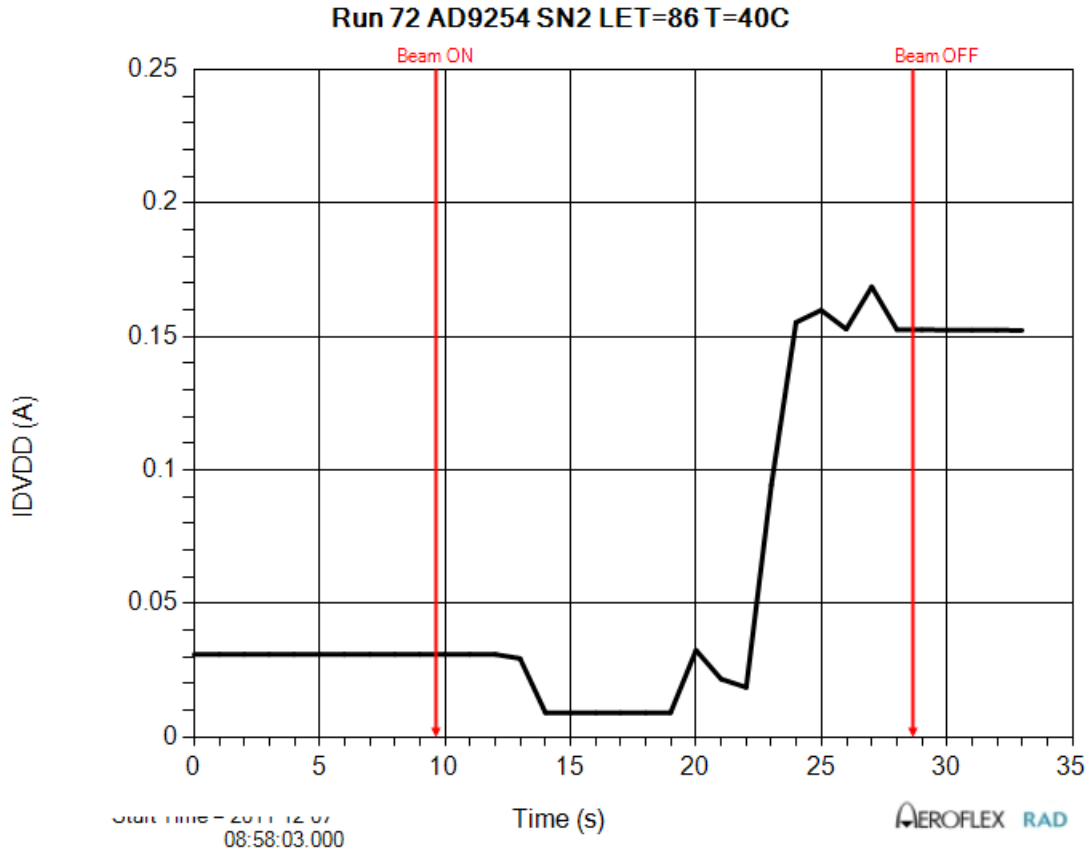

Figure 5.6. Unit-under-test digital supply current versus time/fluence during Run 72 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event in the digital supply after approximately 12-seconds of heavy ion exposure. See Table 5.1 for the details about the run.

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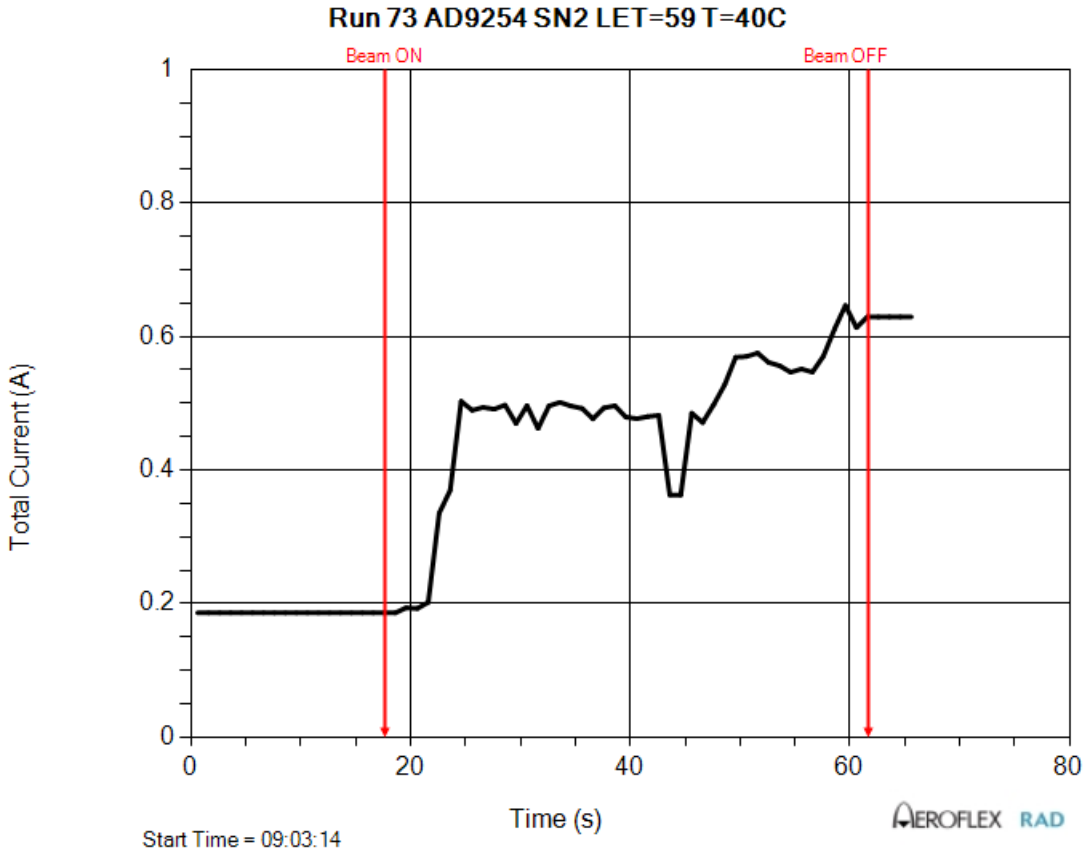

Figure 5.7. Total board current (including the digital supply, analog supply and board current) versus time/fluence during Run 73 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event within a few seconds of heavy ion exposure. See Table 5.1 for the details about the run.

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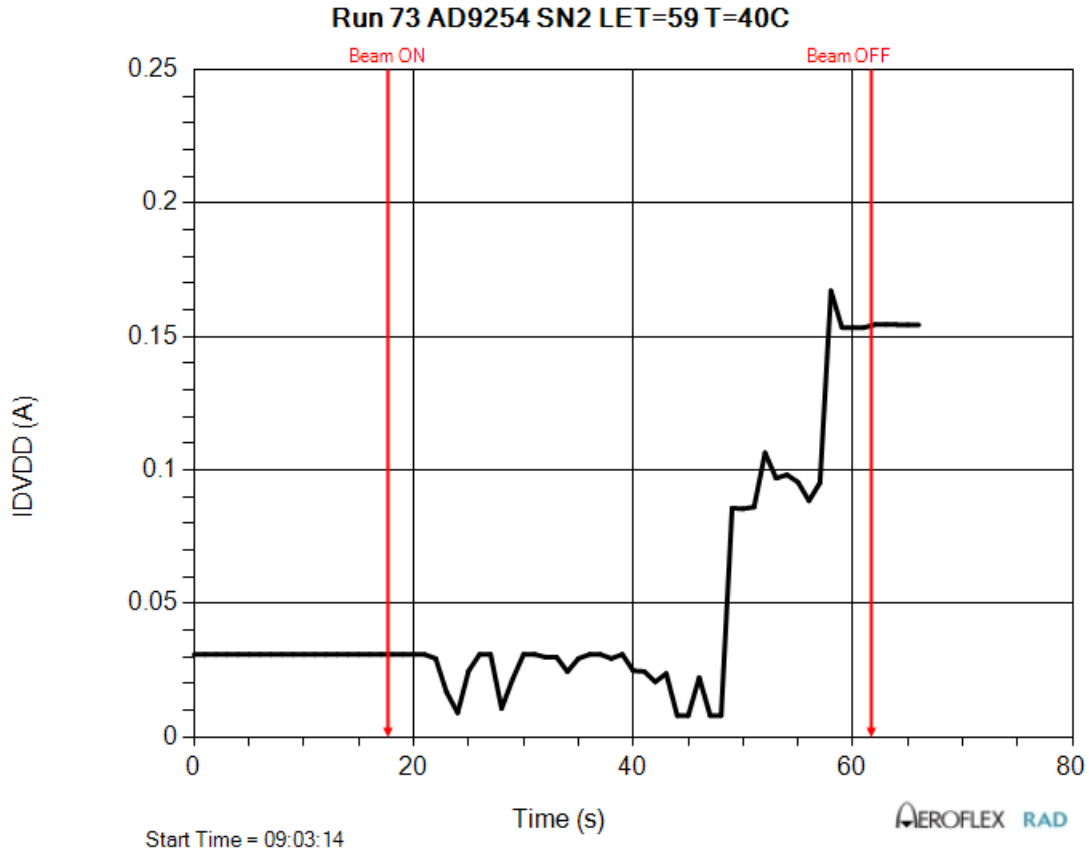

Figure 5.8. Unit-under-test digital supply current versus time/fluence during Run 73 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event in the digital supply after approximately 25-seconds of heavy ion exposure. See Table 5.1 for the details about the run.

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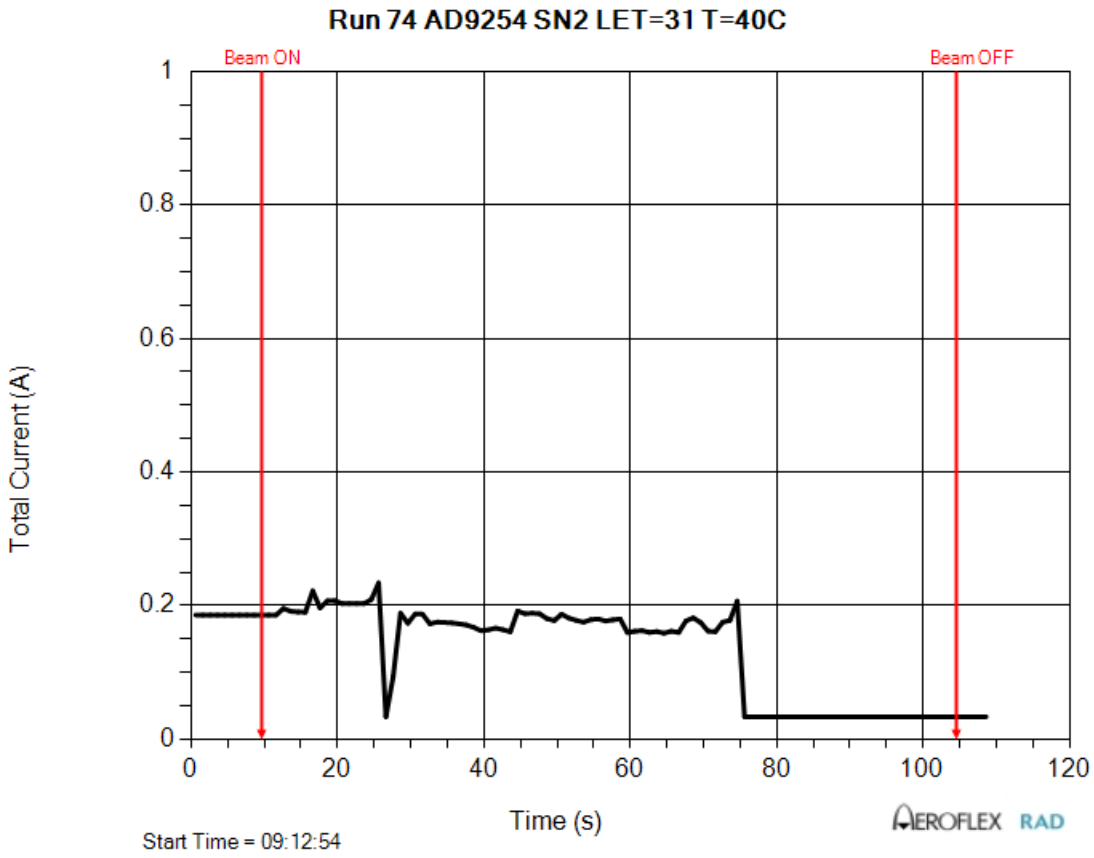

Figure 5.9. Total board current (including the digital supply, analog supply and board current) versus time/fluence during Run 74 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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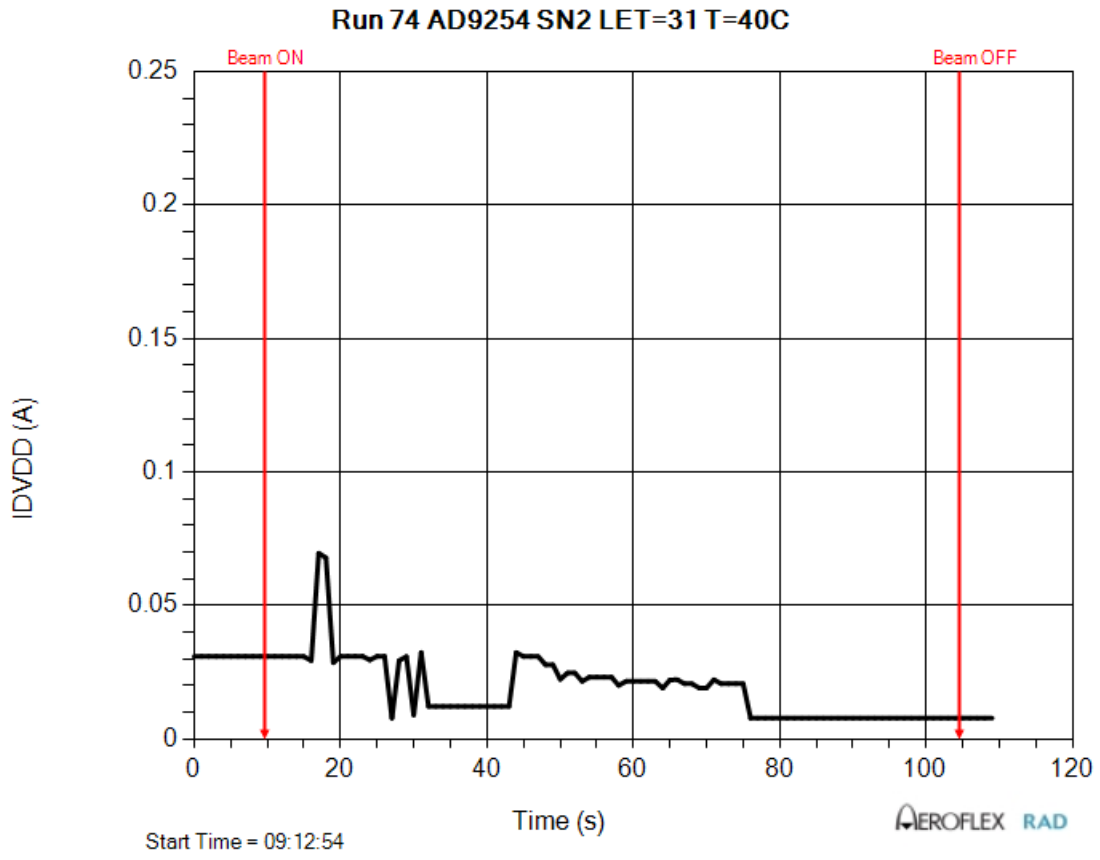

Figure 5.10. Unit-under-test digital supply current versus time/fluence during Run 74 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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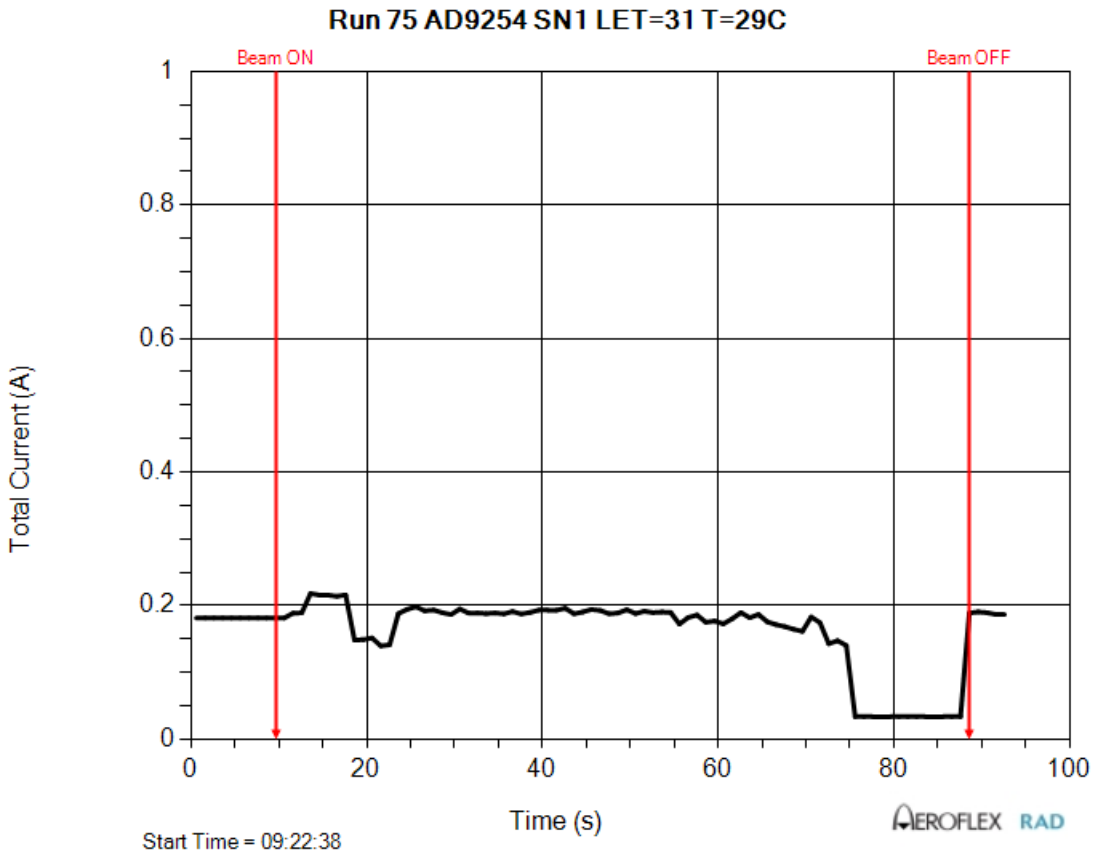

Figure 5.11. Total board current (including the digital supply, analog supply and board current) versus time/fluence during Run 75 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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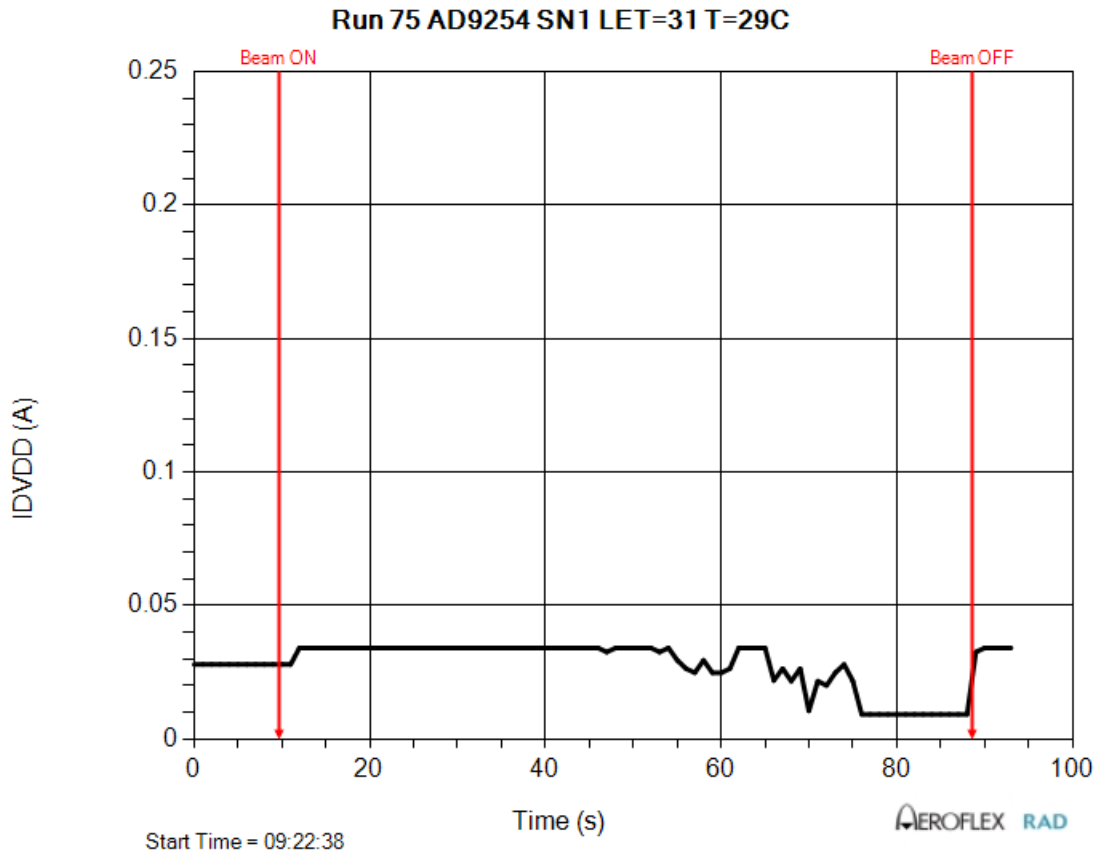

Figure 5.12. Unit-under-test digital supply current versus time/fluence during Run 75 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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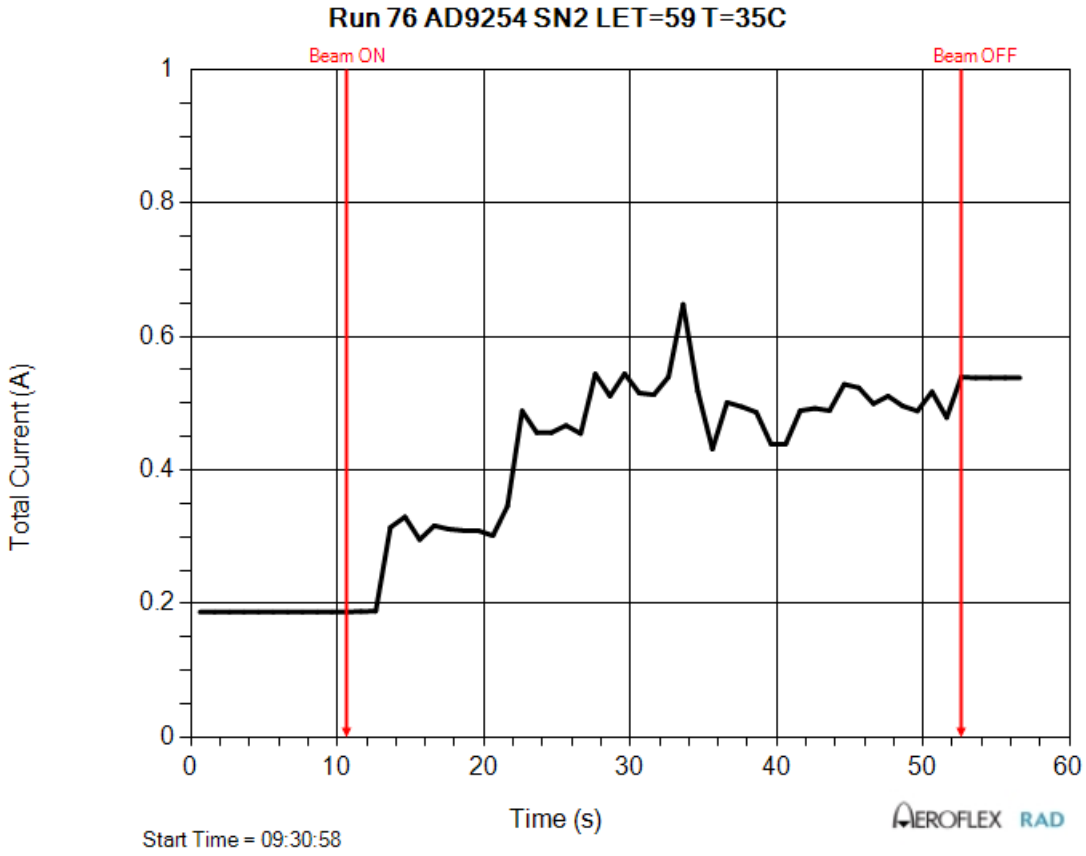

Figure 5.13. Total board current (including the digital supply, analog supply and board current) versus time/fluence during Run 76 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event within a few seconds of heavy ion exposure. See Table 5.1 for the details about the run.

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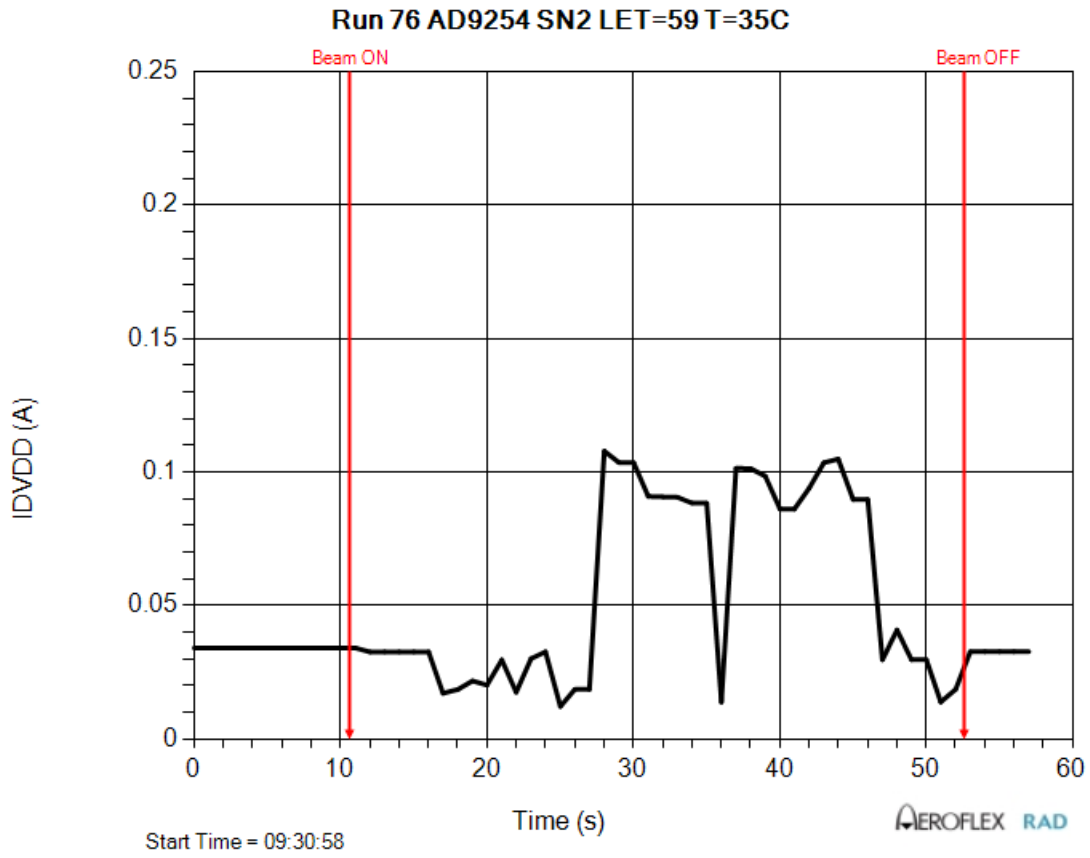

Figure 5.14. Unit-under-test digital supply current versus time/fluence during Run 76 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the digital supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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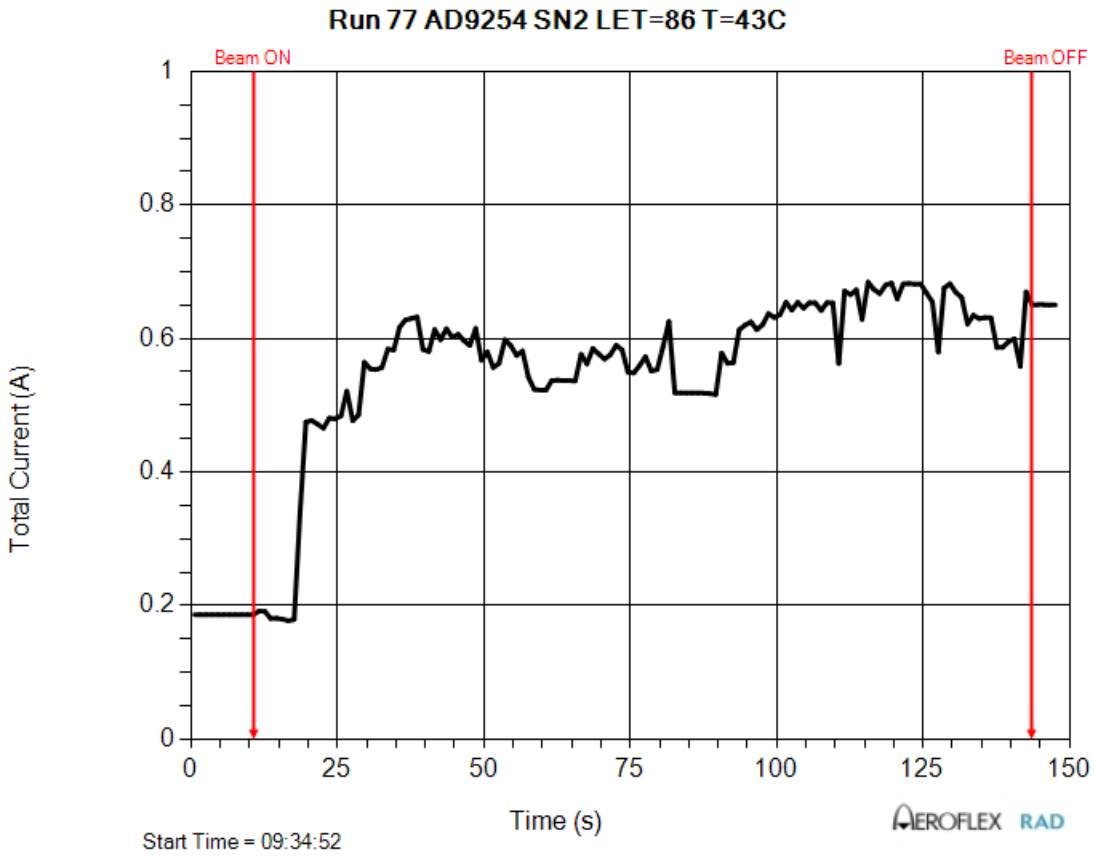

Figure 5.15. Total board current (including the digital supply, analog supply and board current) versus time/fluence during Run 76 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event within a few seconds of heavy ion exposure. See Table 5.1 for the details about the run.

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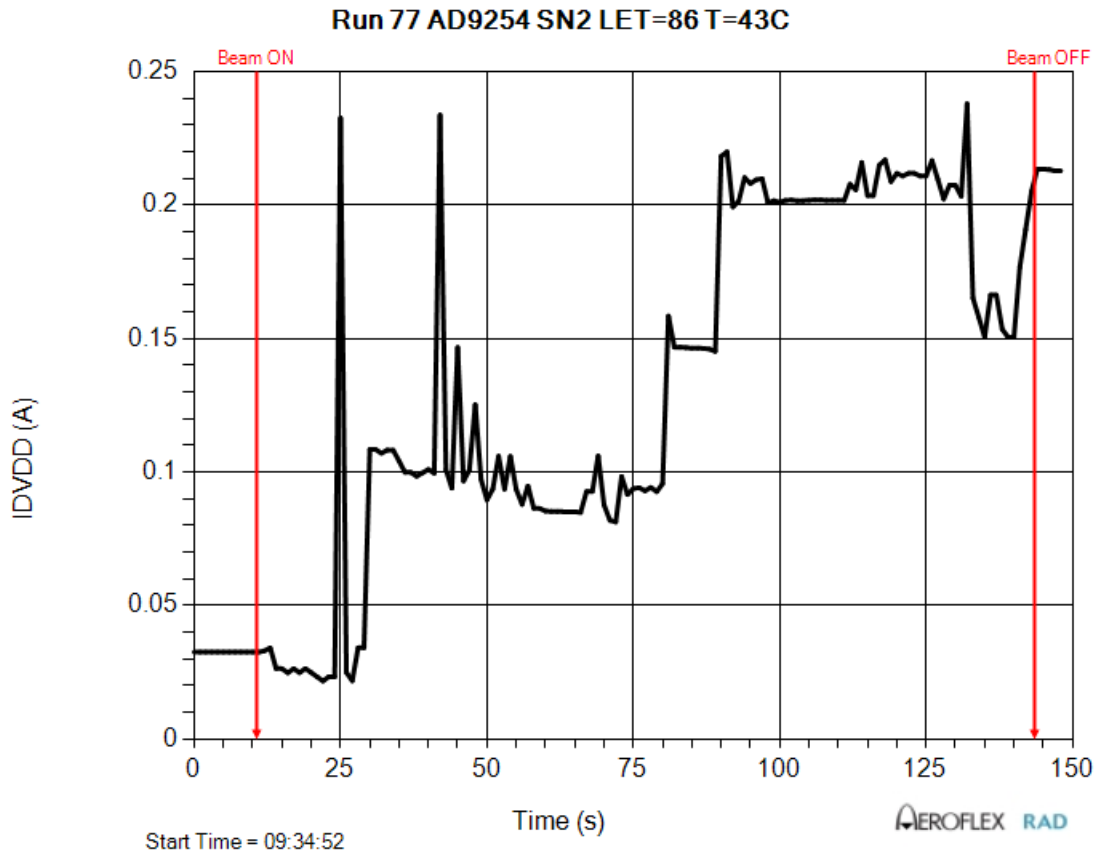

Figure 5.16. Unit-under-test digital supply current versus time/fluence during Run 77 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event in the digital supply after approximately 30-seconds of heavy ion exposure. The change in current during the run, prior to the SEL event is indicative of SEFIs events. See Table 5.1 for the details about the run.

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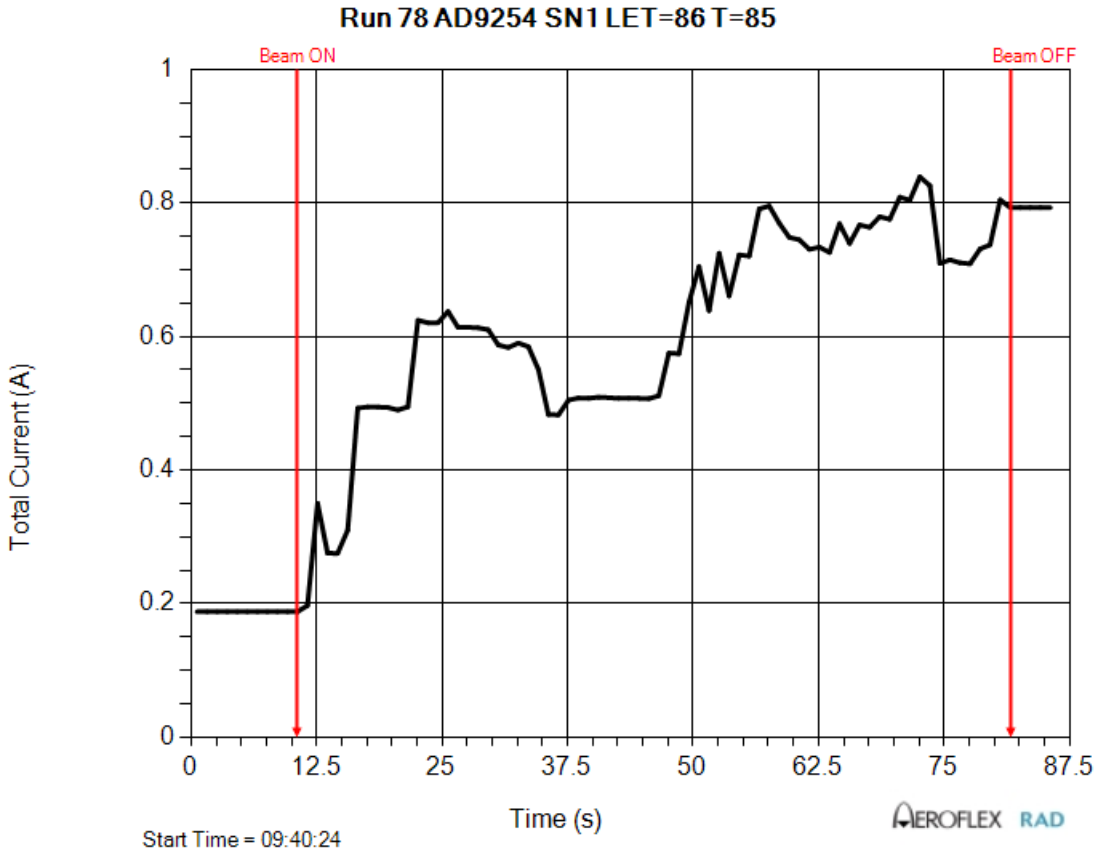

Figure 5.17. Total board current (including the digital supply, analog supply and board current) versus time/fluence during Run 78 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event within a few seconds of heavy ion exposure. See Table 5.1 for the details about the run.

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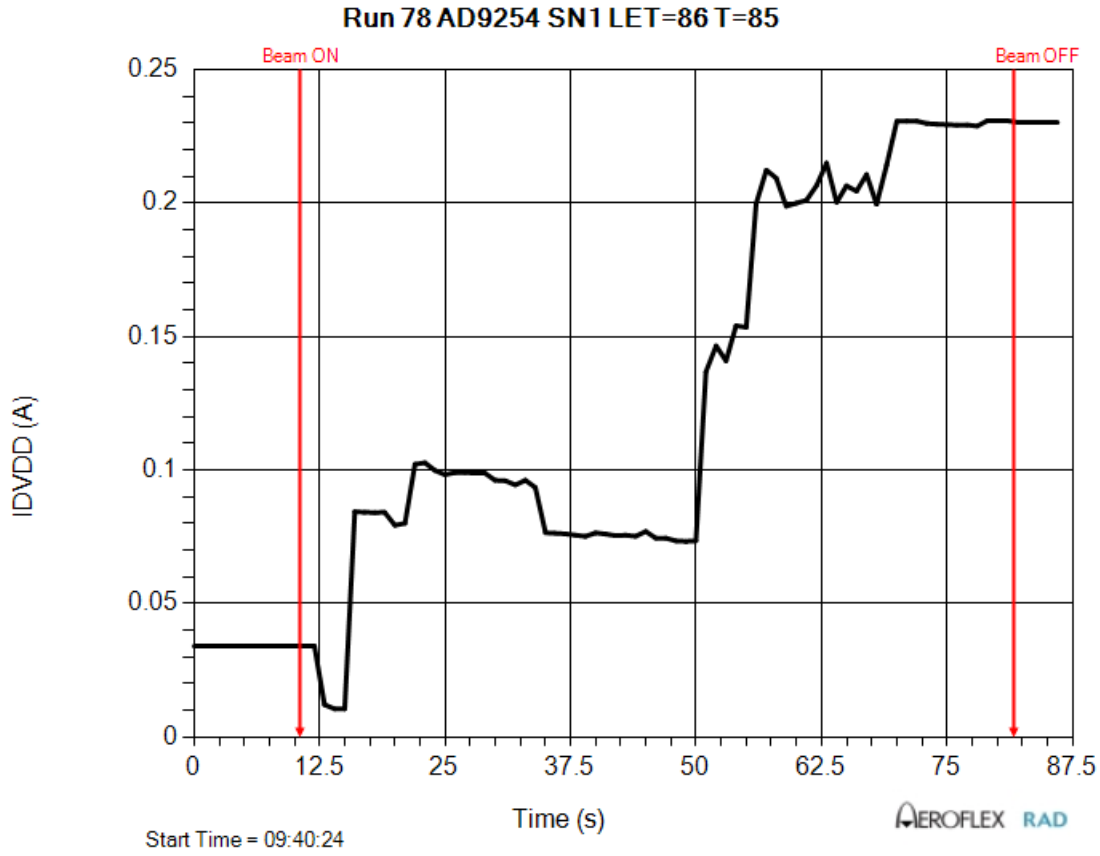

Figure 5.18. Unit-under-test digital supply current versus time/fluence during Run 78 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event in the digital supply after a few seconds of heavy ion exposure. The change in current during the run, prior to the SEL event is indicative of SEFIs events. See Table 5.1 for the details about the run.

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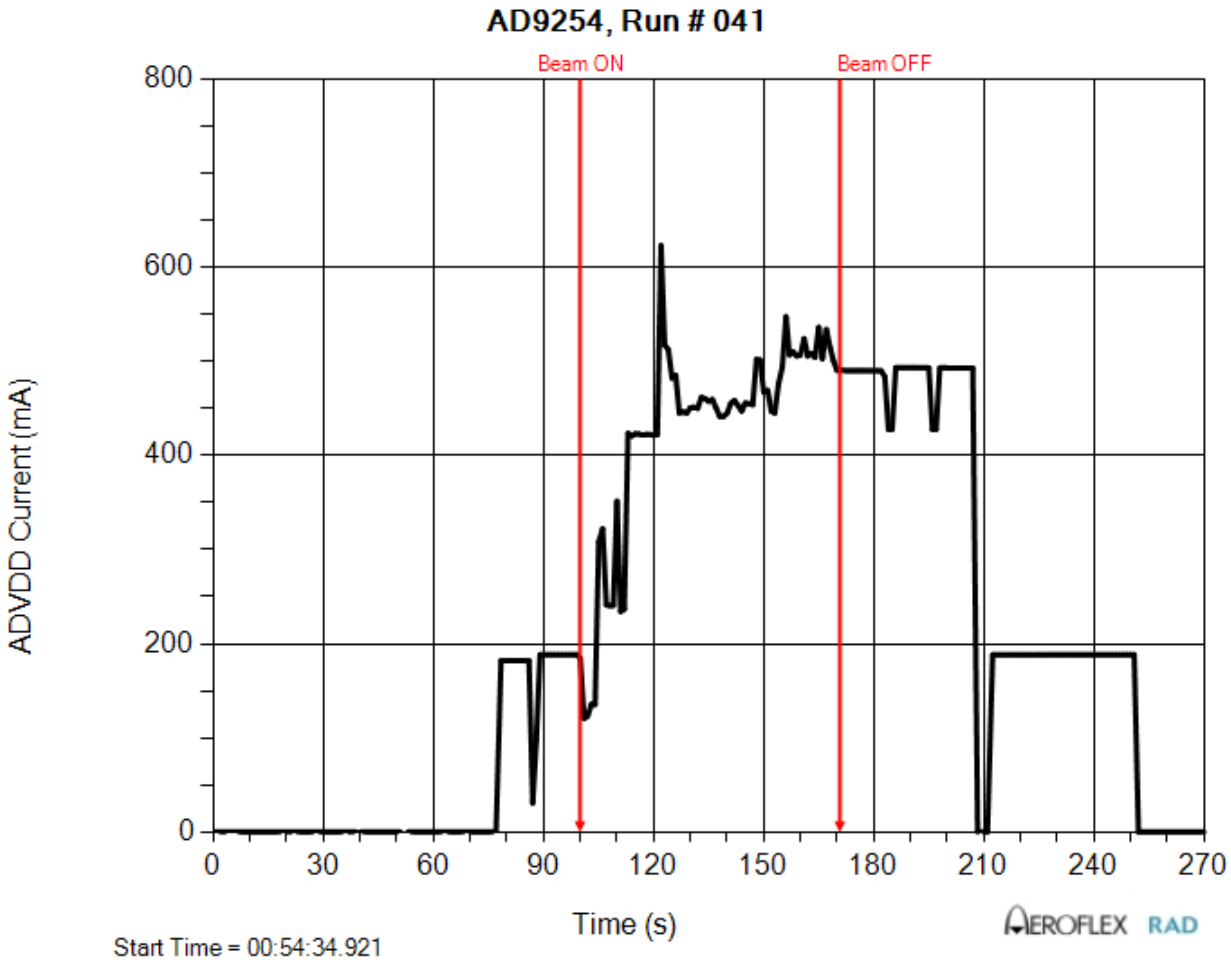

Figure 5.19. Unit-under-test analog supply current versus time/fluence during Run 41 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event in the analog supply after 10-15 seconds of heavy ion exposure. The change in current during the run, prior to the SEL event is indicative of SEFIs events. See Table 5.1 for the details about the run.

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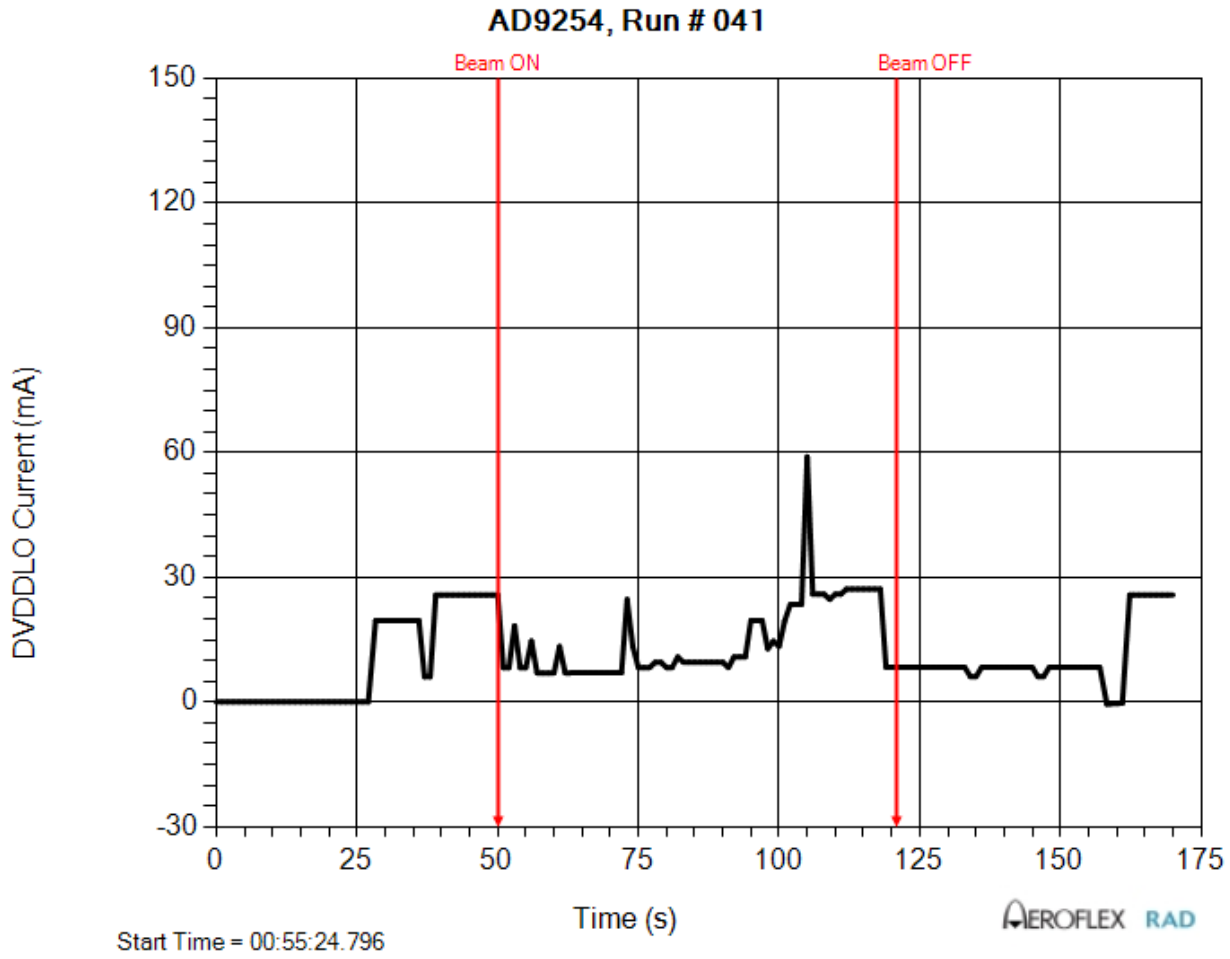

Figure 5.20. Unit-under-test digital supply current versus time/fluence during Run 41 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the digital supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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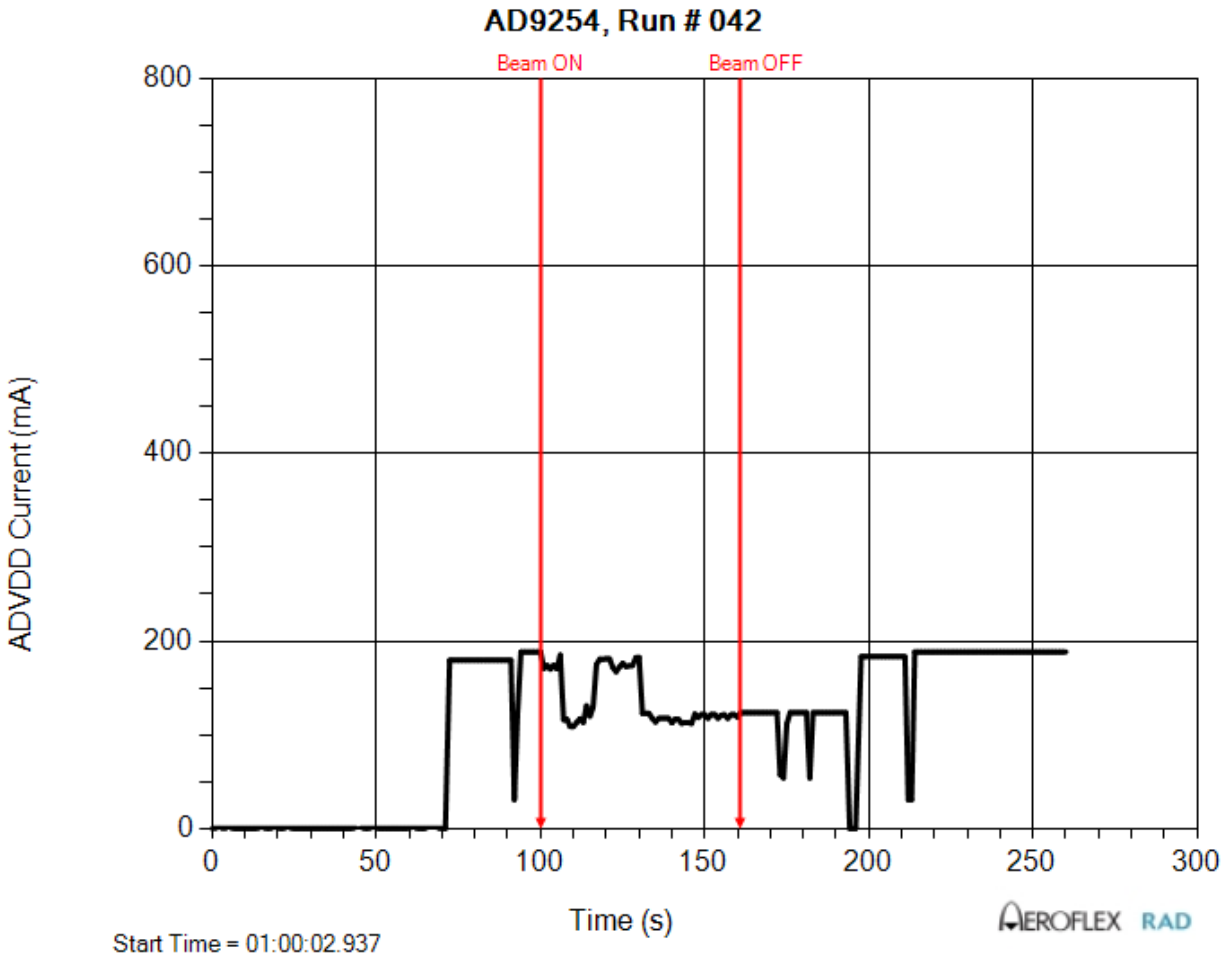

Figure 5.21. Unit-under-test analog supply current versus time/fluence during Run 42 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the analog supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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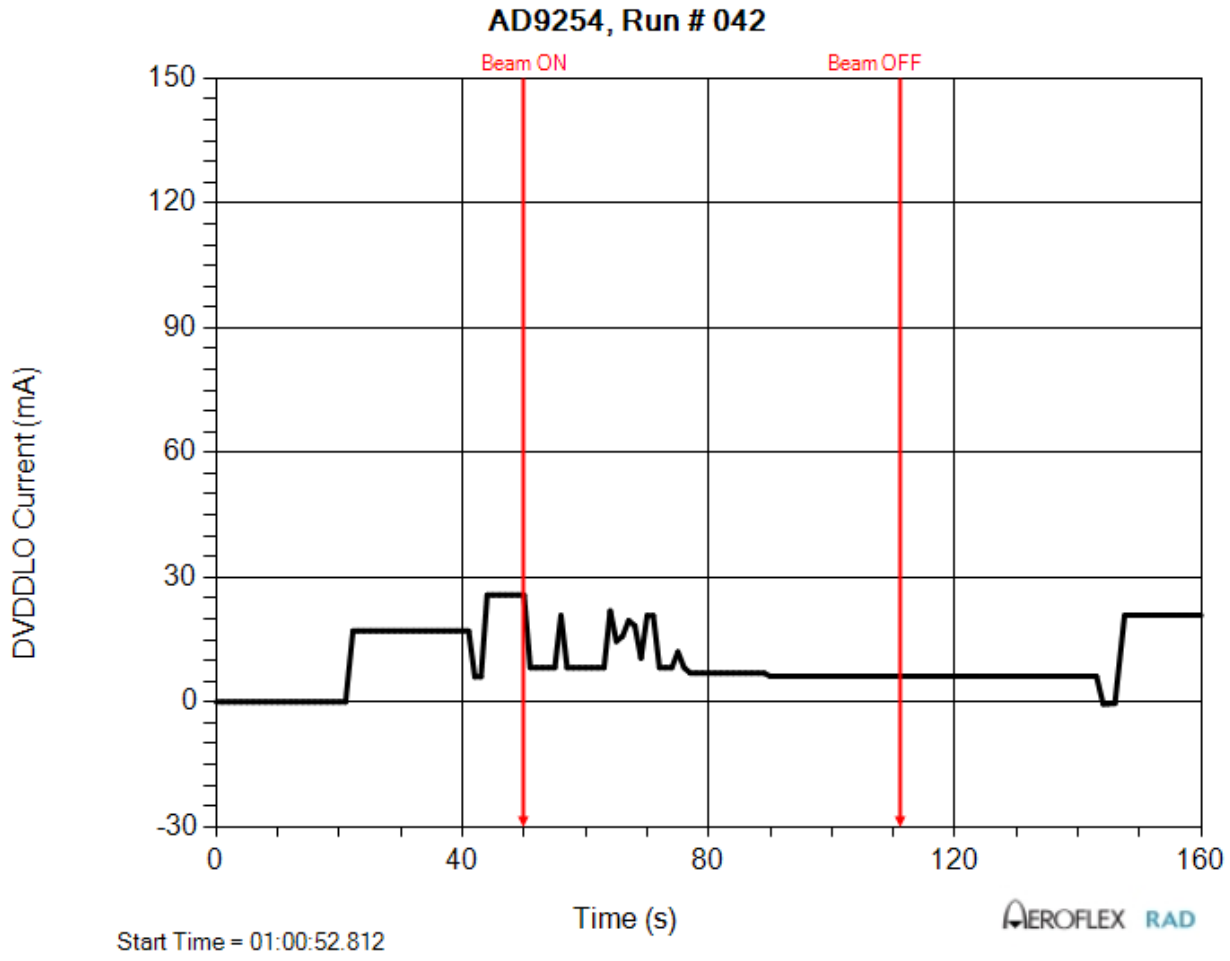

Figure 5.22. Unit-under-test digital supply current versus time/fluence during Run 42 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the digital supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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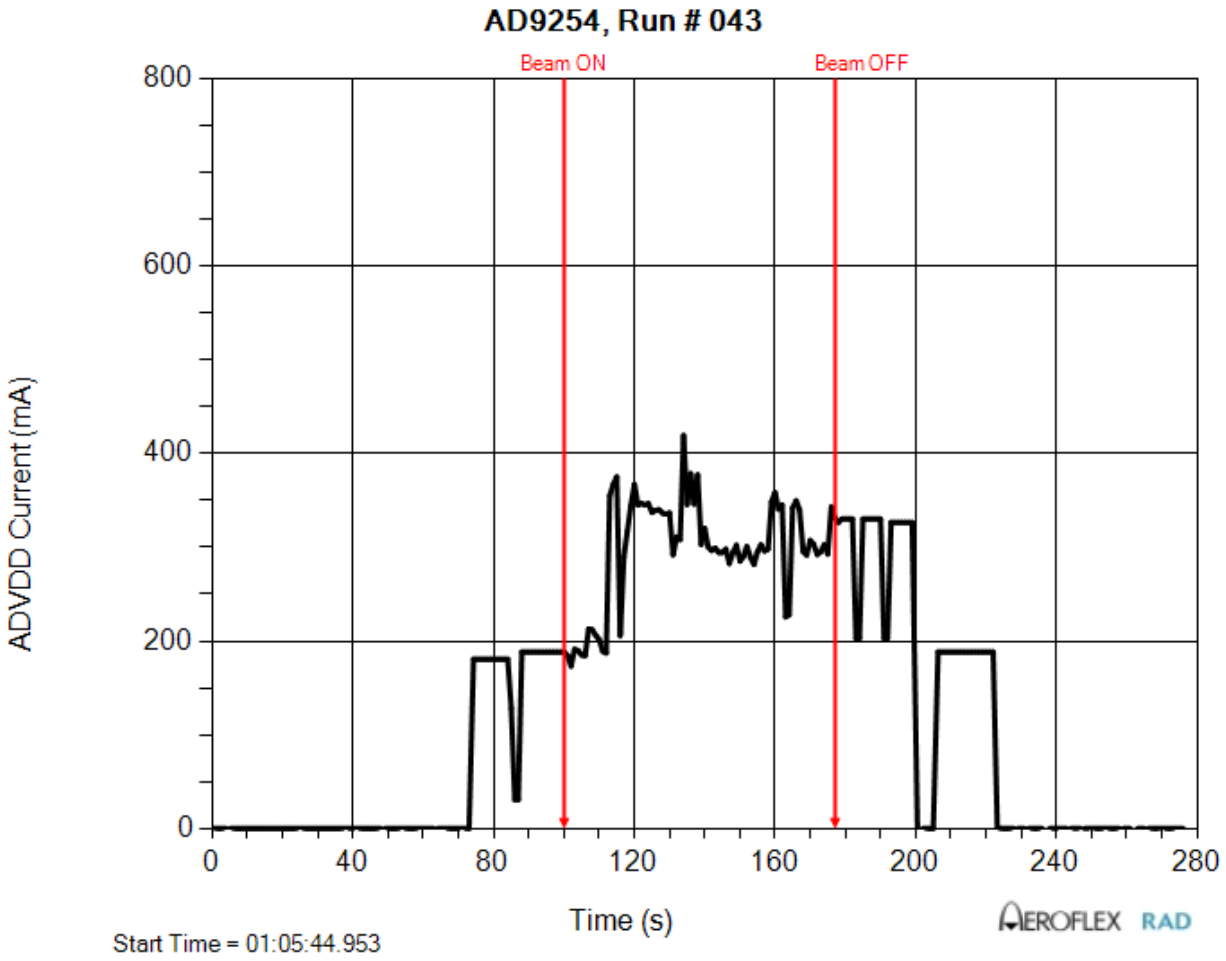

Figure 5.23. Unit-under-test analog supply current versus time/fluence during Run 43 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event in the analog supply after 15-20 seconds of heavy ion exposure. The change in current during the run, prior to the SEL event is indicative of SEFIs events. See Table 5.1 for the details about the run.

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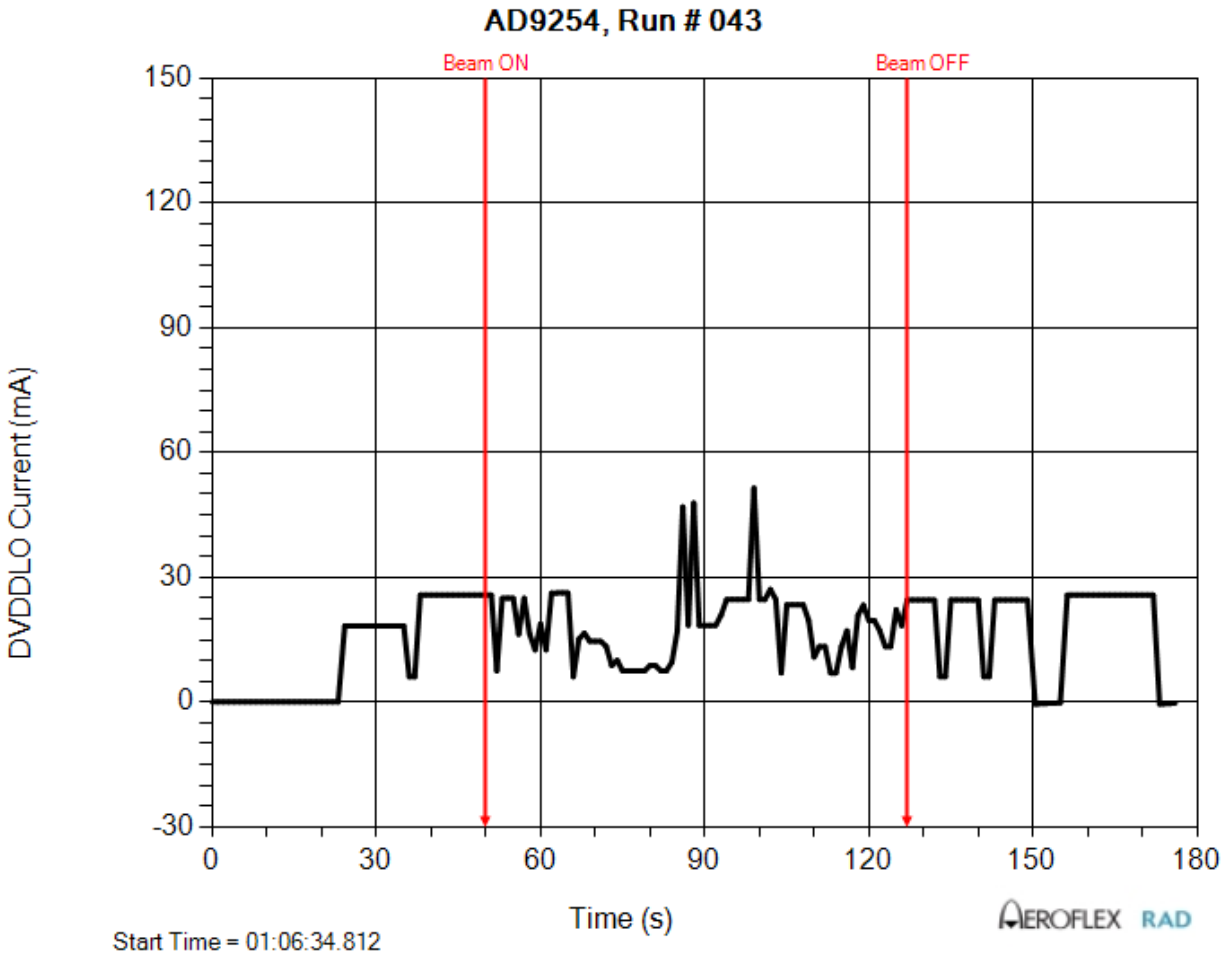

Figure 5.24. Unit-under-test digital supply current versus time/fluence during Run 43 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the digital supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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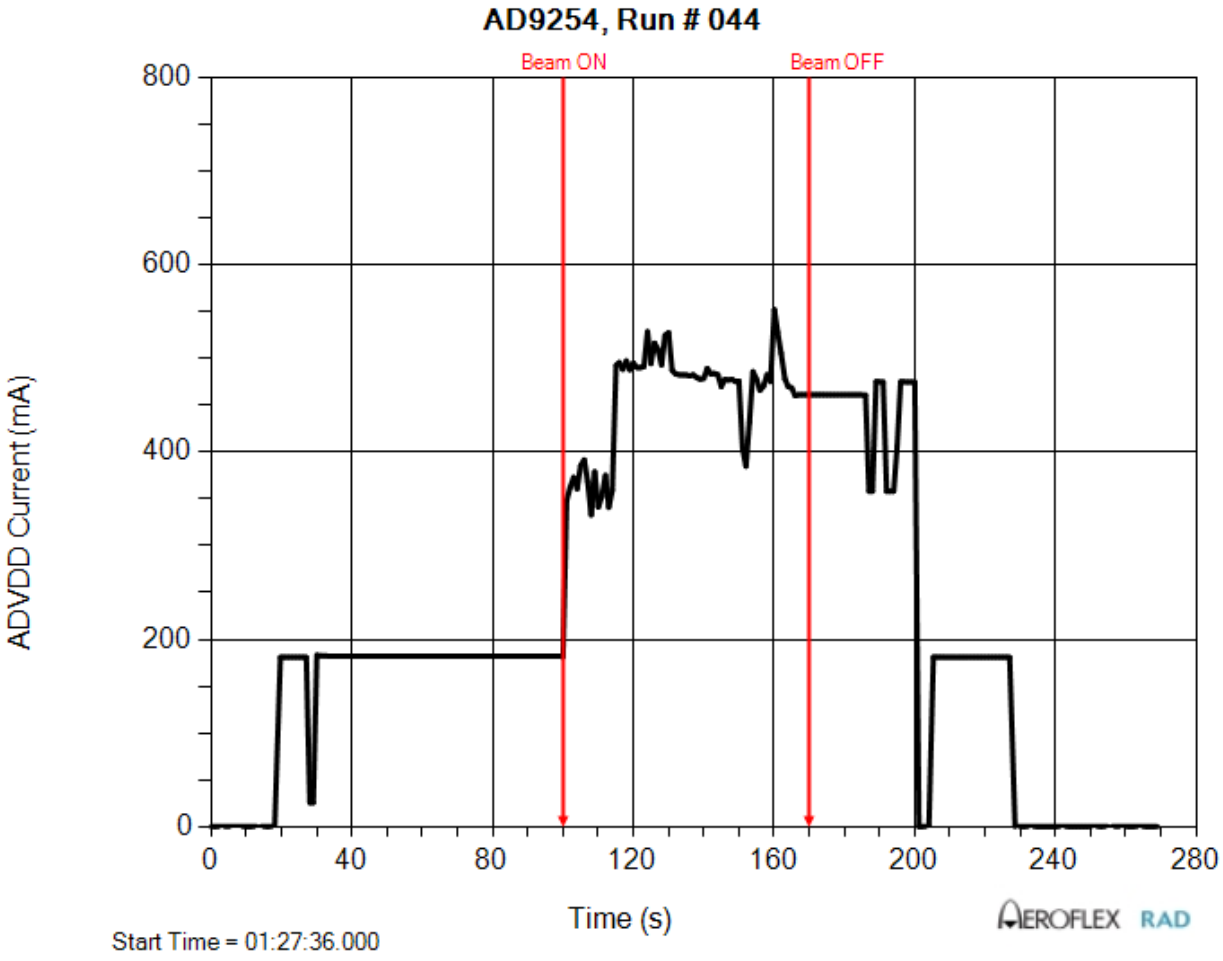

Figure 5.25. Unit-under-test analog supply current versus time/fluence during Run 44 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event in the analog supply after a few seconds of heavy ion exposure. The change in current during the run, prior to the SEL event is indicative of SEFIs events. See Table 5.1 for the details about the run.

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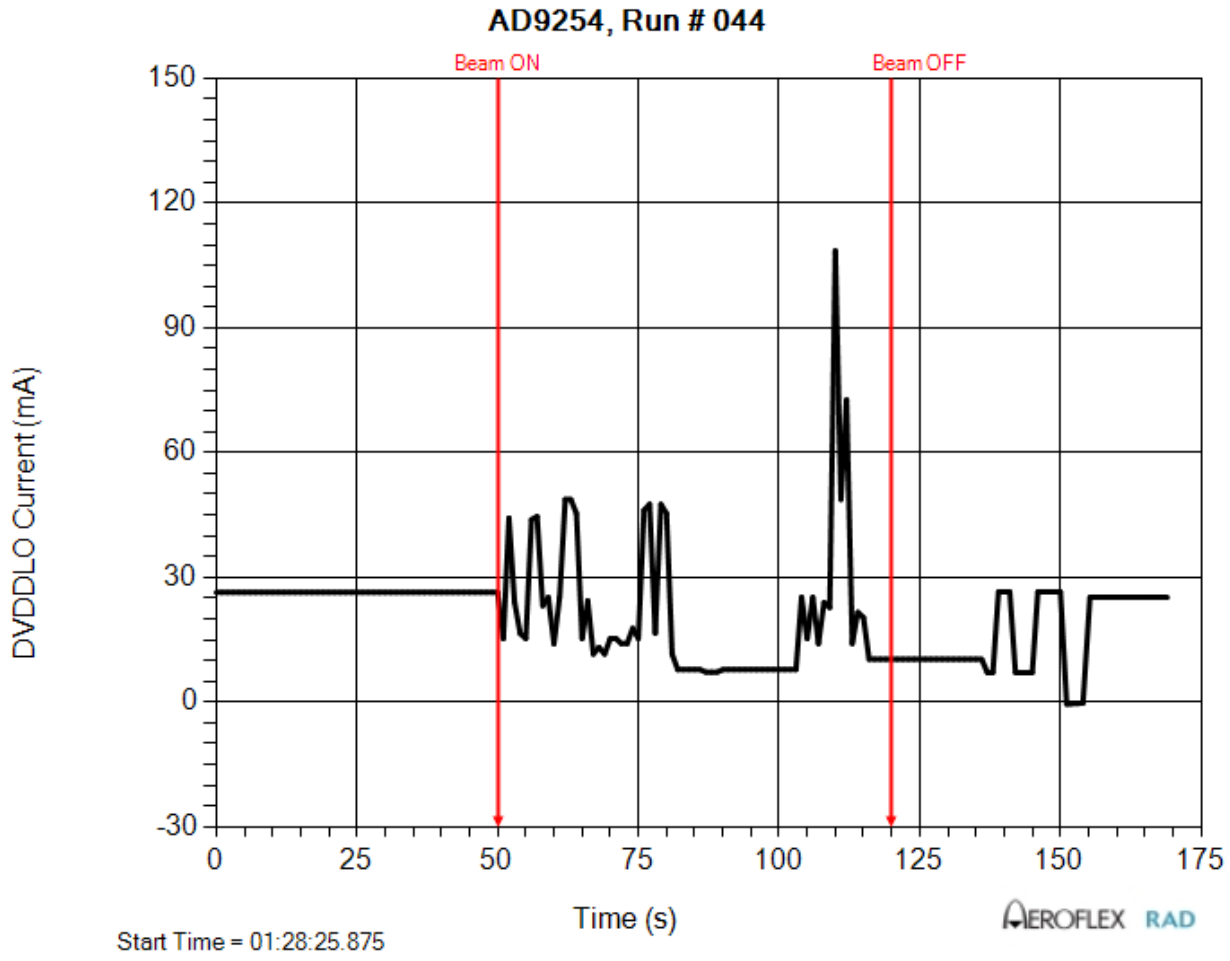

Figure 5.16. Unit-under-test digital supply current versus time/fluence during Run 44 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the digital supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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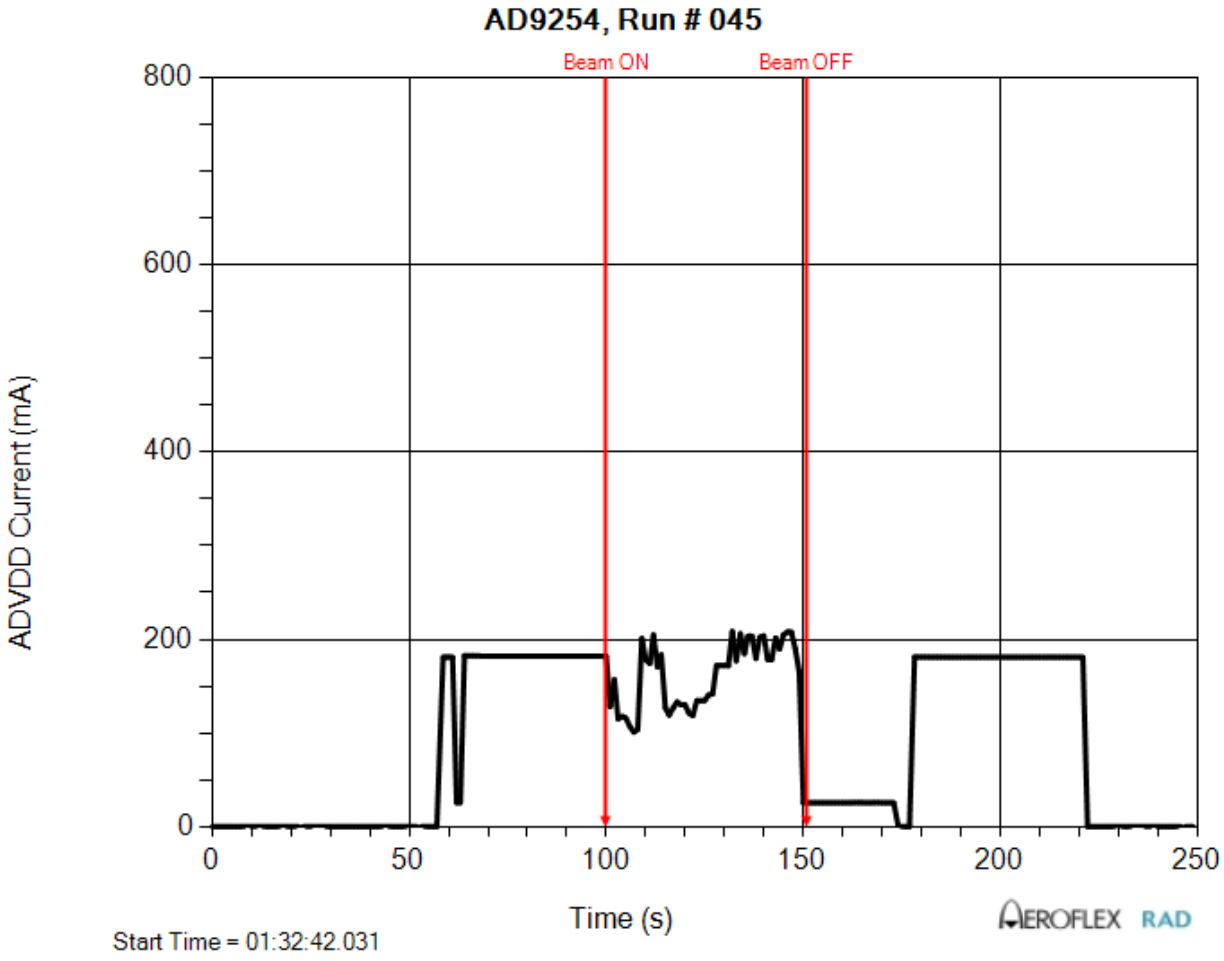

Figure 5.27. Unit-under-test analog supply current versus time/fluence during Run 45 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the analog supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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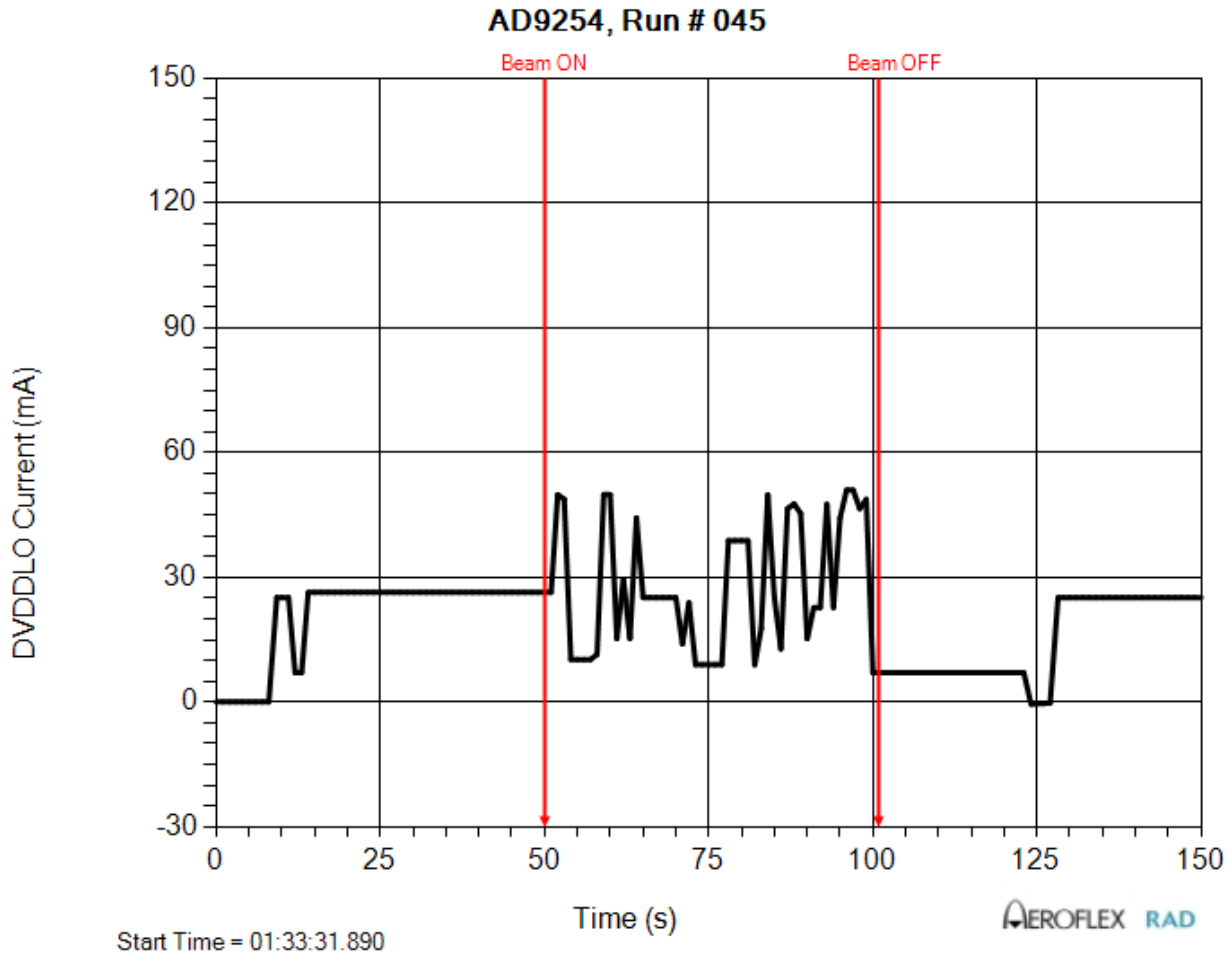

Figure 5.28. Unit-under-test digital supply current versus time/fluence during Run 45 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the digital supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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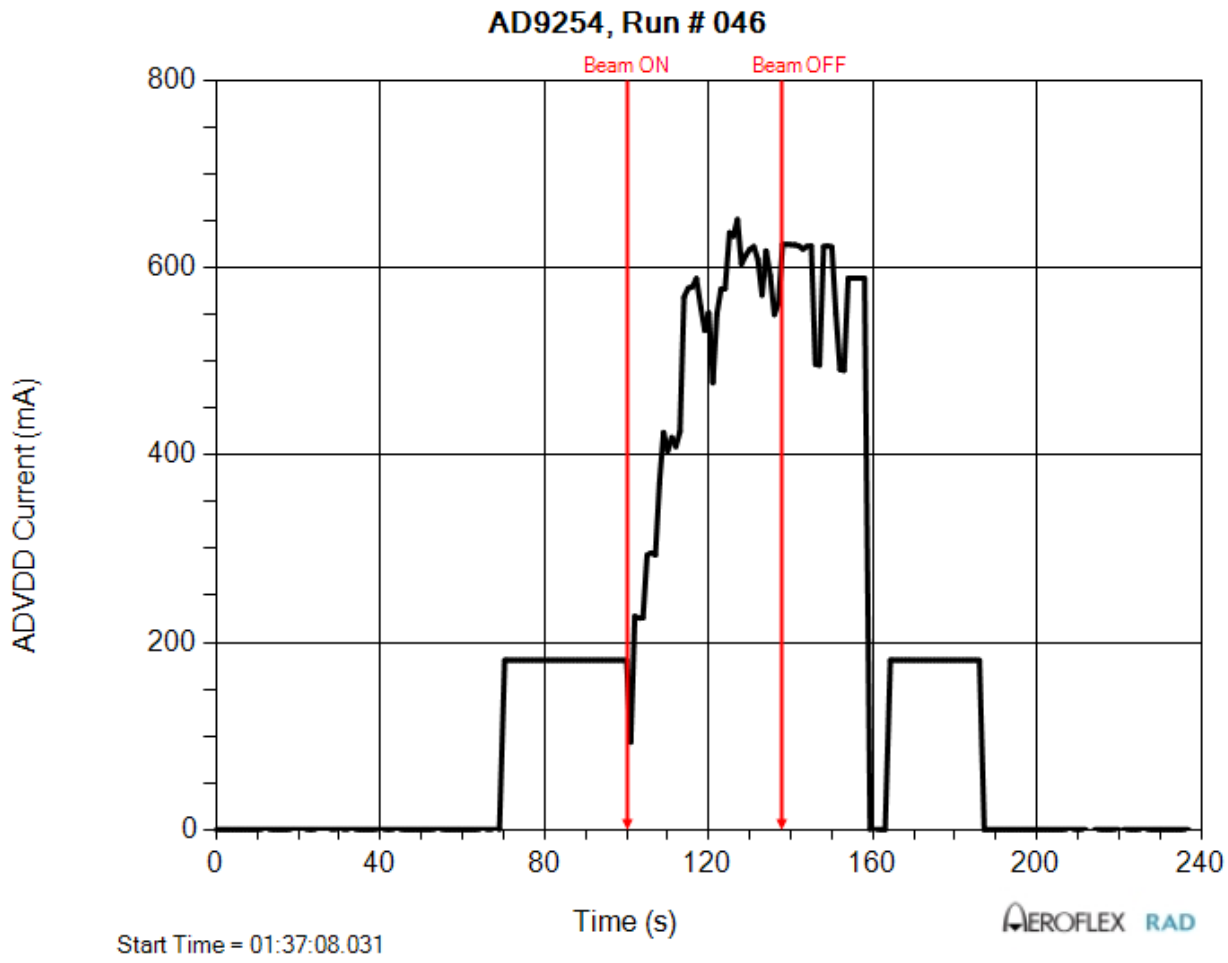

Figure 5.29. Unit-under-test analog supply current versus time/fluence during Run 46 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event in the analog supply after a few seconds of heavy ion exposure. See Table 5.1 for the details about the run.

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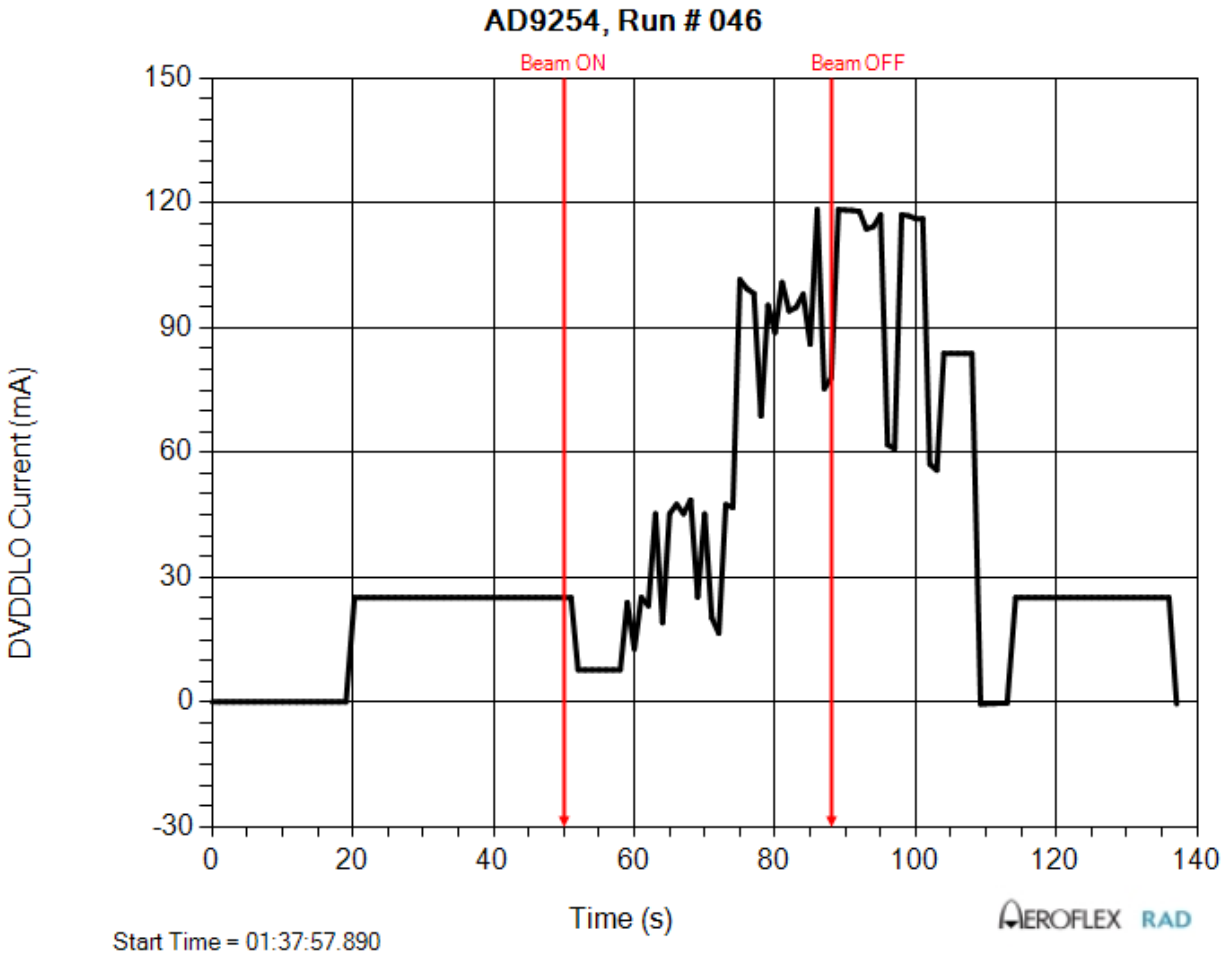

Figure 5.30. Unit-under-test digital supply current versus time/fluence during Run 46 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event in the digital supply after a 75-80 seconds of heavy ion exposure. The change in current during the run, prior to the SEL event is indicative of SEFIs events. See Table 5.1 for the details about the run.

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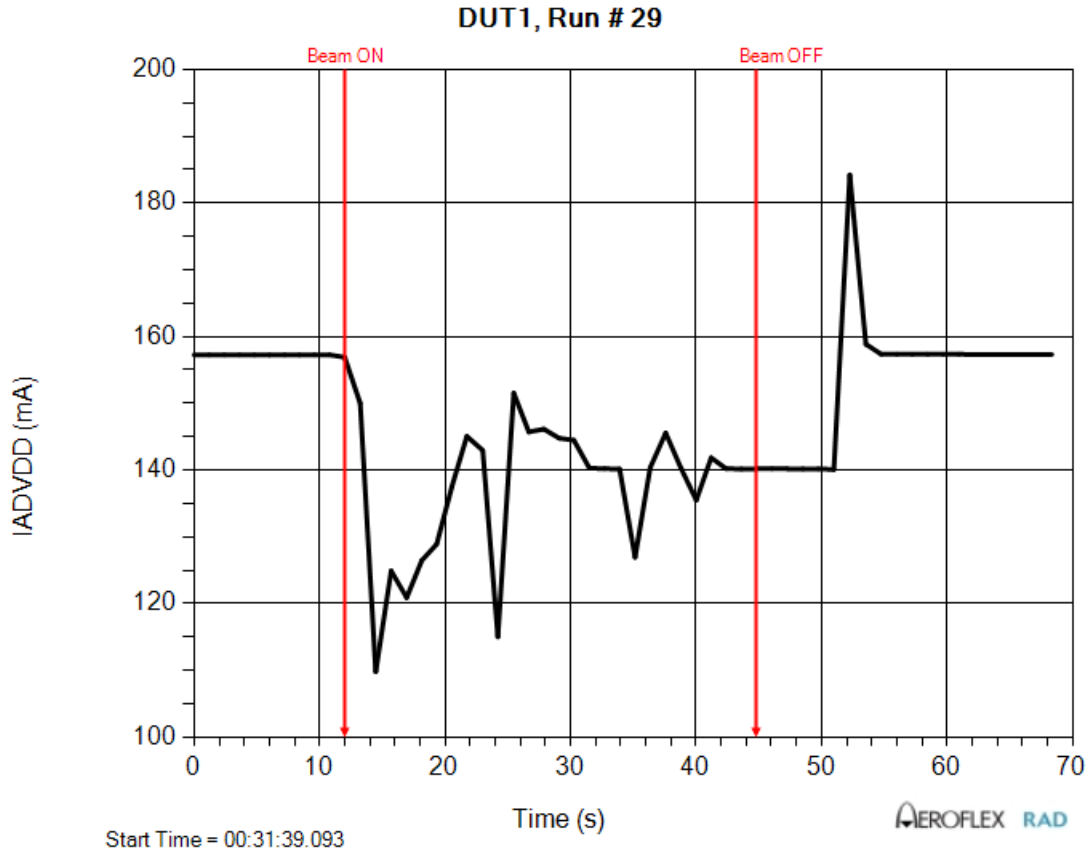

Figure 5.31. Unit-under-test analog supply current versus time/fluence during Run 29 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the analog supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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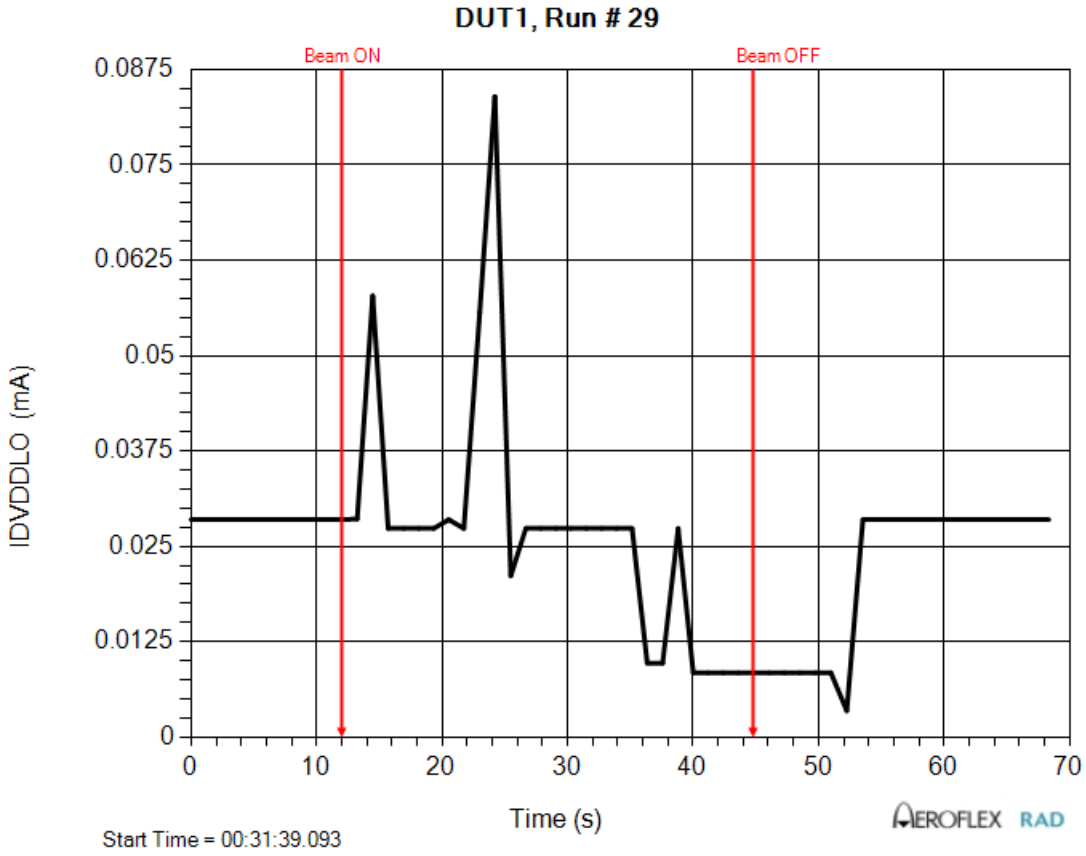

Figure 5.32. Unit-under-test digital supply current versus time/fluence during Run 29 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the digital supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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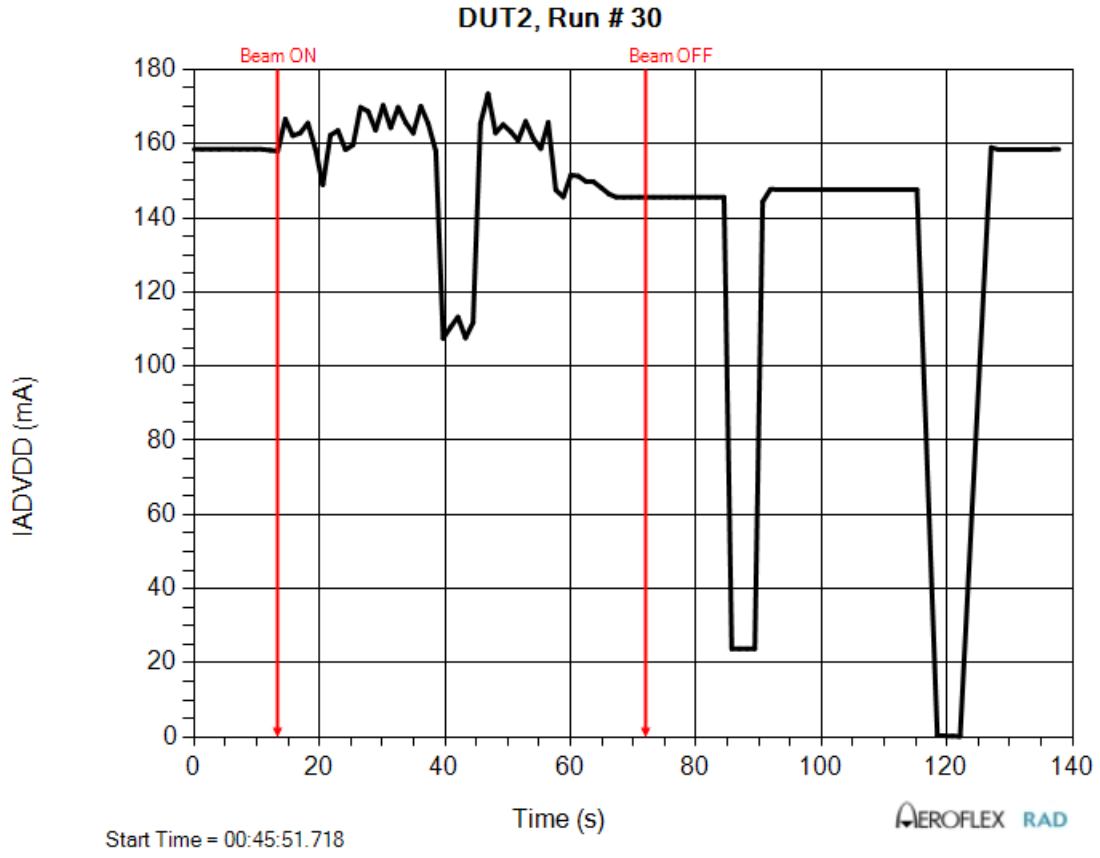

Figure 5.33. Unit-under-test analog supply current versus time/fluence during Run 30 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the analog supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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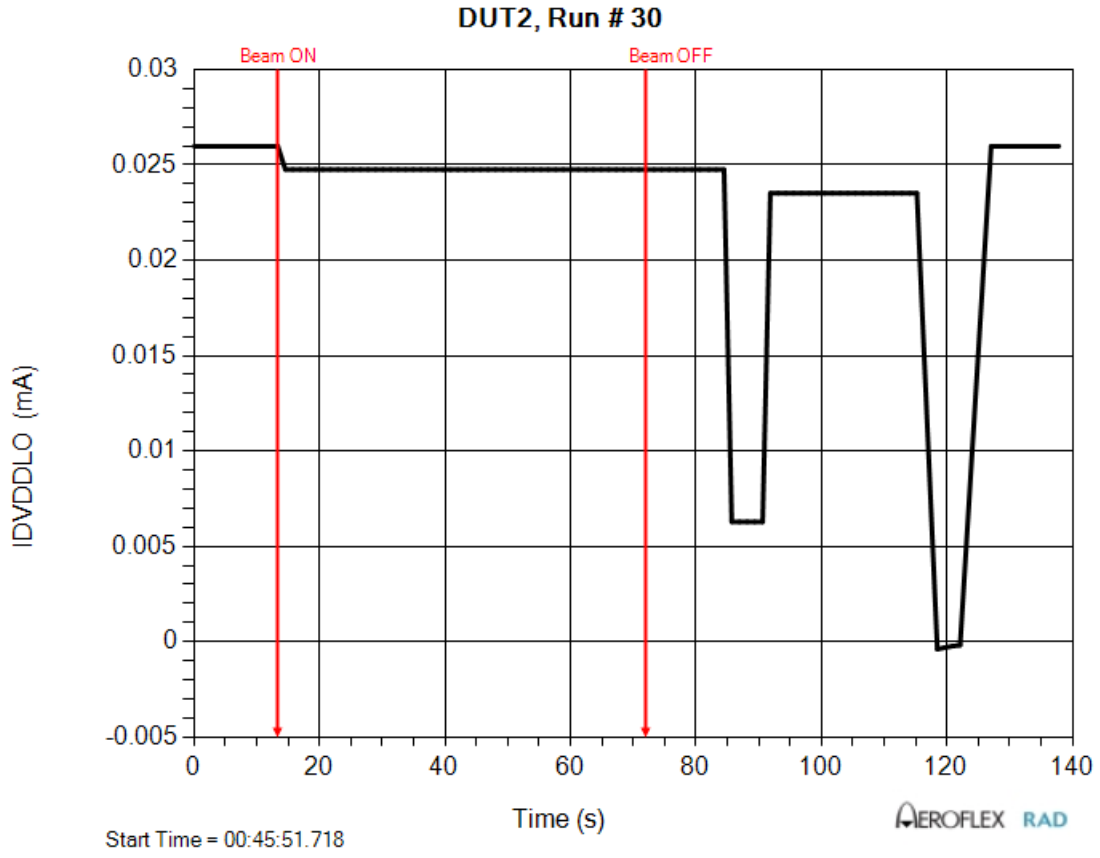

Figure 5.34. Unit-under-test digital supply current versus time/fluence during Run 30 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the digital supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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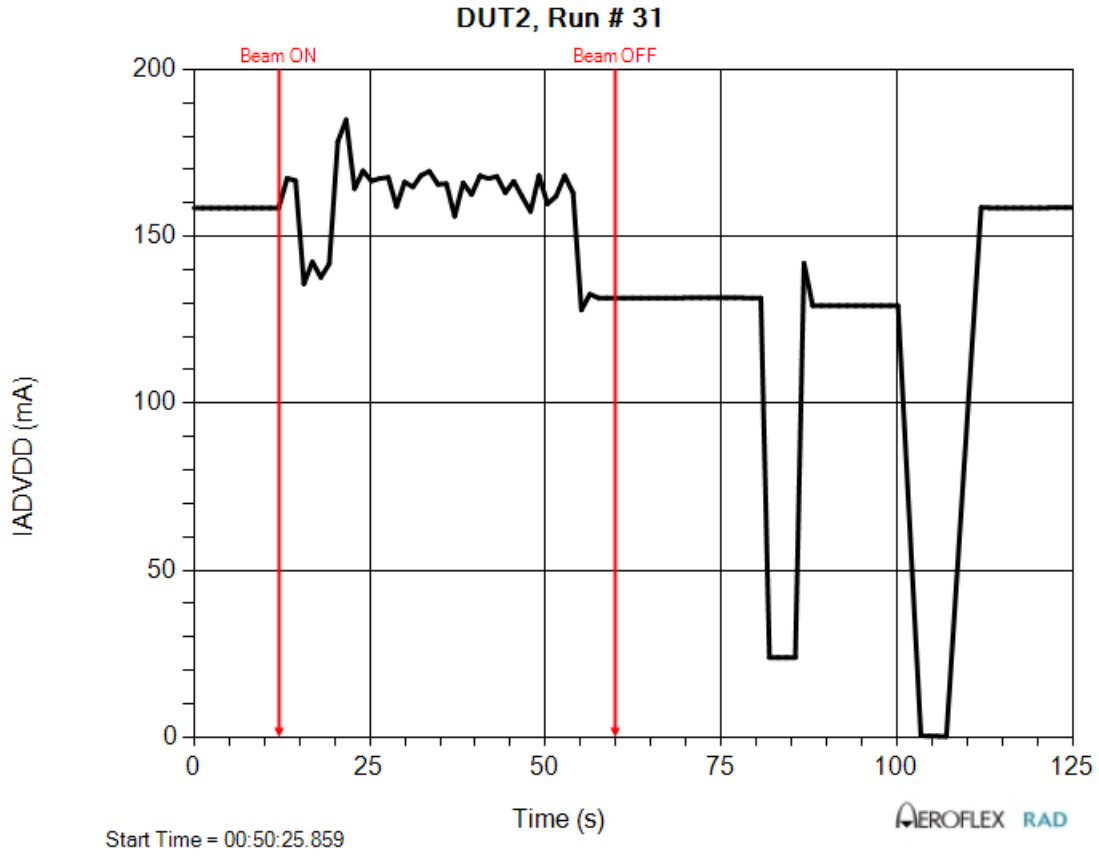

Figure 5.35. Unit-under-test analog supply current versus time/fluence during Run 31 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the analog supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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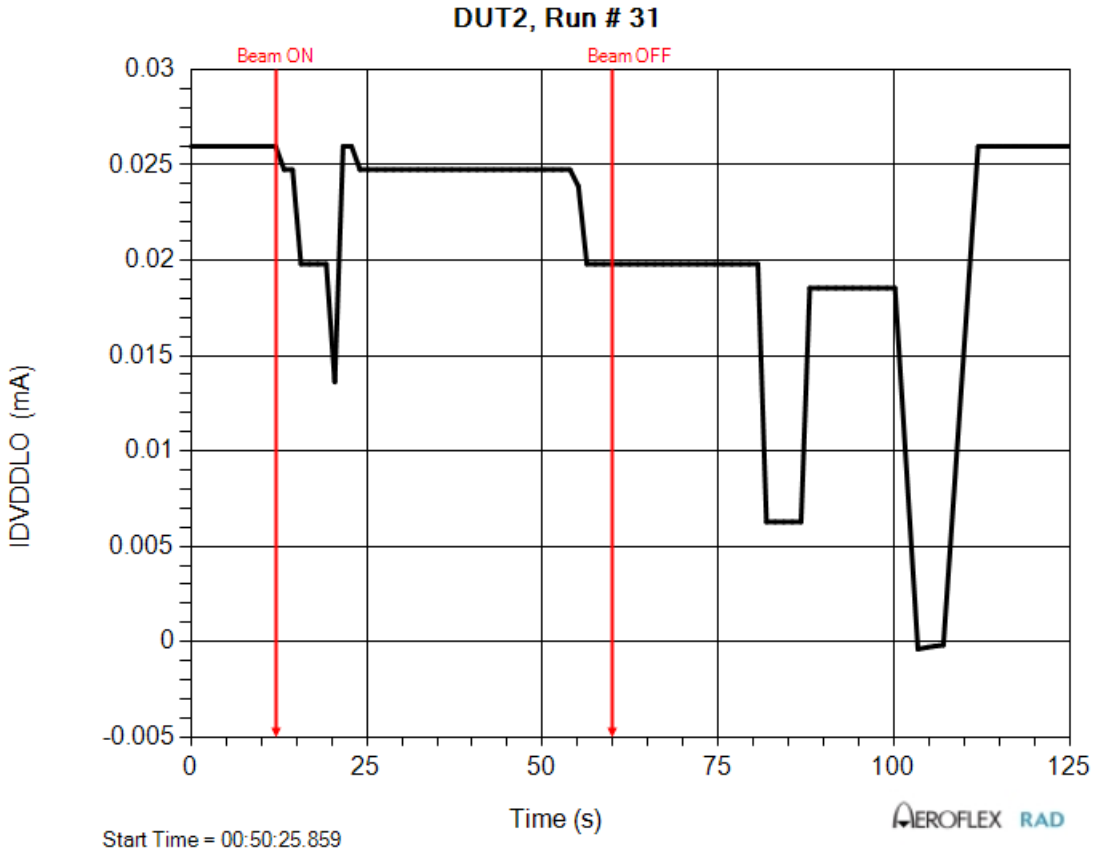

Figure 5.36. Unit-under-test digital supply current versus time/fluence during Run 31 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the digital supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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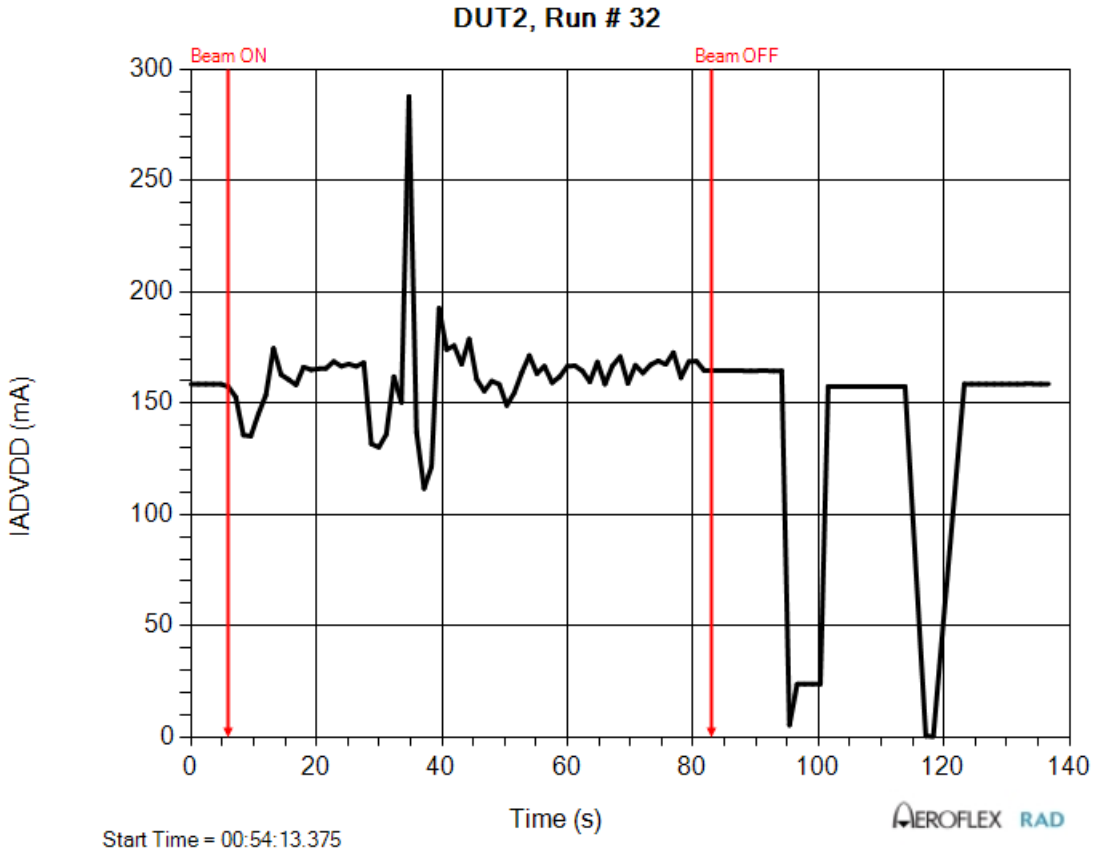

Figure 5.37. Unit-under-test analog supply current versus time/fluence during Run 32 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the analog supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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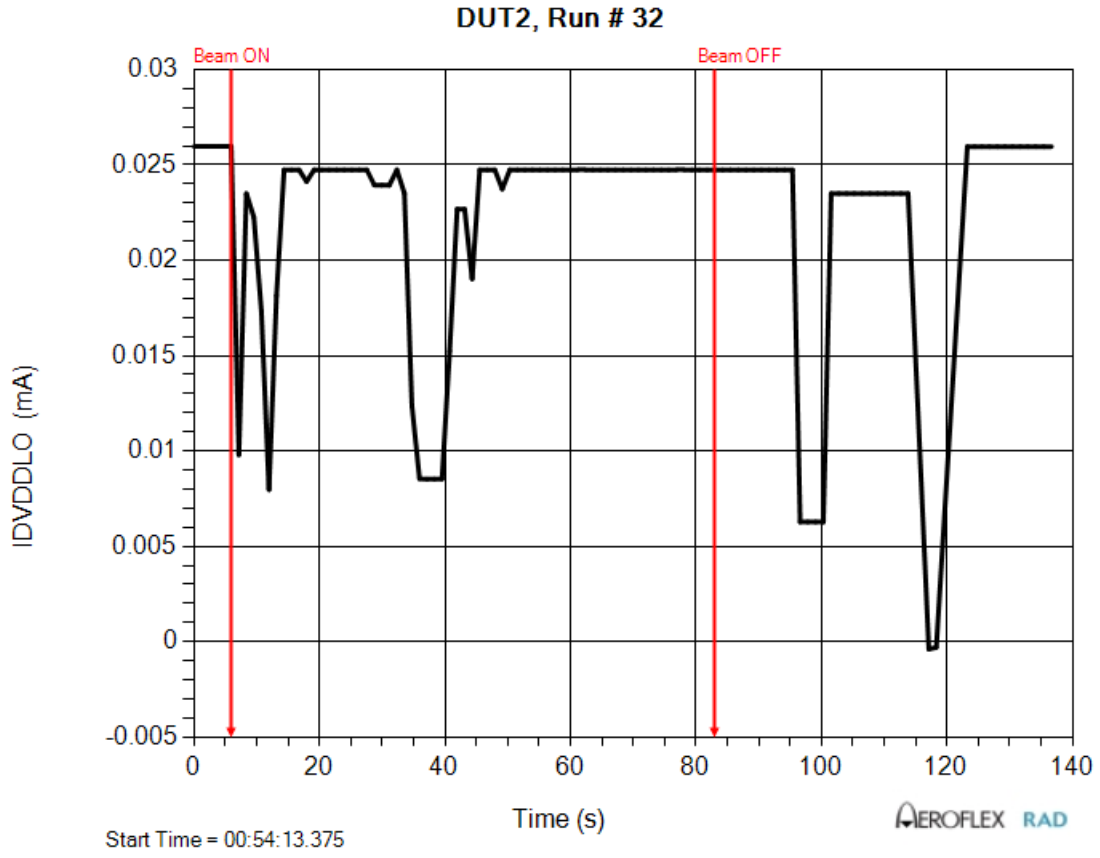

Figure 5.38. Unit-under-test digital supply current versus time/fluence during Run 32 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the digital supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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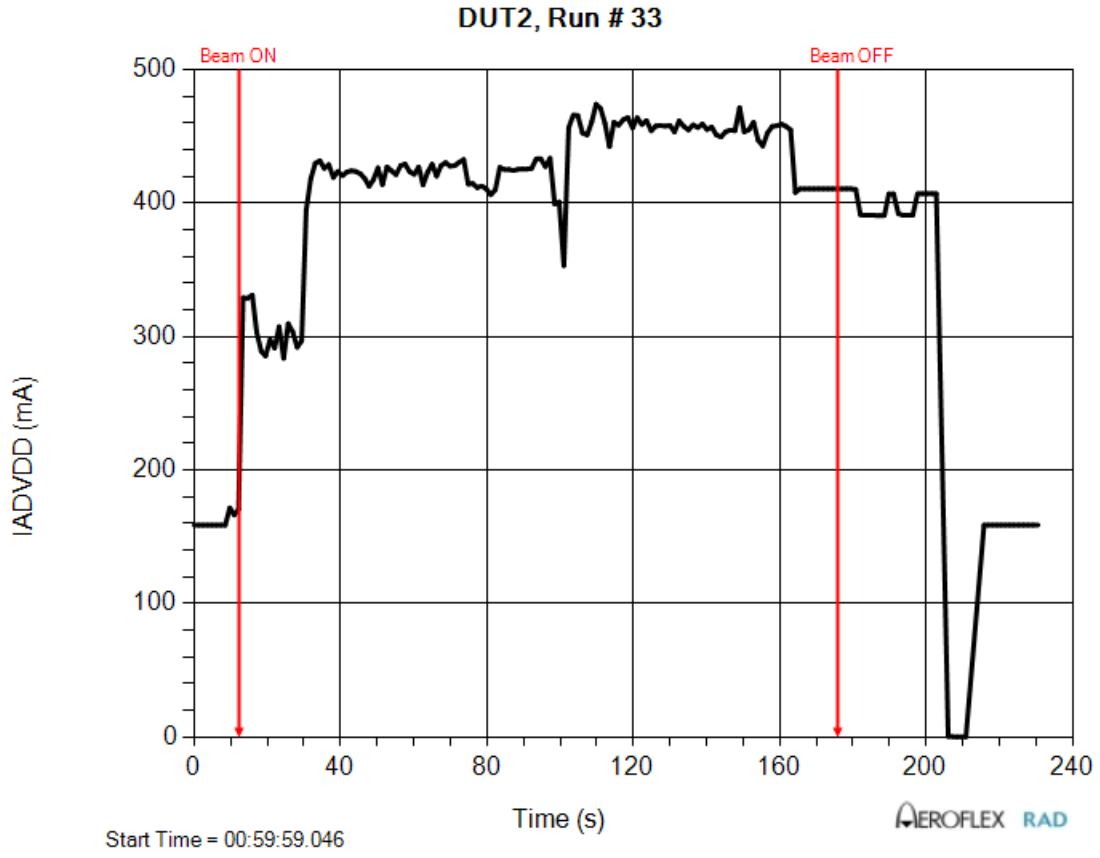

Figure 5.39. Unit-under-test analog supply current versus time/fluence during Run 33 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event in the analog supply immediately after heavy ion exposure. The change in current during the run, prior to the SEL event is indicative of SEFIs events. See Table 5.1 for the details about the run.

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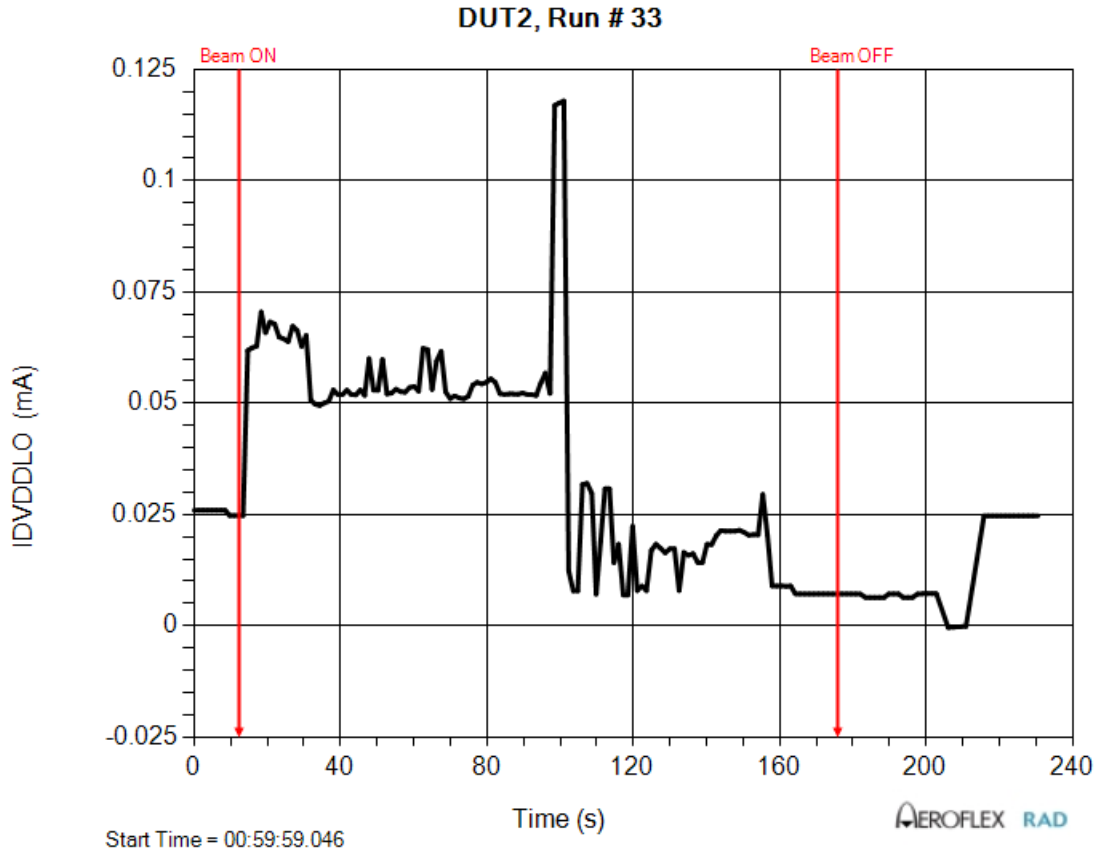

Figure 5.40. Unit-under-test digital supply current versus time/fluence during Run 33 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event in the digital supply immediately after heavy ion exposure. The change in current during the run, prior to the SEL event is indicative of SEFIs events. See Table 5.1 for the details about the run.

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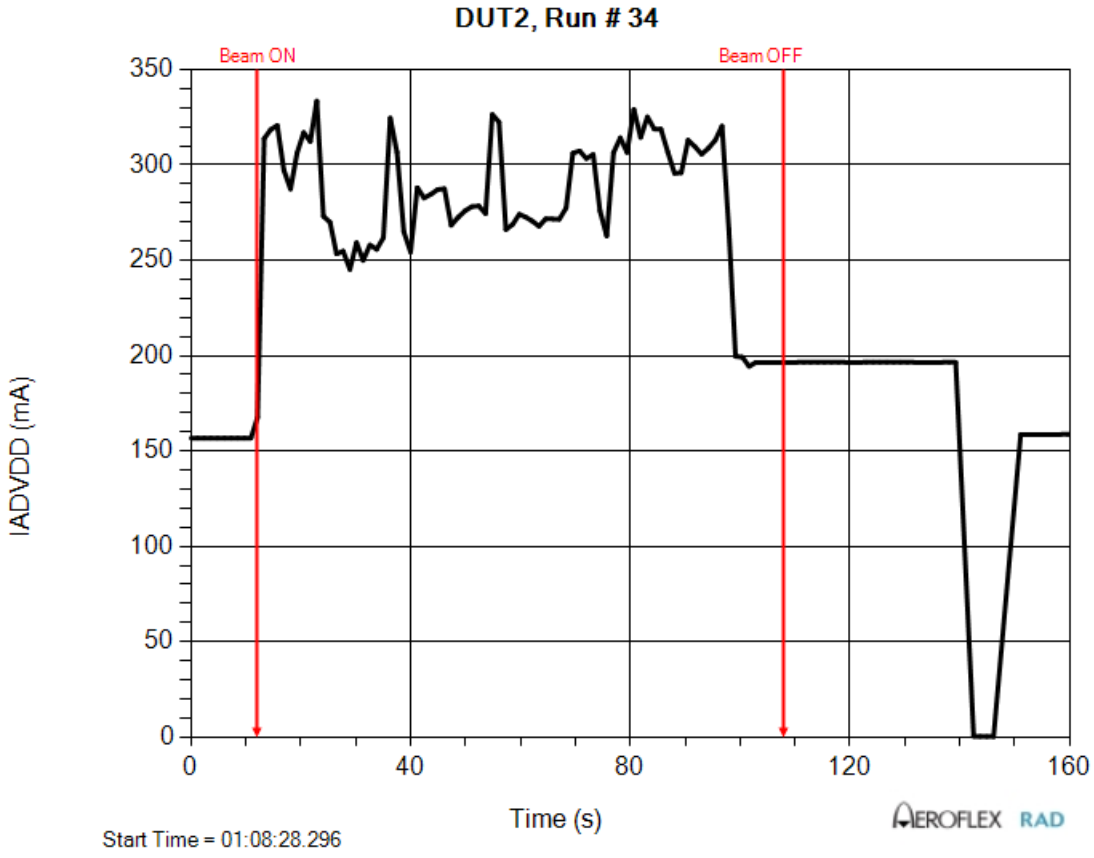

Figure 5.41. Unit-under-test analog supply current versus time/fluence during Run 34 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event in the analog supply immediately after heavy ion exposure. See Table 5.1 for the details about the run.

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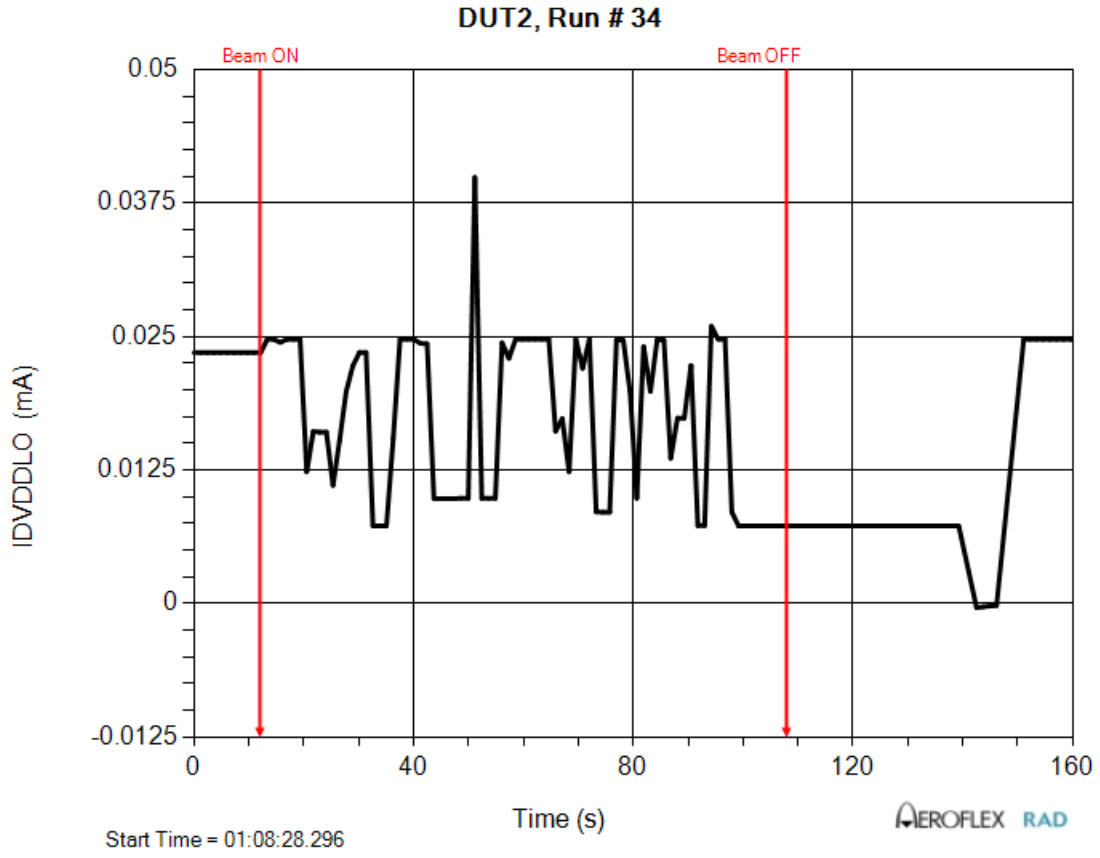

Figure 5.42. Unit-under-test digital supply current versus time/fluence during Run 34 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the digital supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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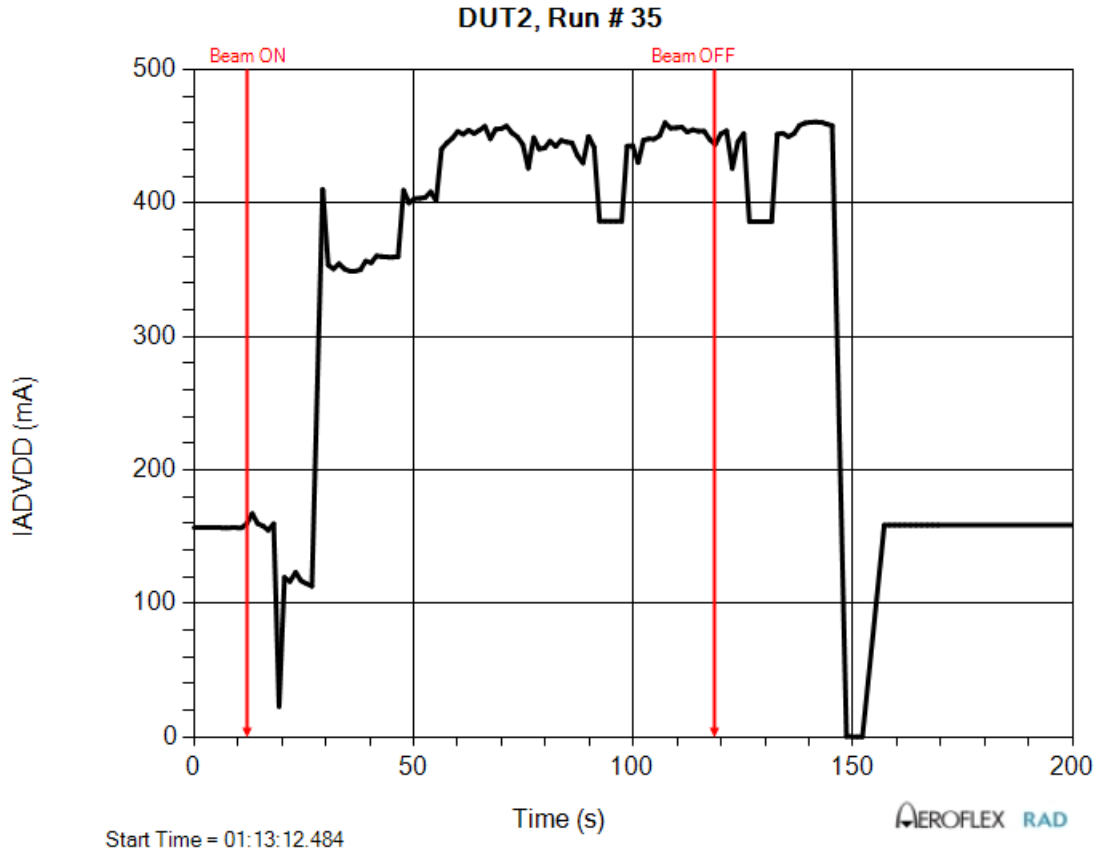

Figure 5.43. Unit-under-test analog supply current versus time/fluence during Run 35 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event in the analog supply after 15-20 seconds after heavy ion exposure. The change in current during the run, prior to the SEL event is indicative of SEFIs events. See Table 5.1 for the details about the run.

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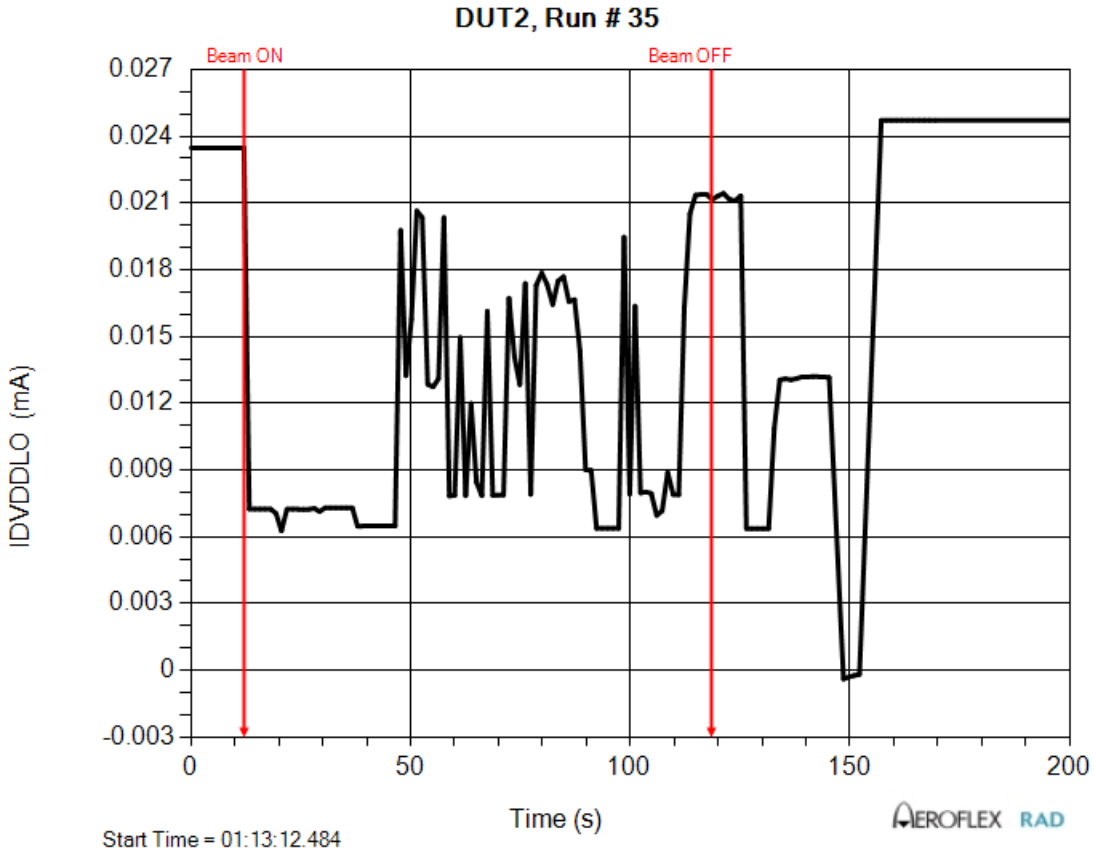

Figure 5.44. Unit-under-test digital supply current versus time/fluence during Run 35 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the digital supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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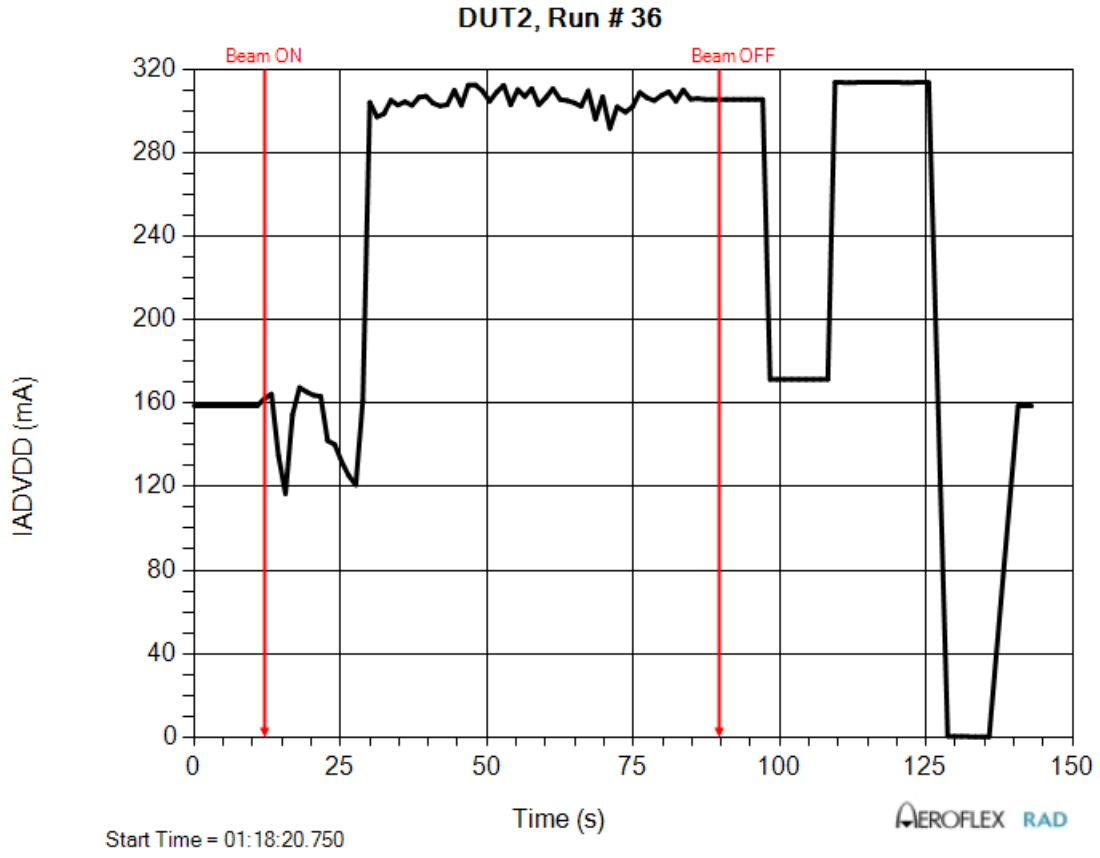

Figure 5.45. Unit-under-test analog supply current versus time/fluence during Run 36 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event in the analog supply after 15-20 seconds after heavy ion exposure. The change in current during the run, prior to the SEL event is indicative of SEFIs events. See Table 5.1 for the details about the run.

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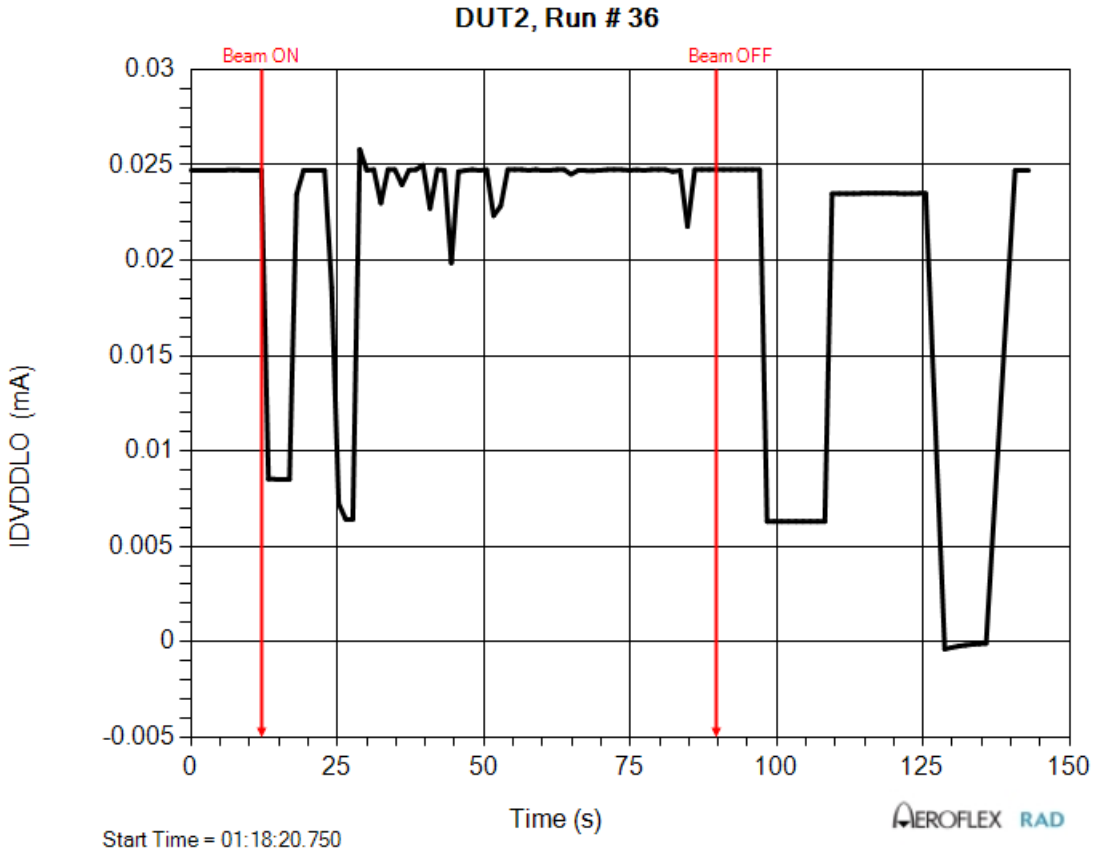

Figure 5.46. Unit-under-test digital supply current versus time/fluence during Run 36 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the digital supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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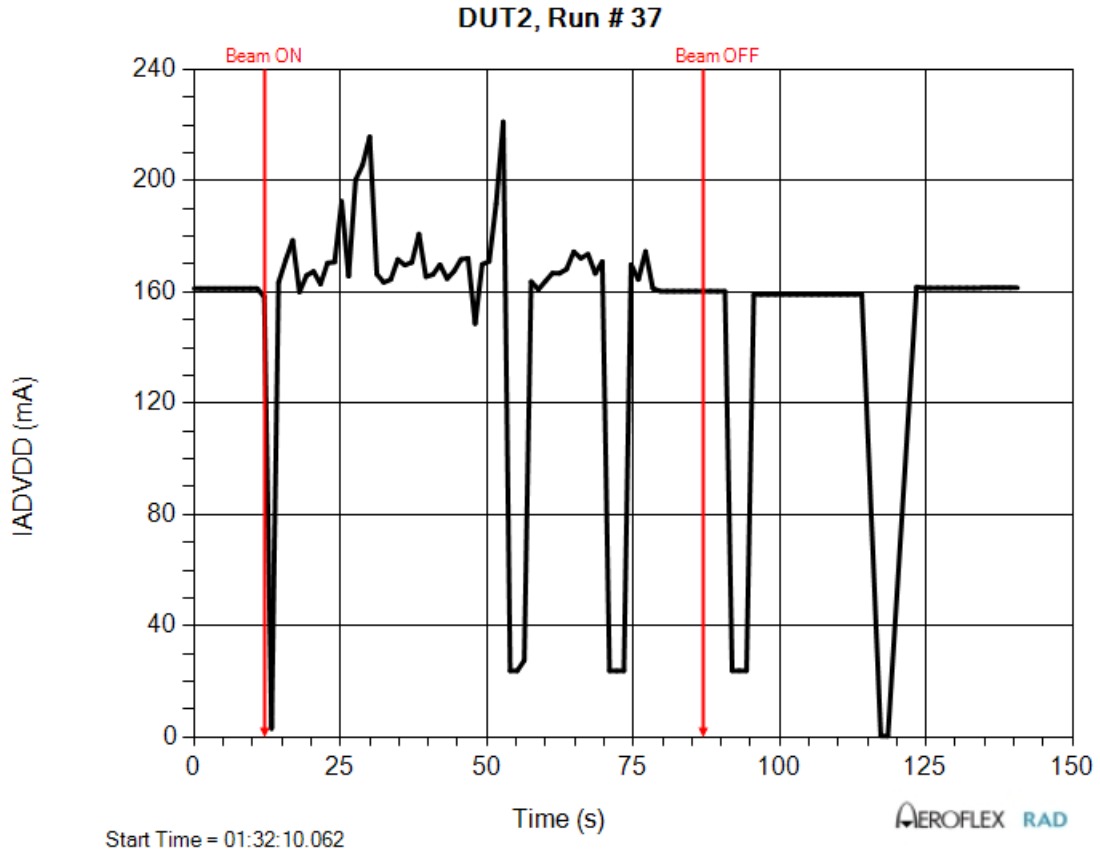

Figure 5.47. Unit-under-test analog supply current versus time/fluence during Run 37 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the analog supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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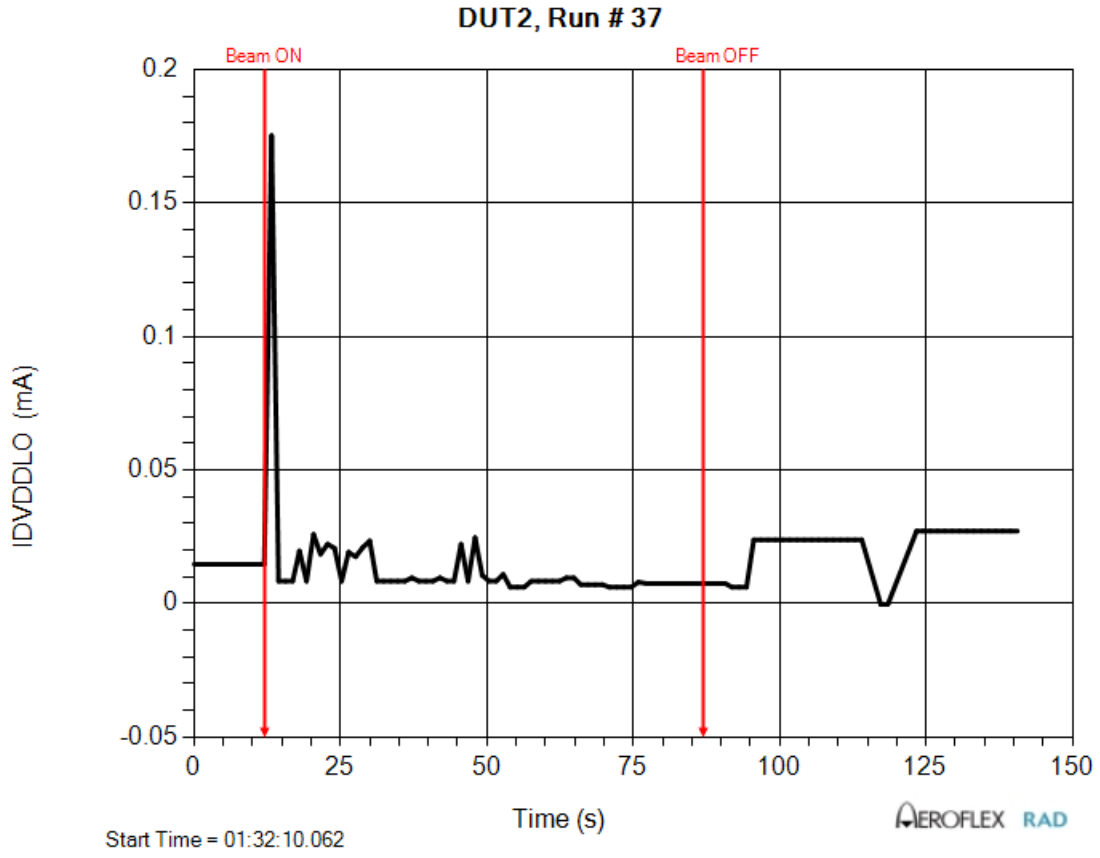

Figure 5.48. Unit-under-test digital supply current versus time/fluence during Run 37 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the digital supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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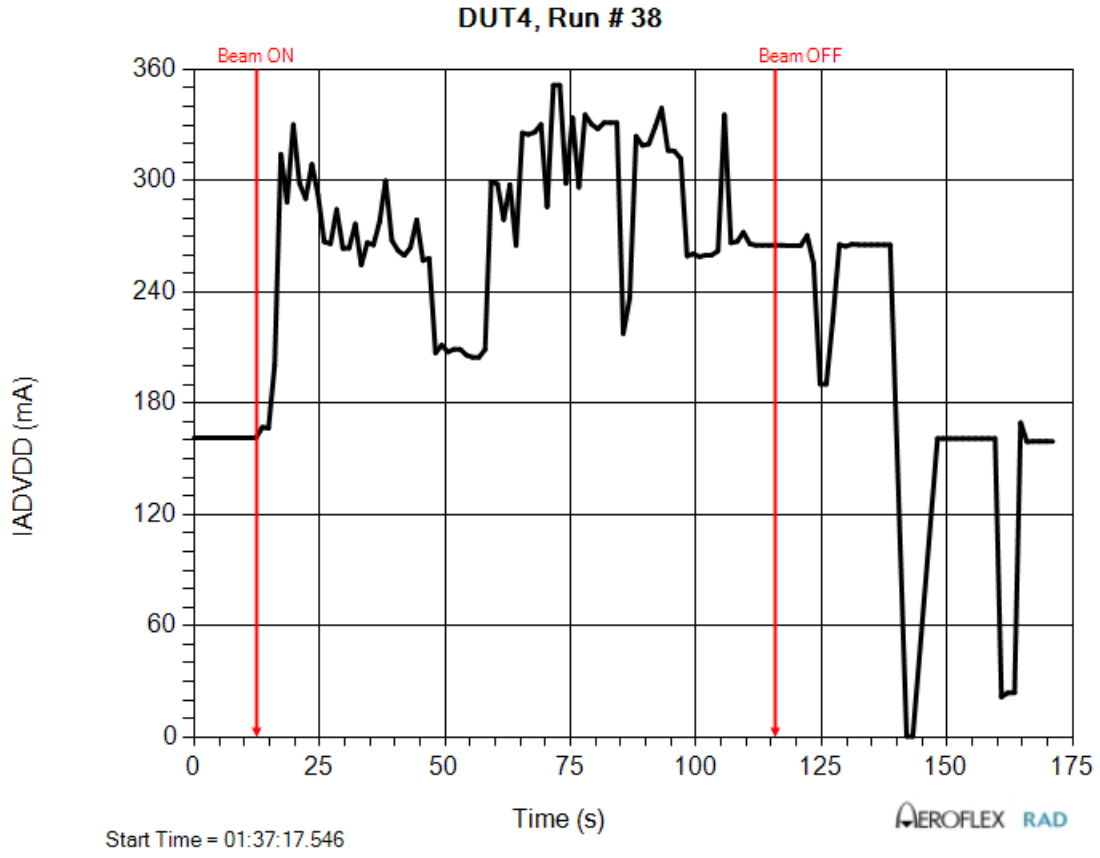

Figure 5.49. Unit-under-test analog supply current versus time/fluence during Run 38 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event in the analog supply after a few seconds after heavy ion exposure. The change in current during the run, prior to the SEL event is indicative of SEFIs events. See Table 5.1 for the details about the run.

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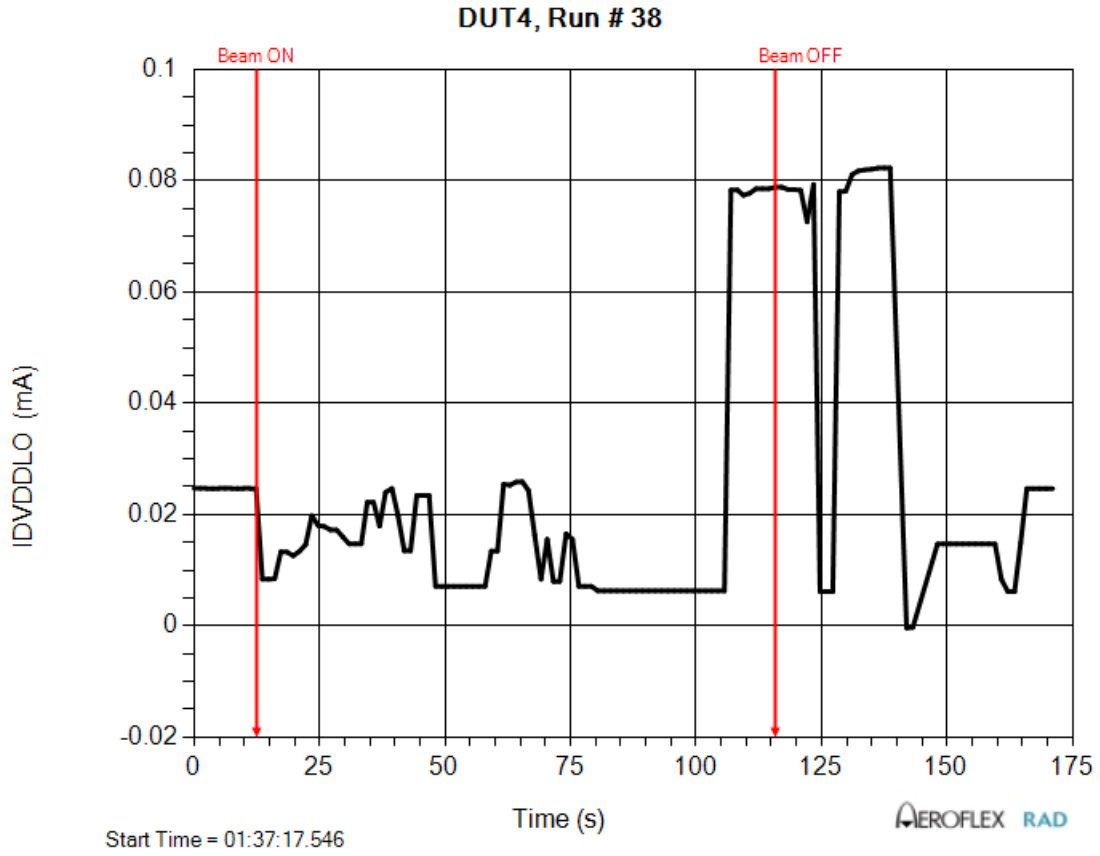

Figure 5.50. Unit-under-test digital supply current versus time/fluence during Run 38 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event in the digital supply ~100 seconds after heavy ion exposure. The change in current during the run, prior to the SEL event is indicative of SEFIs events. See Table 5.1 for the details about the run.

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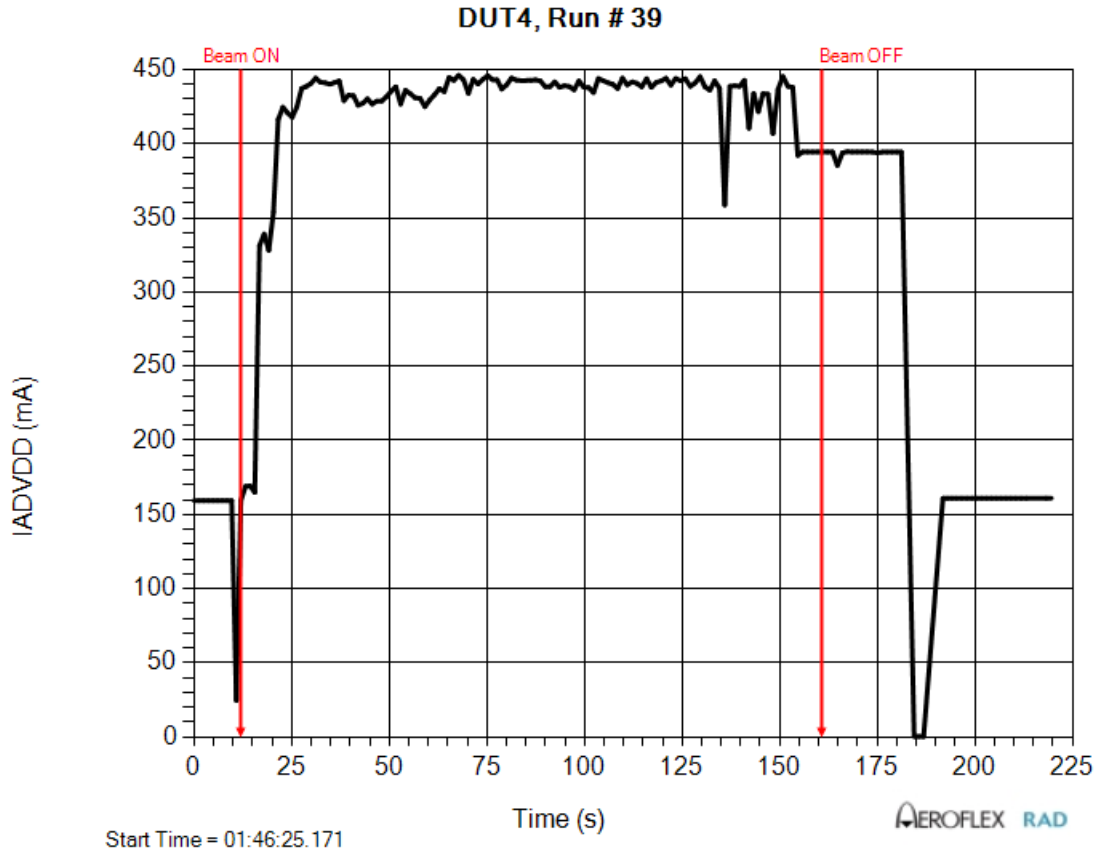

Figure 5.51. Unit-under-test analog supply current versus time/fluence during Run 39 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test experiences an SEL event in the analog supply after a few seconds after heavy ion exposure. The change in current during the run, prior to the SEL event is indicative of SEFIs events. See Table 5.1 for the details about the run.

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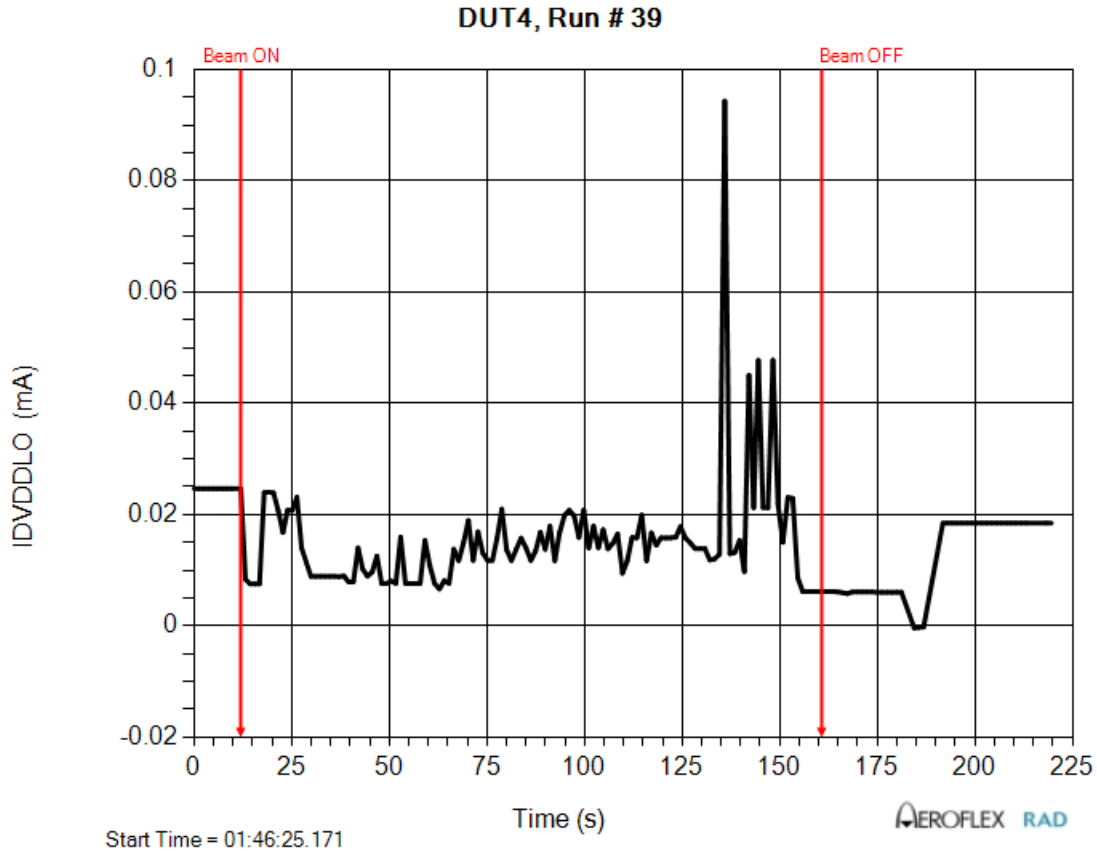

Figure 5.52. Unit-under-test digital supply current versus time/fluence during Run 39 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the digital supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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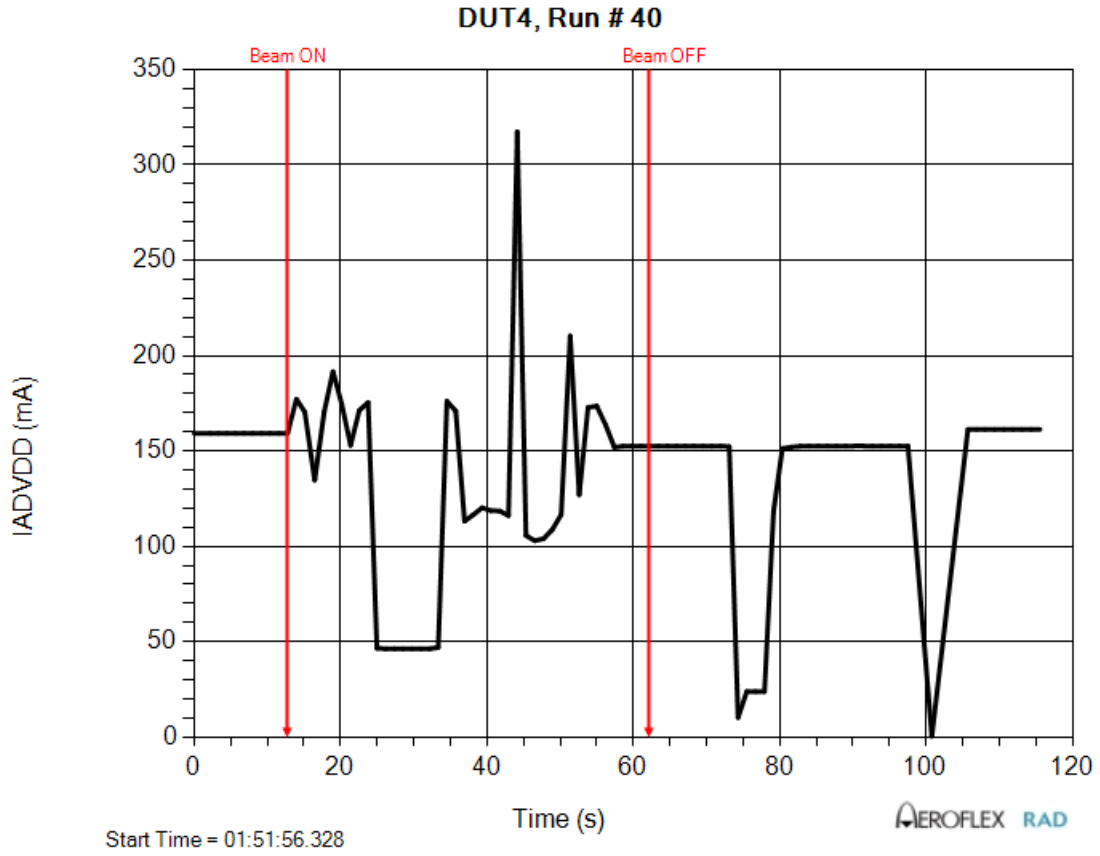

Figure 5.53. Unit-under-test analog supply current versus time/fluence during Run 40 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the analog supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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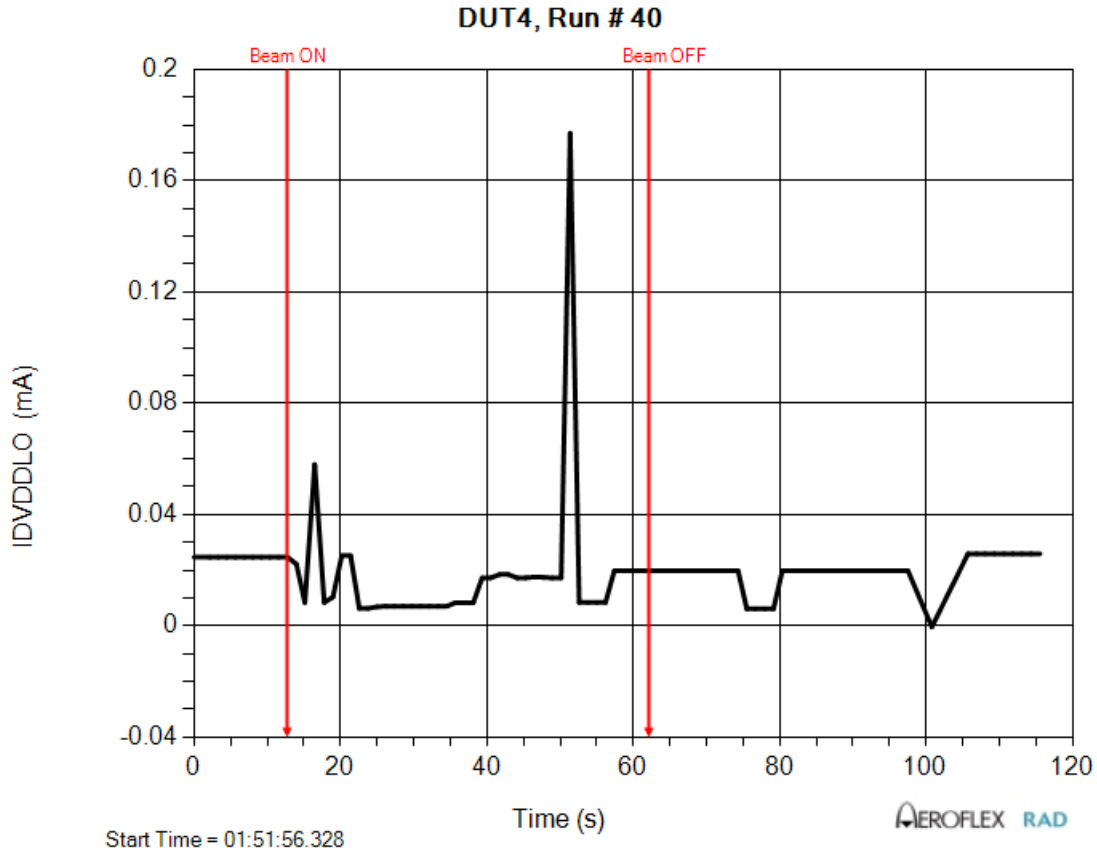

Figure 5.54. Unit-under-test digital supply current versus time/fluence during Run 40 for the AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter. The data shows that the unit-under-test did not experience an SEL event in the digital supply. The change in current during the run is indicative of SEFI events. See Table 5.1 for the details about the run.

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6.0. Summary/Conclusions

The single event latch-up testing described in this final report was performed at the Lawrence Berkeley National Laboratories (LBNL) using the 88-Inch Cyclotron on December 7th, 2011, February 6th, 2012, and April 5th, 2012. The 88-Inch Cyclotron is operated by the University of California for the US Department of Energy (DOE) and is a K=140 sector-focused cyclotron with both light- and heavy-ion capabilities.

The AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter described in this final report was irradiated using Kr and Xe with a supply voltage of +3.6V and +1.9V and with a 120MHz signal on the clock. The units-under-test were exposed using the Berkeley 10MeV/n beam. The 10MeV/n beam was used to provide sufficient range in silicon while meeting the minimum LET requirements of the program of 80MeV-cm^2/mg. The range to the Bragg Peak for Xe at this energy is approximately 60µm.

The devices were irradiated to a minimum fluence of 107 ion/cm^2. The flux varied somewhat during the testing, but was approximately 1x10^5 ion/cm^2-s to 2x10^5 ion/cm^2-s. During the testing the irradiations continued until either the minimum fluence was reached or a latchup event was observed. In general the following minimum criteria must be met for a device to pass SEL testing: During the heavy ion exposure the DUT's supply current must remain within the unit's specification limit without cycling power. If this condition is not satisfied following the heavy ion testing, then the SEL testing could be logged as a failure.

Using the criteria established for pass/fail of this single event latchup test, the Analog Devices AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter (of the lot date code identified on the first page of this report) FAILED. The units-under-test latched up at an LET of 31 MeV-cm^2/mg 110°C). The units-under-test did not latchup, but did suffer SEFI events at an LETs of below 31 MeV-cm^2/mg.

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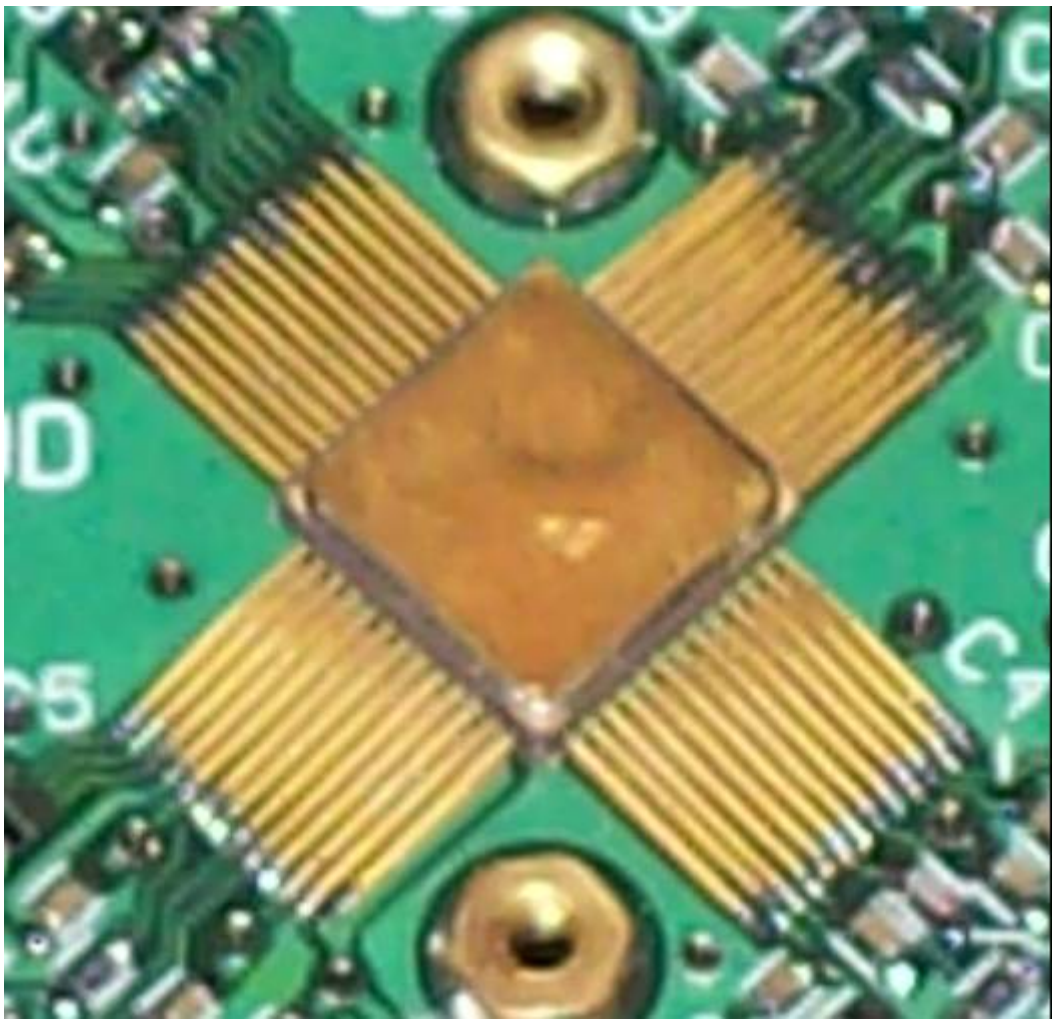
Appendix A: Photograph of a Sample Unit-Under-Test for Device Traceability and a Decapsulated Unit Ready for SEL Testing *(note that the units-under-test came unmarked)*



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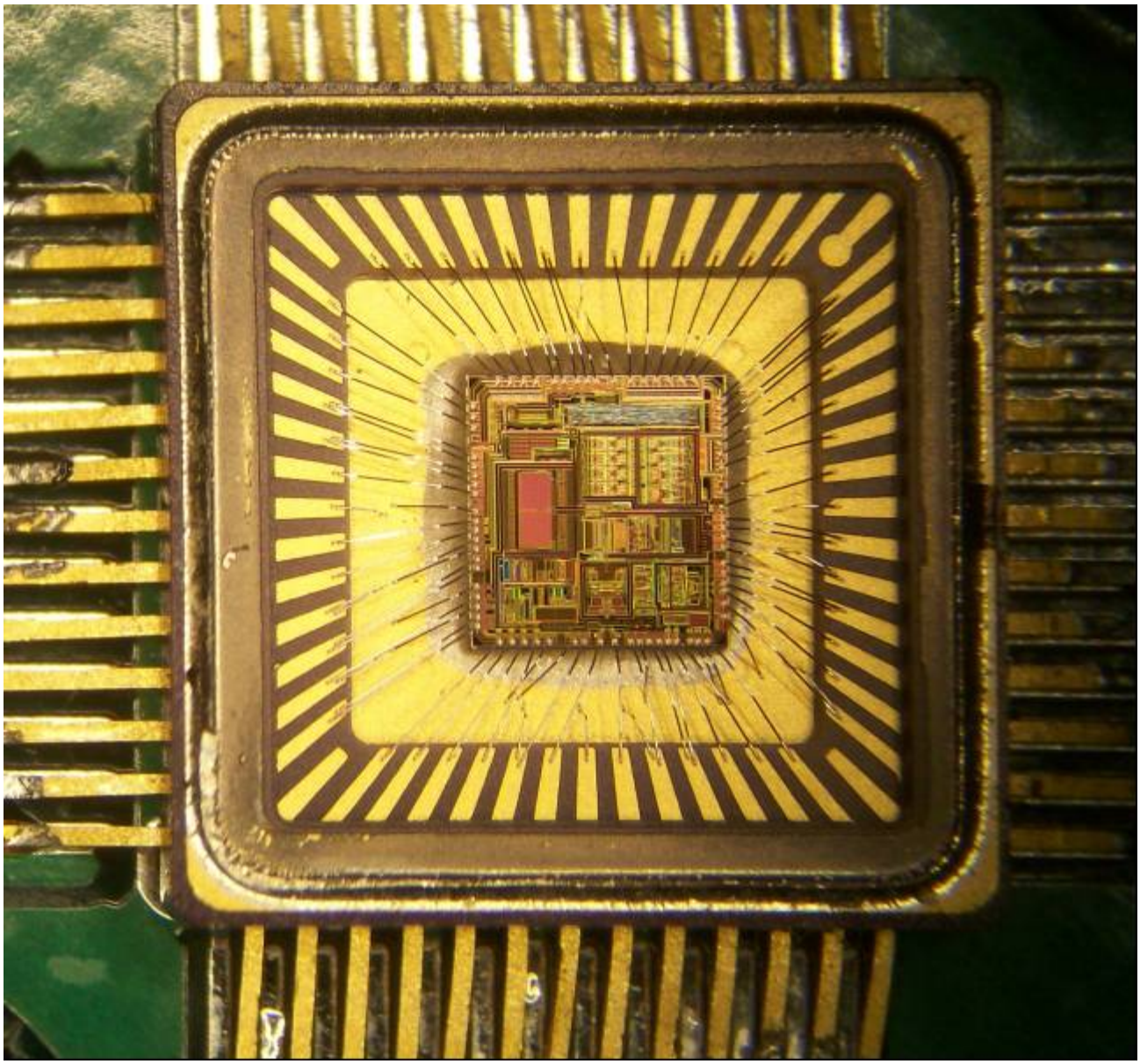

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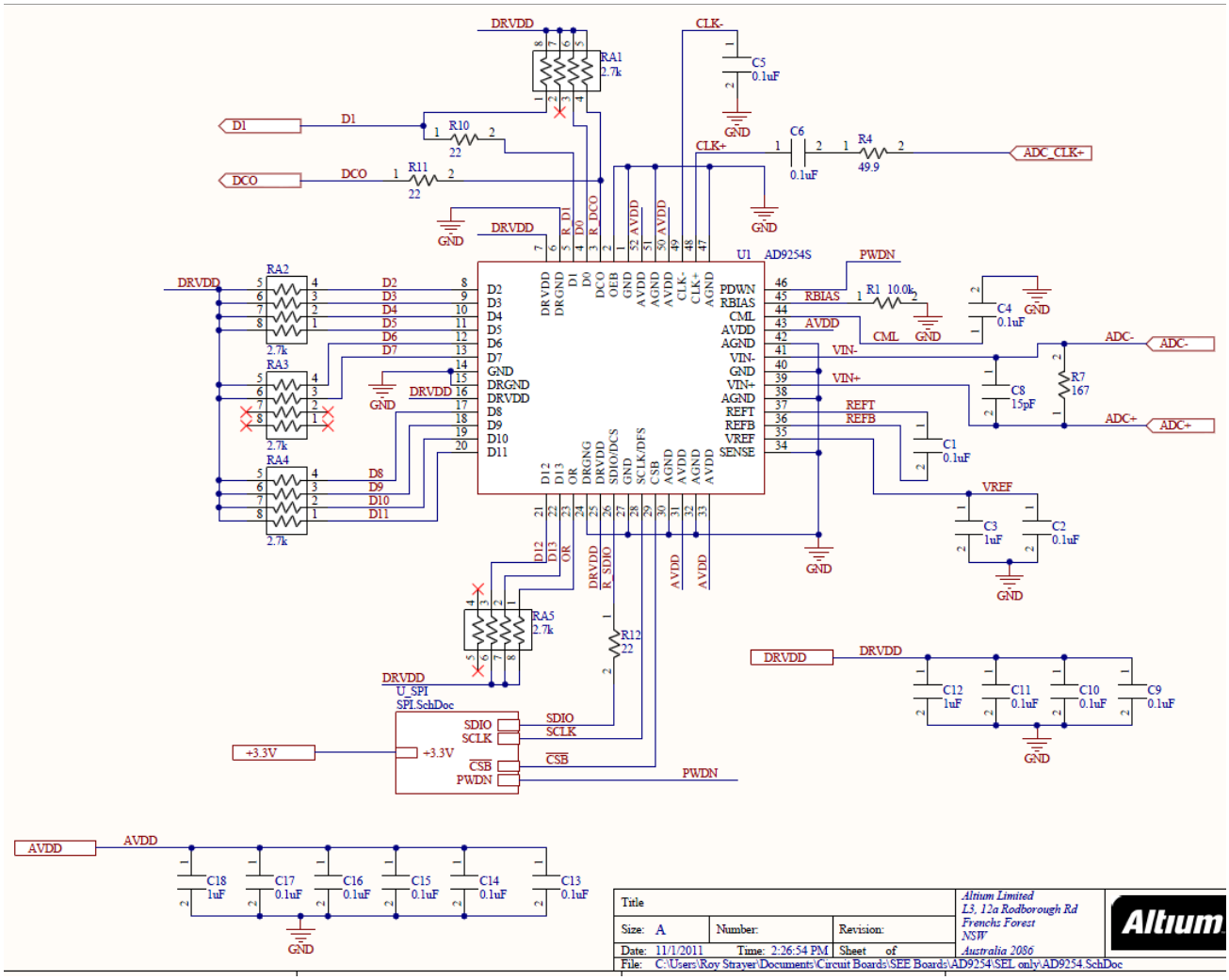
Appendix B: Electrical Bias Schematics Used During Heavy Ion Exposure



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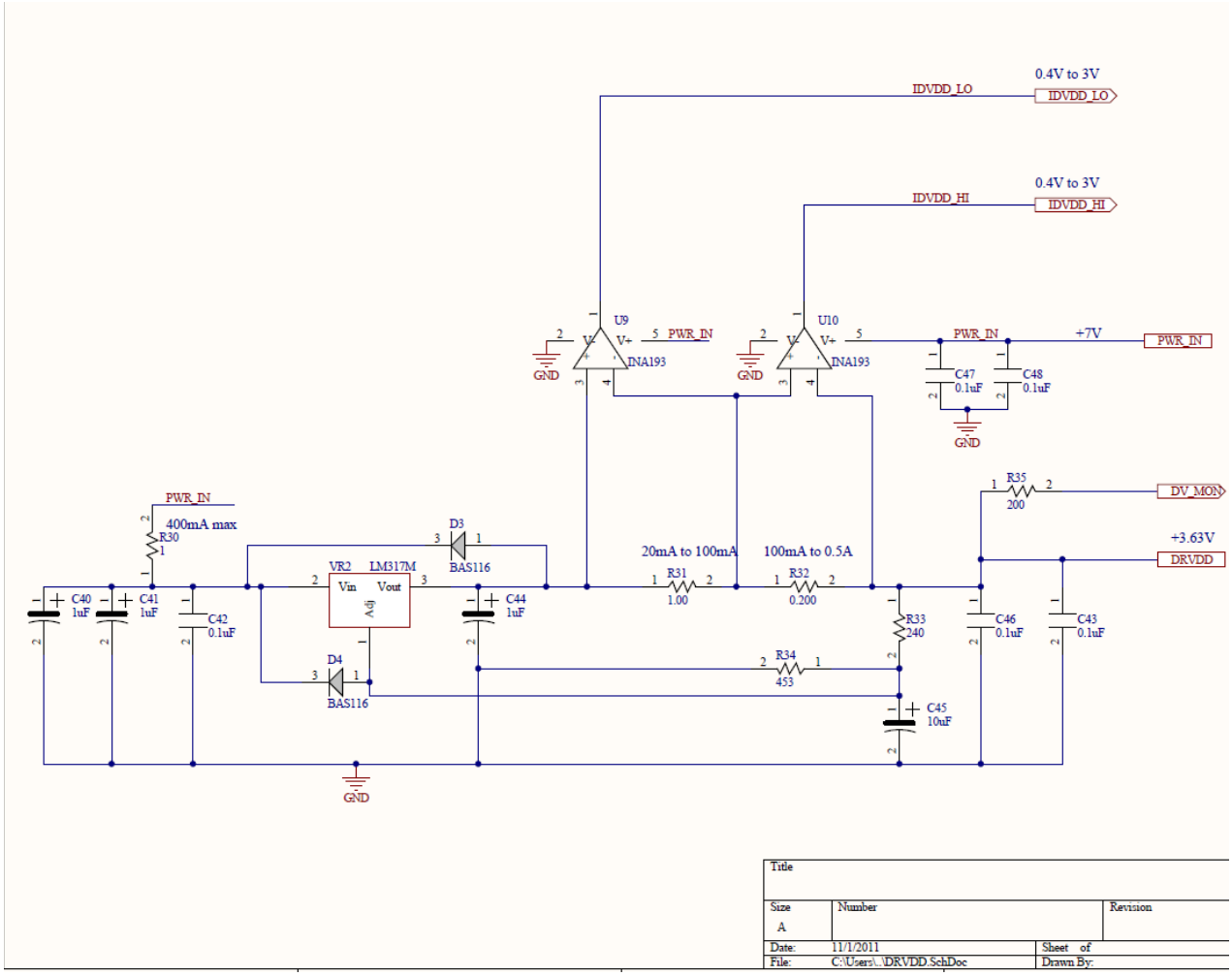

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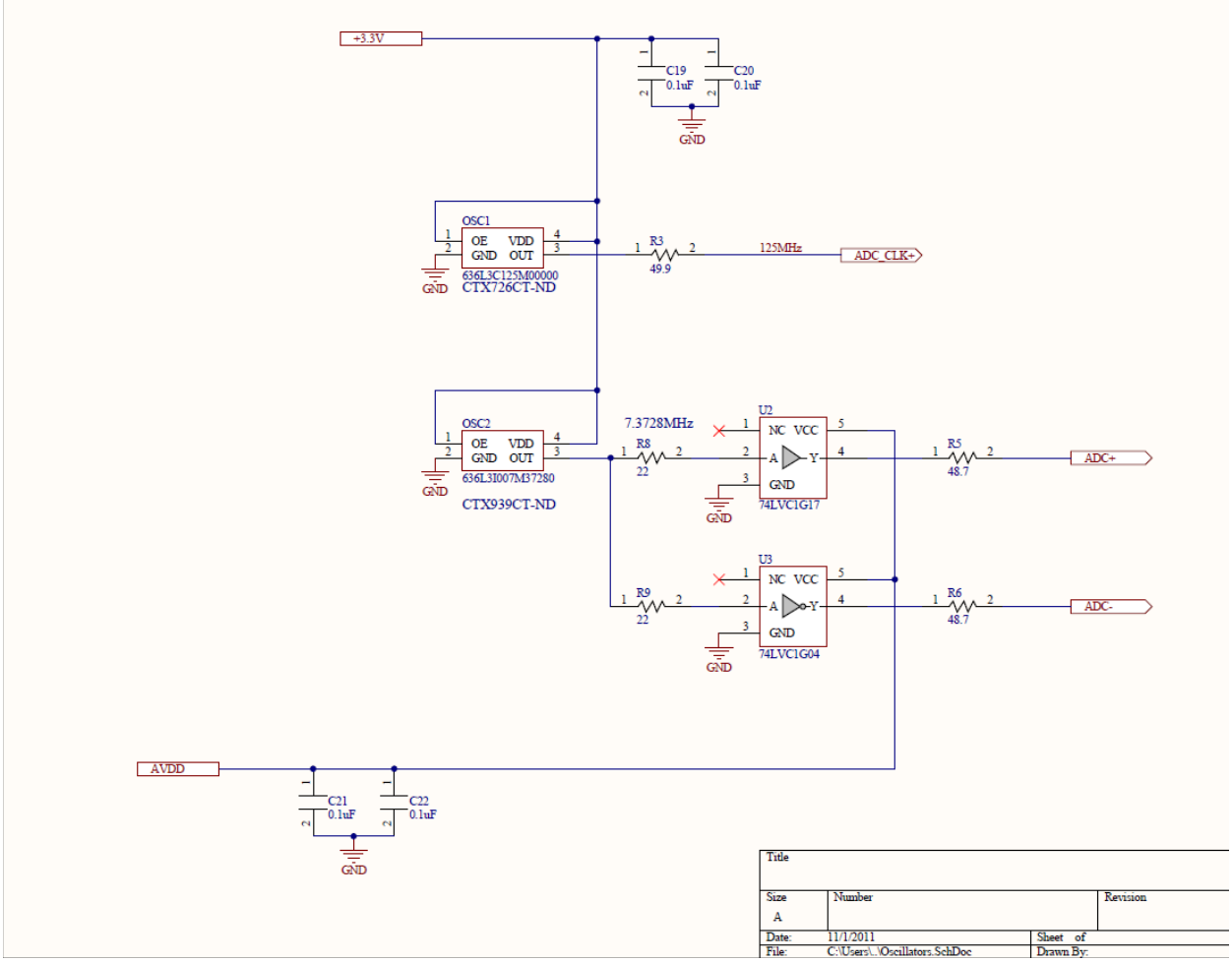

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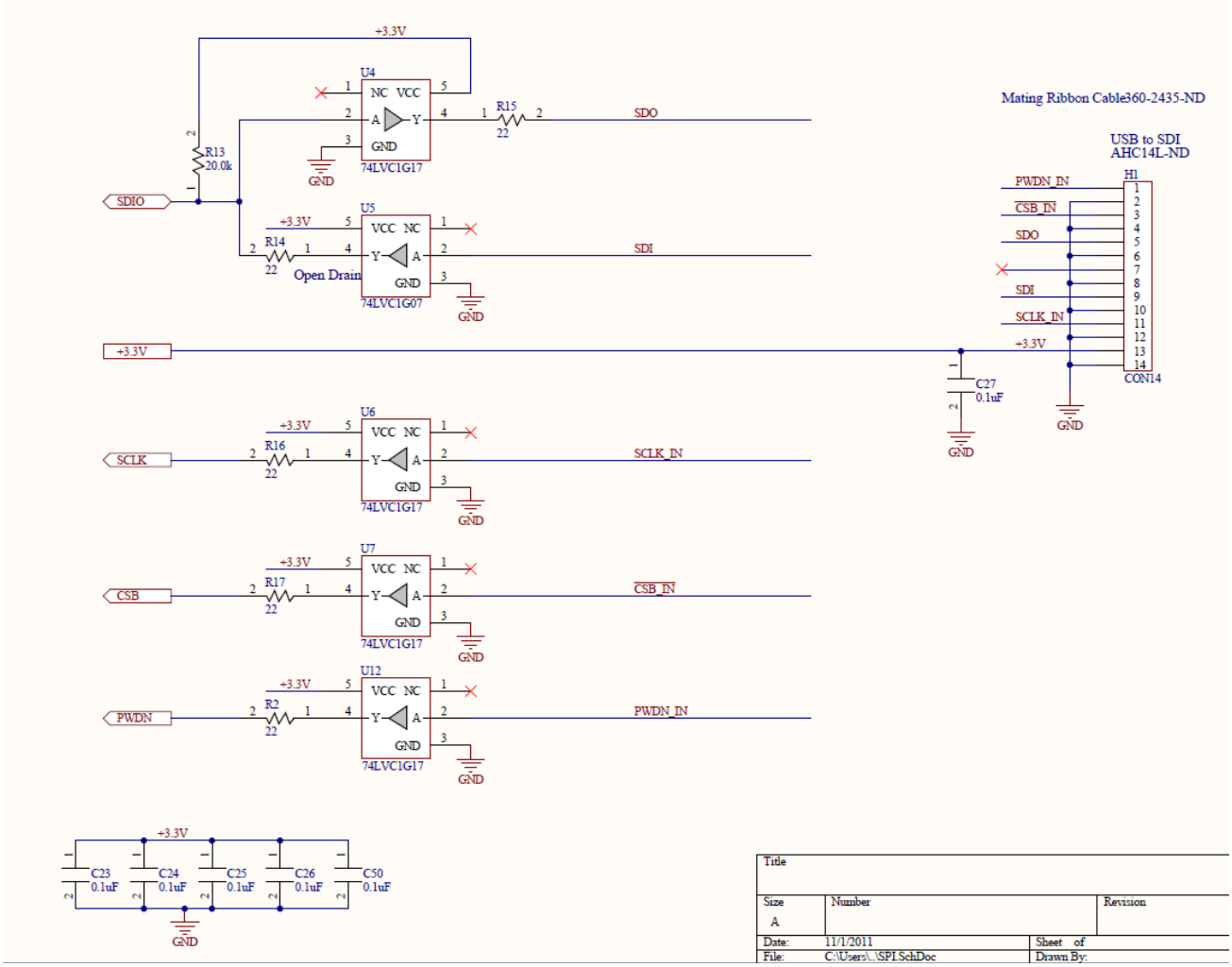

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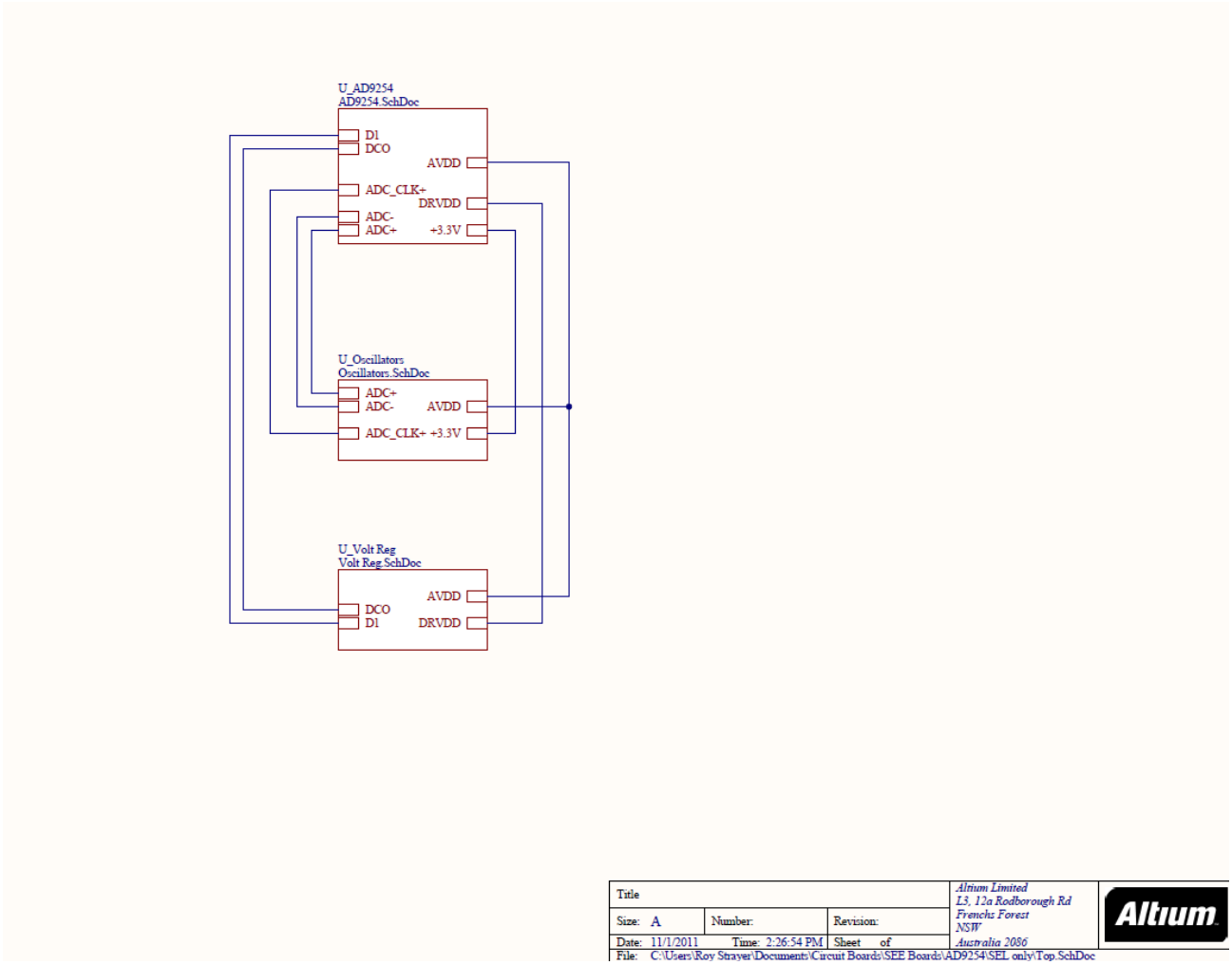

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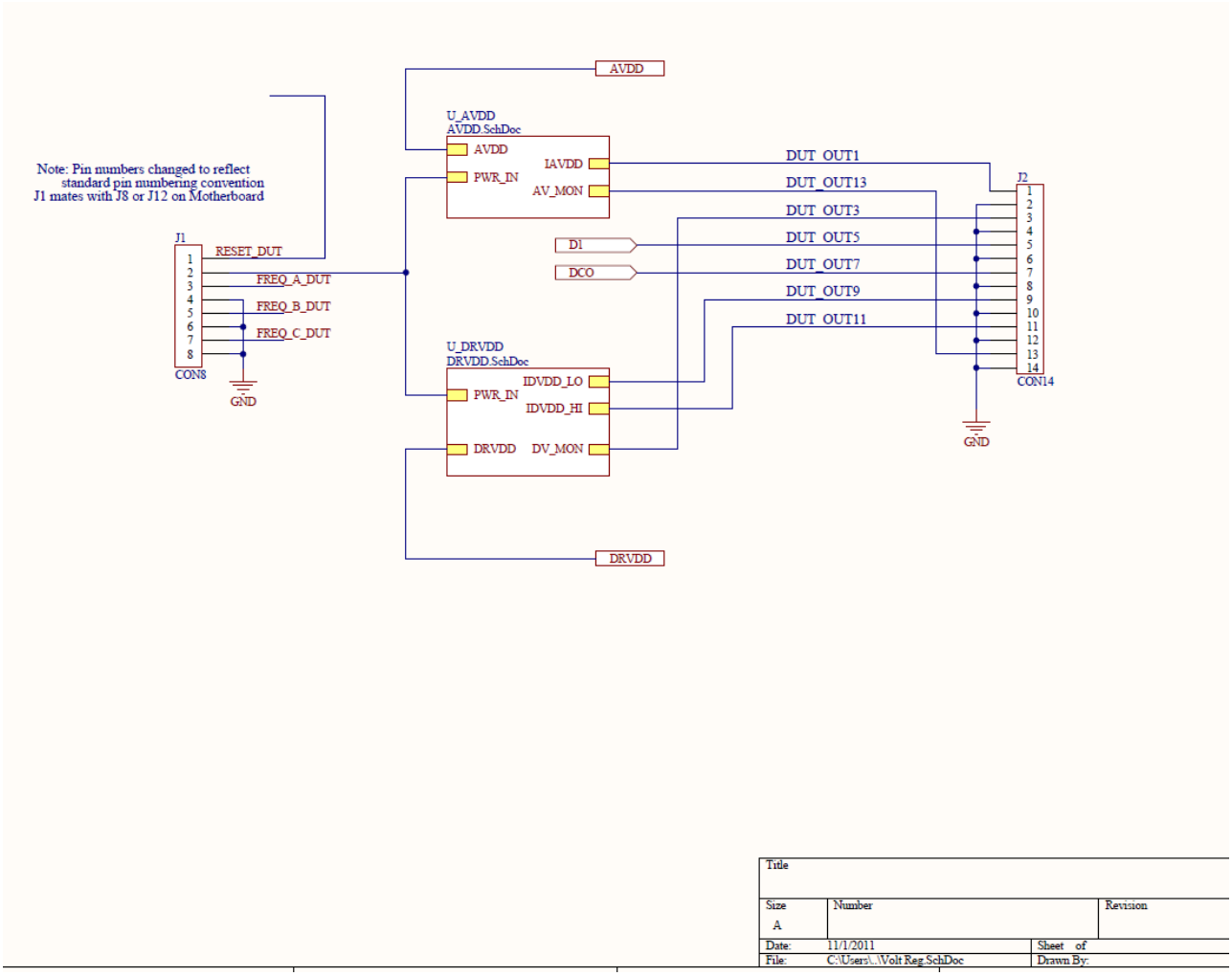

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Appendix C: Electrical Test Parameters and Equipment List:

The Analog Devices AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter described in this final report was irradiated using the 10MeV/n Xe beam at the Lawrence Berkeley National Laboratories with a split supply voltage of +3.6V / +1.9V and a case temperature of 85°C (±5°C). During the heavy ion exposure, the supply current to the unit-under-test was measured and recorded in approximately 1-second increments.

Table C.1 lists the equipment used during the testing as well as the calibration dates and the date the calibration is due.

Table C.1. Test equipment and calibration dates for testing the Analog Devices AD9254 14-Bit, 150 MSPS Analog-to-Digital Converter.

Equipment	**Serial Number**	**Calibration Date**	**Calibration Due**	**Purpose**
Instek SFG-2125	EF201999	N/A	N/A	Square Wave Input
HP 34401A Multimeter	3146A65284	5/15/11	5/15/12	Icc measurement
Agilent E3642A DC Power Supply	MY40004345	N/A	N/A	Test power supply-Positive Supply
Agilent E3631A DC Power Supply	K920920312	N/A	N/A	Test power supply-Negative Supply
Fluke Model 77 Multimeter	38301747	2/19/11	2/19/12	Vcc measurement at the DUT
Omega HH12 Handheld Thermometer	233126	2/19/12	2/19/12	Temperature Calibration
Tektronics TDS5104 Oscilloscope	B012544	10/22/11	10/22/12	Output Waveform Measurements, if applicable

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AD9254 Test Plan Summary for Berkeley (4/5/2012)

Test Type: *SEL*

DUT Temperature: *110˚C*

DUT Power: *AVDD +10% & DRVDD +10% (generated on DUT board from 7V Supply)*

LET: *Previously*

	Description	Comments
Test Type	SEL Characterization	
# of DUTs	3	
Ions	Xe, Kr, Ar	
LET	Find SEL Threshold	0 to 54˚ tilt
Motherboard	HC4000	Cypress I/O
+5V Supply	5.5V (nominal 28mA @ 125C)	Monitor current using 34401
+5V Current Limit	100mA	
DUT Temperature	125C	±5C
Fluence	10^7 ion/cm^2	
Recovery Sequence	Power Cycle +5V Supply	

Equipment Required:

Equipment Type	Description	Comments
Agilent 3631A	7V PWR_IN	
Agilent 34401A	PWR_IN Current Monitor	