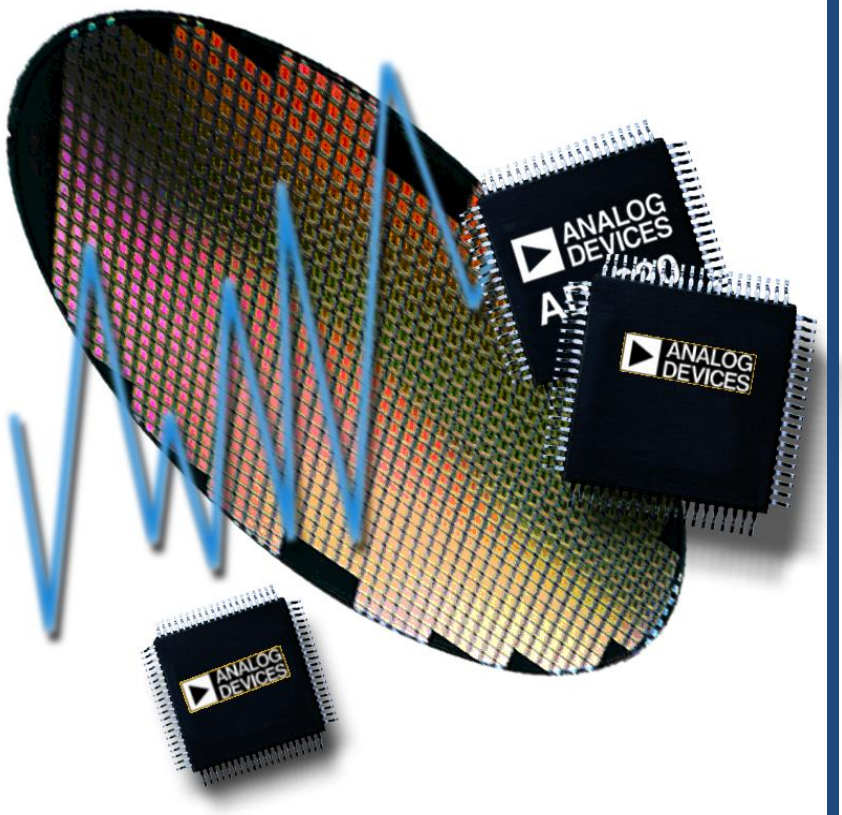

Reliability Report

Report Title: GaAs HBT-A Process Cumulative Reliability

Report Number: 2013-00228

Revision: 13

Date: 11 March 2024

Summary

This report summarizes the process qualification testing of the GaAs HBT-A process.

Table 1: Process Characteristics

Fabrication Details

Wafer Fabrication Process	GaAs HBT-A
Passivation Layer	SiN
Bond Pad Metal Composition	Au

Description / Results of Tests Performed

The following tables provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 2: Process Qualification Test Results

Test Name	Specification	Stress Tj (°C)	Biased Hours	Device	Lot #	Sample Size	Qty. Failures
High Temperature Operating Life (HTOL)	JESD22-A108	135	1000	HMC511	QTR2011-00013	159	0
		175	1000	HMC416	QTR2012-00198	24	0
		165	240	HMC361	QTR2012-00255	80	0
		165	1000	HMC361	QTR2012-00255	12	0
		150	1000	HMC8362	Q13356	82	0
		150	1000	ADMV8416	Q14625.HO1	82	0
		150	1000	ADMV8420	Q14647.HO1	82	0
		125	1000	ADH363S	Q14676.HO1	45	0
		148	1000	HMC8362	Q15090.11	82	0
		148	1000	HMC8362	Q17319.4	81	0

Test Name	Specification	Stress Tj (°C)	Biased Hours	Device	Lot #	Sample Size	Qty. Failures
		148	1000	HMC8362	Q17994.21	82	0
		148	1000	HMC8362	Q18642.10	81	0
		127	1000	HMC586	Q14546	221	0
		148	1000	HMC8362	Q19141.13	80	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

Approvals

Reliability Engineer: Tom Wood

Additional Information

Data sheets and other additional information are available on Analog Devices' web site

Appendix

GaAs HBT-A Failure Rate Estimate

The failure rate estimation was determined using the process HTOL test results and the parameters shown below:

- Die Use Junction Temperature, $T_{j\text{-}use}$ = 85°C
- Activation Energy = 1.1 eV
- Acceleration Factor (AF): $$AF = \exp\left[\left(\frac{E_A}{k}\right)\cdot\left(\left(\frac{1}{T_{USE}}\right)-\left(\frac{1}{T_{STRESS}}\right)\right)\right]$$
- Equivalent hours = Device hours x Acceleration Factor

Device	Qual Number	Equivalent Device Hours
HMC511	QTR2011-00013	$1.27x10^7$
HMC416	QTR2012-00198	$3.14x10^7$
HMC361	QTR2012-00255	$1.31x10^7$
HMC361	QTR2012-00255	$8.19x10^6$
HMC8362	Q13356	$1.99x10^7$
ADMV8416	Q14625.HO1	$1.99x10^7$
ADMV8420	Q14647.HO1	$1.99x10^7$
ADH363S	Q14676.HO1	$1.63x10^6$
HMC8362	Q15090.11	$1.72x10^7$
HMC8362	Q17319.4	$1.70x10^7$
HMC8362	Q17994.21	$1.72x10^7$
HMC8362	Q18642.10	$1.70x10^7$
HMC586	Q14546	$9.41x10^6$
HMC8362	Q19141.13	$1.68x10^7$
HMC8362	Q20258.13	$4.09x10^6$
Total Equivalent Device Hours =		$2.25x10^8$

The failure rate was calculated using Chi Square Statistic:

Since there were no failures and the tests were time terminated, F=0, and R = 2F+2 = 2

$\lambda_{CL} = \frac{\chi^2_{(\%CL,2F+2)} \cdot 10^9}{2 \cdot (Equiv.\ Device\ Hours)}$ at 60% and 90% Confidence Level (CL) and a die use junction temp, T_j = 85°C;

Failure Rate:

$\lambda_{60} = [(\chi^2)_{60,2}]/(2X\ \ 2.25x10^8\ \ )] = 1.8/\ 4.51x10^8 = \ 4.06x10^{-9}$ failures/hour or 4.1 FIT or MTTF = $2.46x10^8$ Hours

$\lambda_{90} = [(\chi^2)_{90,2}]/(2X\ \ 2.25x10^8\ \ )] = 4.6/\ 4.51x10^8 = \ 1.02x10^{-8}$ failures/hour or 10.2 FIT or MTTF = $9.78x10^7$ Hours