



ADV202 Errata [ADV202 Bug/Anomaly List]

This document presents all known bugs/anomalities and work arounds for the ADV202 second silicon ES2.

ADV202 parts to which this errata refers to are branded as follows:

ADV202xxx
xxxxxx
xxxx 0.1

1) Entropy codecs are not robust to bit errors in decode mode.

Issues: If the code stream contains bit errors, i.e. lost data or additional data, the IC will stop operation.

Workaround: Input correct code stream to the ADV202.

Fix: Fix will be implemented on ES3.

2) Line noise in HDTV decode mode.

Issues: This applies only to applications that use 2 or more ADV202s in sync mode, i.e aligning the video output of the VDATA buses, for the part that is set to decode slave mode. The error is visible on the slave device due to random lines that are delayed by one sample. In CbCr mode this results in color inversion only on those lines.
The delay between Hsync active edge on the input of the slave device and data output should always be 7clk cycles. This is not always the case with ES2 [and ES1] parts that are set to decode slave mode.

Workaround: Use a mux and a delay line to detect when the slave device's EAV/SAV code in the code stream is longer than 7 clkcycles and use the delay line to align both code streams at the output.
Note that the sometimes the anomaly does not occur at all.

Fix: Fix implemented on ES3.



- 3) Pixel activity on VDATA or HSYNC pins can cause hang-ups when the Host interface pins are used for pixel data.

Issues: ES2 parts become non-functional if an SAV code is present on the VDATA or the Hsync pin is pulsing while the Host interface [HDATA] is being used for pixel data.

Workaround: While the HDATA bus is used, the VDATA bus and the HSYNC pin must be idle by either a pull-up or pull-down.

Fix: Fix implemented on ES3.

- 4) Host FIFOs will reset to empty state when threshold registers are written to during operation.

Issues: Host FIFOs CODE, ATTR, ANC will reset to empty (i.e. empty contents of the FIFO) when the threshold registers FFTHRC, FFTHRA, FFTHRN are written to during operation. This does not apply to the PIXEL FIFO and the FFTHRP registers.

Workaround: If FIFO threshold settings are to be used, they should be programmed after power-up/ reset and should be left unchanged during operation.

Fix: Fix implemented on ES3.

- 5) Decode mode on HDATA bus for YYCbCr format.

Issues: Last transfer in the PIXEL FIFO is corrupted in decode mode when using the HDATA interface to output YYCbCr data in 8-bit or 16-bit format. This does not apply to Encode YYCbCr data on HDATA bus.

Workaround: Use YCbYCr packing mode for Decode.

Fix: Fix implemented on ES3.