PCN # 1581

DATE: October 27, 2015

EXPECTED PCN SHIP DATE: April 9, 2018

**Quality Assurance**
160 Rio Robles
San Jose, CA 95134

**www.maximintegrated.com**

# ☐ PROCESS CHANGE NOTICE
# ☒ PRODUCT CHANGE NOTICE

**MAXIM INTEGRATED** HEREBY ISSUES NOTIFICATION OF CHANGE THAT MAY AFFECT THE FOLLOWING CATEGORIES:

| | | | | |
|---|---|---|---|---|
| ☒ DESIGN | ☐ WAFER FAB | ☐ ASSEMBLY | ☐ TEST | ☒ ELEC/MECH SPECS |

AFFECTED PRODUCT:

Ordering P/N: (See PN listing XLS in PCN ZIP file)

| CHANGE FROM: Die Revision: APX6 | CHANGE TO: Die Revision: AUC2 |
|---|---|
| Datasheet changes: | Datasheet changes: |
| 1. Offset error: +/-13 LSB | 1. Offset error: +/-5.0 LSB (OVDD=/< 3.6V) , +/-8.0 LSB (OVDD > 3.6V) |
| 2. Gain Error: +/-12 LSB | 2. Gain Error: +/-8 LSB |
| 3. Integral Nonlinearity: +/-2 LSB | 3. Integral Nonlinearity: +/-1.5 LSB (OVDD =/< 3.6V) , +/-2.25 LSB (OVDD > 3.6V) |
| 4. Positive Full-Scale Error: +/-16 LSB | 4. Positive Full-Scale Error: +/-5.5 LSB (OVDD =/< 3.6V) , +/-7.5 LSB (OVDD > 3.6V) |
| 5. Negative Full-Scale Error: +/-16 LSB | 5. Negative Full-Scale Error: +/-7.5 LSB (OVDD =/< 3.6V) , +/-9.0 LSB (OVDD > 3.6V) |
| 6. SNR: 89.5dB (min) | 6. SNR: 89.7dB (min) |
| 7. SFDR: 96dB (min) | 7. SFDR: 99 dB (min) (OVDD =/< 3.6V) , 96 dB (min) (OVDD > 3.6V) |
| 8. THD: -96 dB (max) | 8. THD: -97.6 dB (max) (OVDD =/< 3.6V) , -95.5 dB (max) (OVDD > 3.6V) |
| 9. SCLK Period (CS Mode): 26ns (min) (VOVDD > 2.3V) | 9. SCLK Period (CS Mode): 25ns (min) (VOVDD > 2.3V) |
| 10. SCLK Period (Daisy-Chain Mode): 36ns (min)(VOVDD > 2.3V) | 10. SCLK Period (Daisy-Chain Mode): 30ns (min)(VOVDD > 2.3V) |
| 11. SCLK Low Time: 5 ns (min) | 11. SCLK Low Time: 6 ns (min) |
| 12. SCLK High Time: 5 ns (min) | 12. SCLK High Time: 6 ns (min) |
| 13. CNVST Low to SDO D15 MSB Valid (CS Mode), VOVDD , 2.7V: 17ns (max) | 13. CNVST Low to SDO D15 MSB Valid (CS Mode), VOVDD , 2.7V: 18ns (max) |
| 14. SCLK Valid Setup Time from CNVST Rising Edge: 5ns (min) | 14. SCLK Valid Setup Time from CNVST Rising Edge: 3ns (min) |
| 15. SCLK Valid Hold Time from CNVST Rising Edge: 5ns (min) | 15. SCLK Valid Hold Time from CNVST Rising Edge: 3ns (min) |
| 16. SDI Valid Setup Time from SCLK Falling Edge: 5ns (min) | 16. SDI Valid Setup Time from SCLK Falling Edge: VOVDD > 4.5V, 3ns(min); VOVDD > 2.7V, 5ns(min); VOVDD > 2.3V, 6ns(min) |
| 17. SDI High to SDO High, VOVDD > 4.5V, 15ns(max) | 17. SDI High to SDO High, VOVDD > 4.5V, 10ns(max) |
| 18. SDI High to SDO High, VOVDD > 2.3V, 26ns(max) | 18. SDI High to SDO High, VOVDD > 2.3V, 20ns(max) |

JUSTIFICATION: Minor design modification to the reference buffer to enhance select static and dynamic performance specifications, improve settling time, and increase manufacturing throughput.

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The datasheet is for the MAX11168 devices only.
Please see the attached datasheet for all changes and additional information to clarify the device operation.

TRACEABILITY: Maxim Integrated maintains full traceability by device marking, packaging labels and shipment documents.

Maxim Integrated's Change Notification System is designed to keep our customer base apprised of major product, manufacturing, or facility improvements.

Nasser Ali Chaouche

Nasser AliChaouche / PCN Coordinator

For further information, please contact either of the people listed below.

**Contact your local Maxim Integrated Company Representative** or Nasser AliChaouche, PCN Coordinator
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