

PROCESS CHANGE NOTICE
 PRODUCT CHANGE NOTICE
**MAXIM INTEGRATED HEREBY ISSUES NOTIFICATION OF CHANGE
 THAT MAY AFFECT THE FOLLOWING CATEGORIES:**

| | | | | |
|---------------------------------|------------------------------------|-----------------------------------|-------------------------------|---|
| <input type="checkbox"/> DESIGN | <input type="checkbox"/> WAFER FAB | <input type="checkbox"/> ASSEMBLY | <input type="checkbox"/> TEST | <input checked="" type="checkbox"/> ELEC/MECH SPECS |
|---------------------------------|------------------------------------|-----------------------------------|-------------------------------|---|

AFFECTED PRODUCT:

Ordering P/N: (See PN listing XLS in PCN ZIP file)

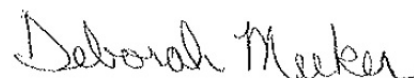
CHANGE FROM: VINL: max 0.8V

CHANGE TO: VINL: max 1V

JUSTIFICATION: CSb must be held high in polling mode. An npn transistor between CSb and the uC output pin can be used to pull up CSb to PVL if VIO is the pull-up supply and is switched off in polling mode. In this case, the logic low output from the uC is shifted by the Vbe of the npn transistor and, in consequence, it is helpful if the maximum VINL is changed from 0.8V to 1V. It is now easier for the customer to meet the VINL requirement.

TRACEABILITY: Maxim Integrated maintains full traceability by device marking, packaging labels and shipment documents.

Maxim Integrated's Change Notification System is designed to keep our customer base apprised of major product, manufacturing, or facility improvements.



Deborah Meeker / PCN Coordinator

For further information, please contact either of the people listed below.

Contact your local Maxim Integrated Company Representative

or

Deborah Meeker, PCN Coordinator

 408-601-5618 / pcn.coordinator@maximintegrated.com

Electrical Characteristics (continued)

($V_{BATT} = 14V$, $V_{IO} = 5V$, $T_A = T_J = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 2)

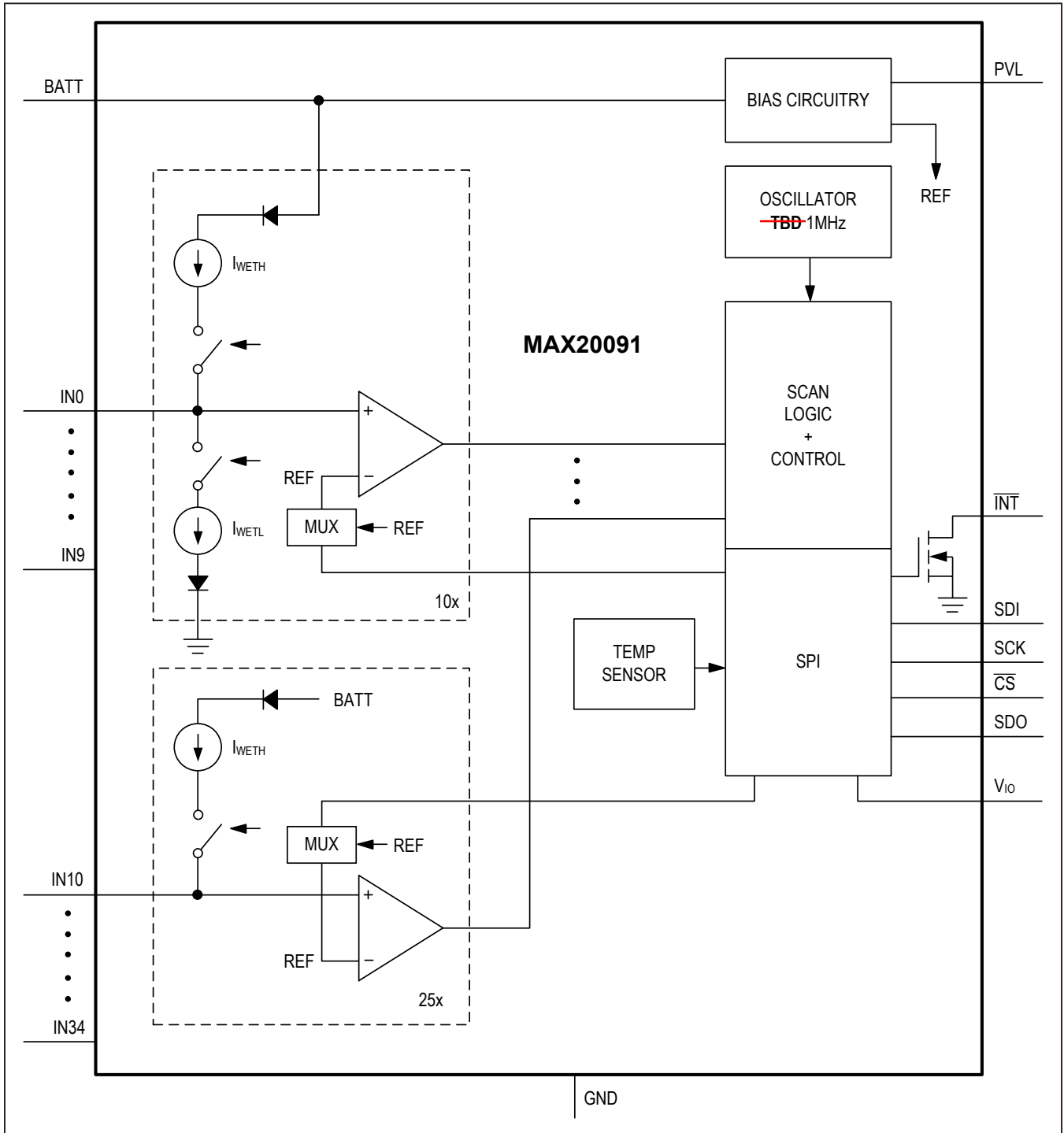
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|----------------|--|---------------------|-----|---------------------|------------|
| SWITCH INPUTS | | | | | | |
| Input Voltage Threshold (Open to Closed) | V_{THR} | $V_{BATT} = 7.5V$ to $28V$, SPI setting 00 | 3.7 | | 4.3 | V |
| | | $V_{BATT} = 7.5V$ to $28V$, SPI setting 01 | 3.5 | 3.8 | 4.1 | |
| | | $V_{BATT} = 7.5V$ to $28V$, SPI setting 10 | 2.75 | 3 | 3.25 | |
| | | $V_{BATT} = 7.5V$ to $28V$, SPI setting 11 | 1.8 | 2 | 2.2 | |
| Input Hysteresis | V_{HYST} | $V_{BATT} = 7.5V$ to $28V$ | | 0.2 | | V |
| Wetting Current Accuracy | I_{WETT} | 2mA setting, $5.5V < V_{BATT} < 28V$ | 1.7 | 2 | 2.3 | mA |
| IN0–IN34 Input Current | $I_{IN_}$ | $V_{BATT} = 14V$, wetting current set to zero, $T_A = +25^\circ C$ | -2 | 1 | +2 | μA |
| Dropout Voltage with GND-Connected Switch | $V_{DROPOUT}$ | $V_{BATT} - V_{IN_}$, wetting current at 90% of set value (90% of actual value when set to 10mA) | | | 2.9 | V |
| | | $V_{BATT} - V_{IN_}$, wetting current at 90% of set value (90% of actual value when set to of 2mA) | | | 1.5 | |
| Polling Active Time Accuracy | $t_{POLLACT}$ | | -10 | | +10 | % |
| Polling Time Accuracy | t_{POLL} | | -10 | | +10 | % |
| LOGIC LEVELS | | | | | | |
| \overline{INT} Output Voltage Low | V_{OUTL} | Sinking 2mA | | | 0.4 | V |
| SDO Output Voltage Low | V_{SDOL} | Sinking 2mA | | | $0.2 \times V_{IO}$ | V |
| SDO Output Voltage High | V_{SDOH} | Sourcing 1mA | $0.8 \times V_{IO}$ | | | V |
| SDO Leakage Current in High-Impedance Mode | I_{LKSDO} | $\overline{CS} = V_{IO}$ | -1 | | +1 | μA |
| SDI, CLK, CS Input Voltage Low | V_{INL} | | | | -0.8 1 | V |
| SDI, CLK, CS Input Voltage High | V_{INH} | | 2.2 | | | V |
| \overline{INT} Output Leakage Current | | | -5 | | +5 | μA |
| SDI Internal Pulldown Resistor | R_{SDI} | | | 50 | | k Ω |
| THERMAL PROTECTION | | | | | | |
| Thermal Warning | T_{WARN} | \overline{INT} asserted low and T bit set in SPI word | | 145 | | $^\circ C$ |
| Thermal Shutdown | T_{SHDN} | | | 165 | | $^\circ C$ |
| Thermal-Shutdown Hysteresis | $T_{SHDN.HYS}$ | | | 15 | | $^\circ C$ |

Pin Description

| PIN | NAME | FUNCTION |
|--------|------------------|--|
| 1, 2 | IN8, IN9 | Switch Monitor Input Channels 8 and 9. Connect to a battery-connected or ground-connected switch. When used for a battery-connected switch, add a 100Ω series protection resistor to the input. |
| 3–27 | IN10, IN34 | Switch Monitor Input Channels 10–34. Connect to a ground-connected switch. |
| 28 | GND | Ground Connection |
| 29 | V _{IO} | Logic Supply for SPI Interface Pins. Connect to a supply between 3V and 5V. Bypass VIO to GND with a 0.1μF capacitor placed as close to VIO as possible. |
| 30 | SDO | SPI Data Output. SDO is high impedance when \overline{CS} is high. |
| 31 | \overline{CS} | SPI Active-Low Chip-Select. Drive \overline{CS} low to enable clocking of data into and out of the IC. SPI data is latched into the device on the rising edge of \overline{CS} . |
| 32 | SCK | SPI Clock Input |
| 33 | SDI | SPI Data Input. SPI data is latched into the internal shift register on the rising edges of SCK while CS is held low. SDI has an internal 75kΩ pulldown resistor. Connect SDI to the SDO of a preceding device in a daisy chain or to the microcontroller data output. |
| 34 | \overline{INT} | Open-Drain Interrupt Output. \overline{INT} goes low when an input switch change has been detected in scan mode. |
| 35, 36 | PVL | Internal Linear Regulator Output. PVL is the supply for the internal blocks. Bypass PVL with a 2.2μF capacitor to ground. |
| 37–39 | GND | Ground |
| 40 | BATT | Battery Voltage Connection. BATT should be protected from reverse battery using a series diode. Bypass BATT to GND with a 0.1μF ceramic capacitor placed as close as possible to the pin. In addition, bypass BATT with a 47μF or greater capacitor. |
| 41–48 | IN0–IN7 | Switch Monitor Input Channels 0–7. Connect to a battery-connected or ground-connected switch. When used for a battery-connected switch, add a 100Ω series protection resistor to the input. |
| — | EP | Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use as the only IC ground connection. EP must be connected to GND. |

In polling mode CS must be maintained high in order to ensure correct operation of the INT output. If needed the PVL output can be used as the pullup power.

Functional Diagram



Detailed Description

The MAX20091 is a 35-channel automotive contact monitor designed as an interface between mechanical switches and low-voltage microcontrollers or other logic circuits. It features an SPI interface to monitor individual switch inputs and to configure interrupt capability, wetting current, switch configuration (battery-connected or ground-connected), polling time, and polling active time. Any switch status change causes an interrupt signal if the switch is interrupt enabled. The IC has two modes of operation: continuous mode and polling mode.

BATT and V_{IO}

V_{IO} is the power-supply input for the logic output circuitry. Connect V_{IO} to a 3V to 5.5V logic-level supply. Bypass V_{IO} to GND with at least a 0.1μF capacitor placed as close as possible to the V_{IO} pin.

BATT is the main power-supply input. Bypass BATT to GND with a 0.1μF ceramic capacitor placed as close as possible to the pin. In addition, bypass BATT with a 47μF or greater capacitor. When BATT exceeds 28V (typ) wetting current is disabled, switch scanning is stopped and the OVP bit in SPI register 0x04 is set.

PVL is the output of an internal ultra-low current regulator that is always enabled when BATT is above its undervoltage lockout. Bypass PVL with a 2.2μF capacitor.

Operating Modes

The IC features two modes of operation: continuous mode and polling mode. In continuous mode, the wetting currents (if enabled) are continuously applied to closed switches. In polling mode, the wetting currents are applied to the closed switches for a preset duration to reduce the power consumption.

Continuous Mode Operation (P2:P0 = 0)

In continuous mode, reading of the switch status is initiated by a falling edge on \overline{CS} . The microcontroller initiates a low pulse on \overline{CS} to update the IC's switch status register. If \overline{INT} remains high, no action needs be taken by the microcontroller. If \overline{INT} goes low, the microcontroller may perform a read operation to read the updated switch status. On the rising edge of \overline{CS} , \overline{INT} is updated. To get correct data, the microcontroller must wait at least 4μs before initiating a switch status read operation.

Polling-Mode Operation

In polling mode, each switch input is sampled for a programmable polling active time set by the PA[2:0] bits between 96μs and 4ms (see [Table 5](#)). Sampling

is repeated at a period set by the P[3:0] bits (from 8ms to continuous, see [Table 4](#)). All switch inputs are sampled simultaneously at the end of the polling active time. Wetting currents (if enabled) are applied to closed switches during the polling active time. Polling mode thus reduces the current consumption from the BATT power supply to a value dependent on the polling time and polling active time chosen.

Mechanical Switch Inputs (IN0–IN34)

IN0–IN34 are the inputs for remote mechanical switches. The switch status is indicated by the SS[34:0] bits in the switch status registers, and each switch input can be programmed to assert an interrupt (\overline{INT}) by writing to the IE[34:0] bits in registers 0x07 to 0x0B. All switch inputs are interrupt-disabled upon power-up.

The IN10–IN34 inputs are intended for ground-connected switches. The IN0–IN9 inputs can be programmed for either ground-connected switches or battery-connected switches by writing to the LH[9:0] bits in registers 0x05 and 0x06. The default configuration of the IN0–IN9 inputs after power-up is for ground-connected switches. All inputs have an internal glitch filter with a typical filter time of 50μs.

Wetting Current

The IC applies a programmable wetting current to any closed switch to clean switch contacts that are exposed to adverse conditions. The wetting current for each switch can be set to 0mA, 2mA, 5mA, or 10mA by the W__[1:0] data bits in the wetting current registers by means of SPI.

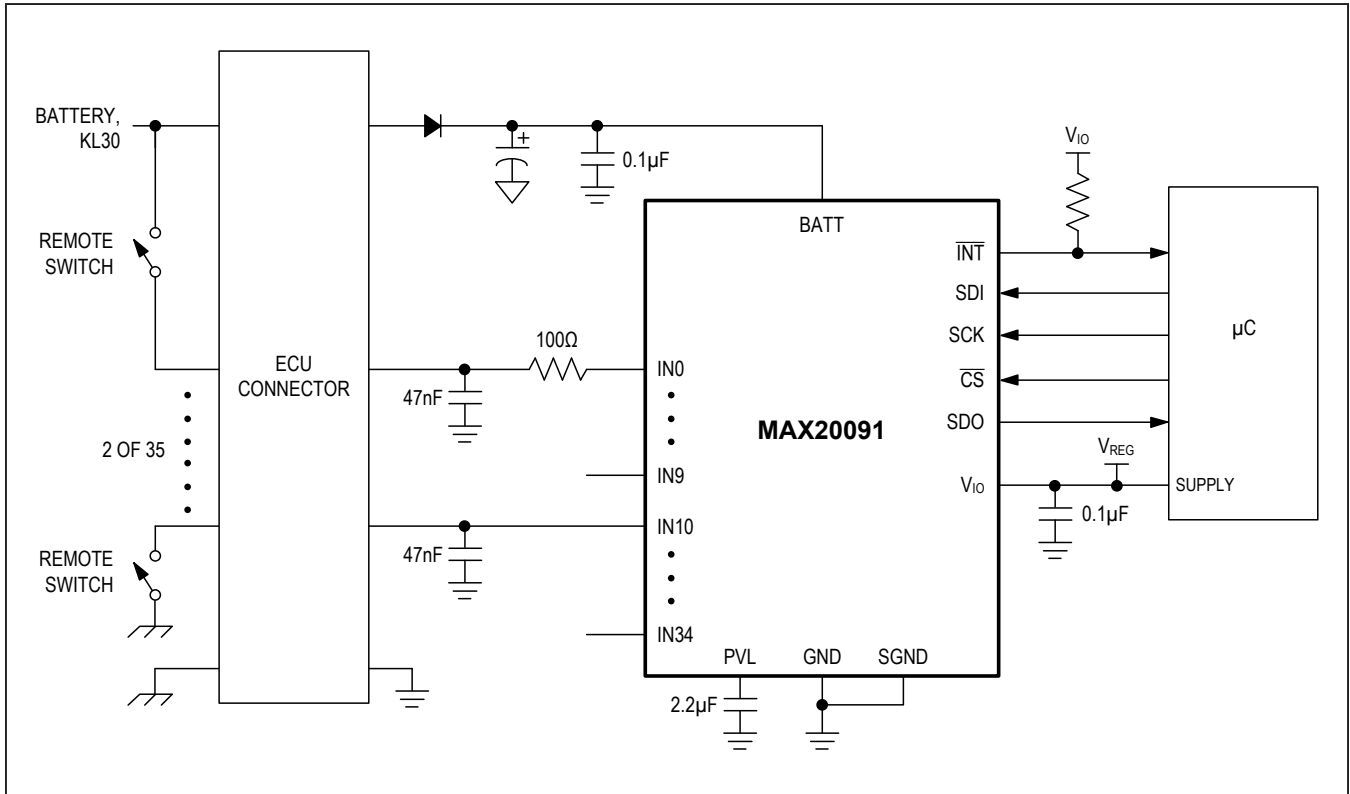
When using wetting current, special care must be taken to avoid exceeding the maximum power dissipation of the IC (see the [Applications Information](#) section). Disabling the wetting current or limiting the active-wetting current time reduces power consumption. The default state upon power-up is with wetting current set to 2mA.

Interrupt Output (\overline{INT})

\overline{INT} is an active-low, open-drain output that asserts low when any of the switch inputs change state and is enabled for interrupts, or when the overtemperature warning threshold is exceeded. An external pullup resistor to V_{IO} is needed on \overline{INT} . \overline{INT} is cleared when \overline{CS} is driven low for a read/write operation. However, in polling mode, any switch state change or overtemperature change that occurs during an SPI transaction is stored and causes an additional interrupt after the SPI transaction is over and \overline{CS} goes high. If V_{IO} is absent, the \overline{INT} output is functional provided that it is pulled up to a different supply voltage.

and that CS is kept high.

Typical Operating Circuit



Ordering Information/Selector Guide

| PART | TEMP RANGE | PIN-PACKAGE | PKG CODE |
|-----------------|-----------------|-------------|-----------|
| MAX20091ATM/V+T | -40°C to +125°C | 48 TQFN | T 4877+6C |

N denotes an automotive qualified part.
 +Denotes a lead(Pb)-free/RoHS-compliant package.
 T = Tape and reel.
 *EP = Exposed pad.

Chip Information

PROCESS: BICMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------------------|-------------------------|
| 48 TQFN-EP | T4877+6C | 21-0144 | 90-0132 |