Product/Process Change Notice - PCN 14_0163 Rev. A

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This notice is to inform you of a change that will be made to certain ADI products (see Material Report). Any issues with this PCN or requirements to qualify the change (additional data or samples) must be sent to ADI within 30 days of publication date. ADI contact information is listed below.

Note: Revised fields are indicated by a red field name. See Appendix B for revision history.

PCN Title: Data Sheet & Silicon Anomaly Sheet updates for ADuC7023, ADuC7121/2/4/6, ADuC7060/61, ADuCM360/1, ADuCM350, ADuCM320 product

Publication Date: 16-Jul-2014

Effectivity Date: 16-Jul-2014 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:

Add ADuCM320 to the list of data sheets being updated

Description Of Change

The datasheet for the parts listed in this PCN are being updated to remove the clock stretching functionality and the corresponding anomaly sheets are being updated to explain two I2C issues.

There is no change to the actual silicon.

Reason For Change

The two I2C issues are:

1. Enabling I2C clock stretching on the rising edge of SCL may cause a glitch which could be interpreted by other devices on the bus as a real clock.

Clock stretching is enabled by setting bit 6 of I2CSCON for a slave and bit 3 of I2CMCON for a master. The hardware enables clock stretching after the bit is set, when SCL is LOW. The hardware uses delayed version of SCL. The delay is 6 x UCLK (system clock) periods. If software enables clock stretching on the rising edge of SCL, the hardware observes SCL as still being LOW and activates clock stretching thus causing a glitch.

Customers should not use the clock stretching feature on the parts listed in the PCN or if they need to they have to ensure that they do not enable it on the rising edge of SCL

2. If a byte with the MSB equal to '0' is loaded into the slave TX FIFO just after the 9th rising edge of SCL the I2C slave will pull the SDA pin low and hold it indefinitely.

The 9th SCL clock is where the ACK/NACK bit is transmitted. If the I2C slave has no data to transmit it will allow the SDA line to be pulled HIGH – this is a NACK. If the slave has data to transmit it will pull the line LOW – this is an ACK. In the case of the slave TX FIFO being loaded on the rising edge of the 9th clock, the slave will pull the SDA line LOW too late. The master will interpret this as a NACK and will not generate any more clocks on the SCL. The slave will pull the SDA line LOW because it is attempting to load the MSB of the TX FIFO and the line will not be released because there are no more clocks generated by the master.

The workaround is to ensure that the slave TX FIFO is loaded before the rising edge of the 9th clock. The TX FIFO can be preloaded in advance or during the preceding RX interrupt.

Other workarounds include resetting the entire chip or generating more clocks so that the slave will empty its FIFO and release the bus.

Impact of the change (positive or negative) on fit, form, function & reliability

The data sheets and anomaly sheets are being updated to accurately reflect the devices' functionality

Summary of Supporting Information

The following documentation will include the information above:
ADuC7023: Data Sheet Rev. G, Silicon Anomaly Sheet Rev. C
ADuC7060/ADuC7061: Data Sheet Rev. E, Silicon Anomaly Sheet Rev. B
ADuC7121: Data Sheet Rev. C, Silicon Anomaly Sheet Rev. A
ADuC7122: Data Sheet Rev. A, Silicon Anomaly Sheet Rev. A
ADuC7124/ADuC7126: Data Sheet Rev. D, Silicon Anomaly Rev. B
ADuCM360/ADuCM361: Hardware User Guide Rev. D, Silicon Anomaly Rev. A
ADuCM350: Hardware Reference Manual Rev. B
ADuCM320: Hardware Reference Manual Rev. A

Supporting Documents None

For questions on this PCN, send email to the regional contacts below or contact your local ADI sales representative					
Americas:	PCN_Americas@analog.com	**Europe:**	PCN_Europe@analog.com	**Japan:**	PCN_Japan@analog.com
				Rest of Asia:	PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Existing Parts - Product Family / Model Number (31)				
ADUC7023 / ADUC7023BCBZ62I-R7	ADUC7023 / ADUC7023BCP6Z62I	ADUC7023 / ADUC7023BCP6Z62IR7	ADUC7023 / ADUC7023BCP6Z62IRL	ADUC7023 / ADUC7023BCPZ62I
ADUC7023 / ADUC7023BCPZ62I-R7	ADUC7023 / ADUC7023BCPZ62I-RL	ADUC7023 / ADUC7023FNS-DIE	ADUC7060 / ADUC7060BCPZ32	ADUC7060 / ADUC7060BCPZ32-RL
ADUC7060 / ADUC7060BSTZ32	ADUC7060 / ADUC7060BSTZ32-RL	ADUC7061 / ADUC7061BCPZ32	ADUC7061 / ADUC7061BCPZ32-RL	ADUC7121 / ADUC7121BBCZ
ADUC7121 / ADUC7121BBCZ-RL	ADUC7122 / ADUC7122BBCZ	ADUC7122 / ADUC7122BBCZ-RL	ADUC7124 / ADUC7124BCPZ126	ADUC7124 / ADUC7124BCPZ126-RL
ADUC7126 / ADUC7126BSTZ126	ADUC7126 / ADUC7126BSTZ126-RL	ADUC7126 / ADUC7126BSTZ126I	ADUC7126 / ADUC7126BSTZ126IRL	ADUCM350 / AD80/001Z-0RL
ADUCM350 / ADUCM350BBCZ	ADUCM350 / ADUCM350BBCZ-RL	ADUCM360 / ADUCM360BCPZ128	ADUCM360 / ADUCM360BCPZ128-R7	ADUCM361 / ADUCM361BCPZ128
ADUCM361 / ADUCM361BCPZ128-R7				

Added Parts On This Revision - Product Family / Model Number (2)				
ADUCM320 / ADUCM320BBCZ	ADUCM320 / ADUCM320BBCZ-RL			

Appendix B - Revision History			
Rev	**Publish Date**	**Effectivity Date**	**Rev Description**
Rev. -	07-Jul-2014	07-Jul-2014	Initial Release
Rev. A	16-Jul-2014	16-Jul-2014	Add ADuCM320 to the list of data sheets being updated