Table 1. Summary of Perfomance Specification Changes

Parameter	Current Value	New Value	Unit	Test Conditions/Comments
ACCURACY				
Gain Error	±0.024	±0.05	% FSR max	At 25°C
	±0.024	±0.06	% FSR max	T_{MIN} to T_{MAX}
DC Crosstalk	0.5	1	LSB max	
REFERENCE INPUT/OUTPUT				
Output Impedance	2200	800	Ω typ	
OUTPUT CHARACTERISTICS				
DC Output Impedance	0.5	0.6	Ω max	
MONITOR PIN				
Output Impedance	0.5	1	kΩ typ	
LOGIC INPUTS (EXCEPT SDA/SCL)				DV_{DD} = 2.7 V to 5.5 V
V_{IL}, Input Low Voltage				
DVDD > 3.6 V	0.8	0.8	V max	
DVDD ≤ 3.6 V	0.8	0.6	V max	
POWER REQUIREMENTS				
AI_{DD} (Power-Down)	2	20	µA max	Typically 100 nA
DI_{DD} (Power-Down)	20	20	µA max	Typically 1 µA

Table 2. Summary of Changes to AC Characterisitcs

Parameter	Current Value	New Value	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Settling Tim	8	3	µs typ	Boost mode off, CR11 = 0
	10	8	µs max	Boost mode off, CR11 = 0
Slew Rate	2	1.5	V/µs typ	Boost mode off, CR11 = 0
	3	2.5	V/µs typ	Boost mode on, CR11 = 1

Table 3. Summary of SPI Timing Specification Changes

	Limit at T_{MIN}, T_{MAX}			
Parameter	Current Value	New Value	Unit	Description
t_{7A}	50	140	ns min	Minimum $\overline{SYNC}$ high time in readback mode
t_{10}	30	36	ns max	24th SCLK falling edge to $\overline{BUSY}$ falling edge
t_{14}	100	100/2000	ns min/max	$\overline{BUSY}$ rising edge to DAC output response time
t_{17}	8	3	µs typ	DAC output settling time boost mode off
t_{19}	12	40	µs max	$\overline{CLR}$ pulse activation time
t_{20}	20	30	ns max	SCLK rising edge to SDO valid