Single Channel, 12-/16-Bit, Serial Input, Current Source and Voltage Output DACs

AD5412/AD5422

FEATURES

- 12-/16-bit resolution and monotonicity
- Current output ranges: 4 mA to 20 mA, 0 mA to 20 mA, 0 mA to 24 mA
  - ±0.01 % FSR typical total unadjusted error (TUE)
  - ±3 ppm/°C output drift
- Voltage output ranges: 0 V to 5 V, 0 V to 10 V, ±5 V, ±10 V
  - 10% overrange
  - ±0.01 % FSR typical total unadjusted error (TUE)
  - ±2 ppm/°C output drift
- Flexible serial digital interface
- On-chip output fault detection
- On-chip reference: 10 ppm/°C maximum
- Asynchronous clear function
- Power supply range
  - AV_{DD}: 10.8 V to 40 V
  - AV_{SS}: −26.4 V to −3 V/0 V
- Output loop compliance: AV_{DD} – 2.5 V
- Temperature range: −40°C to +85°C
- TSSOP and LFCSP packages

APPLICATIONS

- Process control
- Actuator control
- PLC

GENERAL DESCRIPTION

The AD5412/AD5422 are low-cost, precision, fully integrated 12-/16-bit digital-to-analog converters (DAC) offering a programmable current source and programmable voltage output designed to meet the requirements of industrial process control applications.

The output current range is programmable at 4 mA to 20 mA, 0 mA to 20 mA, or an overrange function of 0 mA to 24 mA.

Voltage output is provided from a separate pin that can be configured to provide 0 V to 5 V, 0 V to 10 V, ±5 V, or ±10 V output ranges; an overrange of 10% is available on all ranges.

Analog outputs are short and open-circuit protected and can drive capacitive loads of 1 µF.

The device operates with an AV_{DD} power supply range from 10.8 V to 40 V. Output loop compliance is 0 V to AV_{DD} – 2.5 V.

The flexible serial interface is SPI- and MICROWIRE™-compatible and can be operated in 3-wire mode to minimize the digital isolation required in isolated applications.

The device also includes a power-on-reset function, ensuring that the device powers up in a known state. The part also includes an asynchronous clear pin (CLEAR) that sets the outputs to zero-scale/midscale voltage output or the low end of the selected current range.

The total output error is typically ±0.01% in current mode and ±0.01% in voltage mode.

Table 1. Pin-Compatible Devices

Part Number	Description
AD5410	Single channel, 12-bit, serial input current source DAC
AD5420	Single channel, 16-bit, serial input current source DAC

Rev. C

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FUNCTIONAL BLOCK DIAGRAM

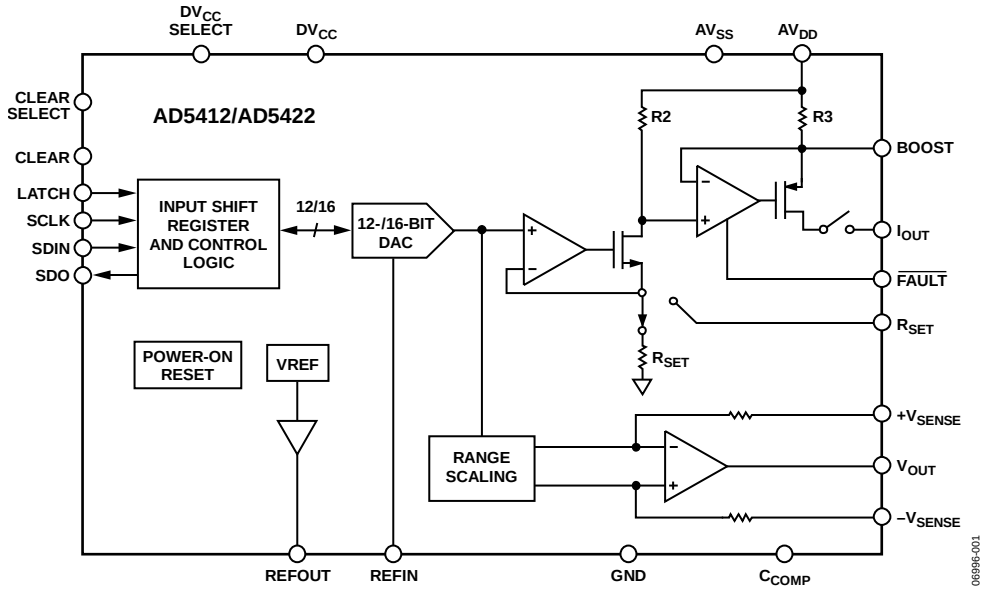


Figure 1.

SPECIFICATIONS

AV_{DD} = 10.8 V to 26.4 V, AV_{SS} = −26.4 V to −3 V/0 V, AV_{DD} + |AV_{SS}| < 52.8 V, GND = 0 V, REFIN = 5 V external; DV_{CC} = 2.7 V to 5.5 V. V_{OUT}: R_{LOAD} = 1 kΩ, C_L = 200 pF, I_{OUT}: R_{LOAD} = 350 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE OUTPUT					
Output Voltage Ranges	0		5	V	
	0		10	V	
	−5		+5	V	
	−10		+10	V	
Accuracy					Output unloaded
Resolution	16			Bits	AD5422
	12			Bits	AD5412
Total Unadjusted Error (TUE)					
B Version	−0.1		+0.1	% FSR	
	−0.05	±0.01	+0.05	% FSR	T_A = 25°C
A Version	−0.3		+0.3	% FSR	
	−0.1	±0.05	+0.1	% FSR	T_A = 25°C
Relative Accuracy (INL)[2]	−0.008		+0.008	% FSR	AD5422
	−0.032		+0.032	% FSR	AD5412
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Bipolar Zero Error	−6		+6	mV	Bipolar output range
	−1.5	±0.2	+1.5	mV	T_A = 25°C, bipolar output range
Bipolar Zero Error Temperature Coefficient (TC)[3]		±3		ppm FSR/°C	Bipolar output range
Zero-Scale Error	−5		+5	mV	
	−3.5	±0.3	+3.5	mV	T_A = 25°C
Zero-Scale Error Temperature Coefficient (TC)[3]		±2		ppm FSR/°C	
Offset Error	−4		+4	mV	Unipolar output range
	−1.5	±0.2	+1.5	mV	T_A = 25°C, unipolar output range
Offset Error Temperature Coefficient (TC)[3]		±2		ppm FSR/°C	Unipolar output range
Gain Error	−0.07		+0.07	% FSR	
	−0.05	±0.004	+0.05	% FSR	T_A = 25°C
Gain Error Temperature Coefficient (TC)[3]		±1		ppm FSR/°C	
Full-Scale Error	−0.07		+0.07	% FSR	
	−0.05	±0.001	+0.05	% FSR	T_A = 25°C
Full-Scale Error Temperature Coefficient (TC)[3]		±1		ppm FSR/°C	
OUTPUT CHARACTERISTICS[3]					
Headroom		0.5	0.8	V	Output unloaded
Output Voltage Drift vs. Time		90		ppm FSR	Drift after 1000 hours, T_A = 125°C
Short-Circuit Current		20		mA	
Load	1			kΩ	
Capacitive Load Stability					T_A = 25°C
R_{LOAD} = ∞			20	nF	
R_{LOAD} = 1 kΩ			5	nF	
R_{LOAD} = ∞			1	µF	External compensation capacitor of 4 nF connected
DC Output Impedance		0.3		Ω	
Power-On Time		10		µs	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DC PSRR		90	130	µV/V	
		3	12	µV/V	Output unloaded
CURRENT OUTPUT					
Output Current Ranges	0		24	mA	
	0		20	mA	
	4		20	mA	
Accuracy (Internal R_{SET})					
Resolution	16			Bits	AD5422
	12			Bits	AD5412
Total Unadjusted Error (TUE)					
B Version	−0.3		+0.3	% FSR	
	−0.13	±0.08	+0.13	% FSR	T_A = 25°C
A Version	−0.5		+0.5	% FSR	
	−0.3	±0.15	+0.3	% FSR	T_A = 25°C
Relative Accuracy (INL)[4]	−0.024		+0.024	% FSR	AD5422
	−0.032		+0.032	% FSR	AD5412
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error	−0.27		+0.27	% FSR	
	−0.12	±0.08	+0.12	% FSR	T_A = 25°C
Offset Error Temperature Coefficient (TC)[3]		±16		ppm FSR/°C	
Gain Error	−0.18		+0.18	% FSR	AD5422
	−0.03	±0.006	+0.03	% FSR	AD5422, T_A = 25°C
	−0.22		+0.22	% FSR	AD5412
	−0.06	±0.006	+0.06	% FSR	AD5412, T_A = 25°C
Gain Temperature Coefficient (TC)[3]		±10		ppm FSR/°C	
Full-Scale Error	−0.2		+0.2	% FSR	
	−0.1	±0.08	+0.1	% FSR	T_A = 25°C
Full-Scale Temperature Coefficient (TC)[3]		±6		ppm FSR/°C	
Accuracy (External R_{SET})					
Resolution	16			Bits	AD5422
	12			Bits	AD5412
Total Unadjusted Error (TUE)					
B Version	−0.15		+0.15	% FSR	
	−0.06	±0.01	+0.06	% FSR	T_A = 25°C
A Version	−0.3		+0.3	% FSR	
	−0.1	±0.02	+0.1	% FSR	T_A = 25°C
Relative Accuracy (INL)[4]	−0.012		+0.012	% FSR	AD5422
	−0.032		+0.032	% FSR	AD5412
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error	−0.1		+0.1	% FSR	
	−0.03	±0.006	+0.03		T_A = 25°C
Offset Error Temperature Coefficient (TC)[3]		±3		µA/°C	
Gain Error	−0.08		+0.08	% FSR	
	−0.05	±0.003	+0.05	% FSR	T_A = 25°C
Gain Temperature Coefficient (TC)[3]		±4		ppm FSR/°C	
Full-Scale Error	−0.15		+0.15	% FSR	
	−0.06	±0.01	+0.06	% FSR	T_A = 25°C
Full-Scale Temperature Coefficient (TC)[3]		±7		ppm FSR/°C	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS[3]					
Current Loop Compliance Voltage	0		AV_{DD} − 2.5	V	
Output Current Drift vs. Time					Drift after 1000 hours, T_A = 125°C
		50		ppm FSR	Internal R_{SET}
		20		ppm FSR	External R_{SET}
Resistive Load			1200	Ω	
Inductive Load		50		mH	T_A = 25 °C
DC PSRR			1	µA/V	
Output Impedance		50		MΩ	
Output Current Leakage When Output Is Disabled		60		pA	
REFERENCE INPUT/OUTPUT					
Reference Input[3]					
Reference Input Voltage	4.95	5	5.05	V	For specified performance
DC Input Impedance	27	40		kΩ	
Reference Output					
Output Voltage	4.995	5	5.005		T_A = 25°C
Reference Temperature Coefficient (TC)[3, 5]		1.8	10	ppm/°C	
Output Noise (0.1 Hz to 10 Hz)[3]		10		µV p-p	
Noise Spectral Density[3]		100		nV/√Hz	At 10 kHz
Output Voltage Drift vs. Time[3]		50		ppm	Drift after 1000 hours, T_A = 125°C
Capacitive Load[3]		600		nF	
Load Current[3]		5		mA	
Short-Circuit Current[3]		7		mA	
Load Regulation[3]		95		ppm/mA	
DIGITAL INPUTS[3]					JEDEC compliant
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Current	−1		+1	µA	Per pin
Pin Capacitance		10		pF	Per pin
DIGITAL OUTPUTS[3]					
SDO					
Output Low Voltage, V_{OL}			0.4	V	Sinking 200 µA
Output High Voltage, V_{OH}	DV_{CC} − 0.5			V	Sourcing 200 µA
High Impedance Leakage Current	−1		+1	µA	
High Impedance Output Capacitance		5		pF	
$\overline{FAULT}$					
Output Low Voltage, V_{OL}			0.4	V	10 kΩ pull-up resistor to DV_{CC}
Output Low Voltage, V_{OL}		0.6		V	At 2.5 mA
Output High Voltage, V_{OH}	3.6			V	10 kΩ pull-up resistor to DV_{CC}
POWER REQUIREMENTS					
AV_{DD}	10.8		40	V	
AV_{SS}	−26.4		0	V	
$\|AV_{SS}\| + AV_{DD}$	10.8		52.8	V	
DV_{CC}					
Input Voltage	2.7		5.5	V	Internal supply disabled
Output Voltage		4.5		V	DV_{CC}, which can be overdriven up to 5.5 V
Output Load Current[3]		5		mA	
Short-Circuit Current[3]		20		mA	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
AI_{DD}					Outputs unloaded
		2.5	3	mA	Outputs disabled
		3.4	4	mA	Current output enabled
		3.9	4.4	mA	Voltage output enabled
AI_{SS}					Outputs unloaded
		0.24	0.3	mA	Outputs disabled
		0.5	0.6	mA	Current output enabled
		1.1	1.4	mA	Voltage output enabled
DI_{CC}			1	mA	$V_{IH} = DV_{CC}$, V_{IL} = GND
Power Dissipation		128		mW	AV_{DD} = 40 V, AV_{SS} = 0 V, outputs unloaded
		120		mW	AV_{DD} = +24 V, AV_{SS} = −24 V, outputs unloaded

[1] Temperature range: −40°C to +85°C; typical at +25°C.
[2] When the AD5412/AD5422 is powered with AV_{SS} = 0 V, INL for the 0 V to 5 V and 0 V to 10 V ranges is measured beginning from Code 256 for the AD5422 and Code 16 for the AD5412.
[3] Guaranteed by design and characterization; not production tested.
[4] For 0 mA to 20 mA and 0 mA to 24 mA ranges, INL is measured beginning from Code 256 for the AD5422 and Code 16 for the AD5412.
[5] The on-chip reference is production trimmed and tested at 25°C and 85°C. It is characterized from −40°C to +85°C.

AC PERFORMANCE CHARACTERISTICS

AV_{DD} = 10.8 V to 26.4 V, AV_{SS} = −26.4 V to −3 V/0 V, $AV_{DD} + |AV_{SS}| < 52.8$ V, GND = 0 V, REFIN = +5 V external; DV_{CC} = 2.7 V to 5.5 V. V_{OUT}: R_{LOAD} = 1 kΩ, C_L = 200 pF, I_{OUT}: R_{LOAD} = 350 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Voltage Output					
Output Voltage Settling Time			25	µs	10 V step to ±0.03 % FSR
		32		µs	20 V step to ±0.03 % FSR
			18	µs	5 V step to ±0.03 % FSR
		8		µs	512 LSB step to ±0.03 % FSR (16-Bit LSB)
Slew Rate		0.8		V/µs	
Power-On Glitch Energy		10		nV-sec	
Digital-to-Analog Glitch Energy		10		nV-sec	
Glitch Impulse Peak Amplitude		20		mV	
Digital Feedthrough		1		nV-sec	
Output Noise (0.1 Hz to 10 Hz Bandwidth)		0.1		LSB p-p	16-bit LSB
Output Noise (100 kHz Bandwidth)		200		µV rms	
1/f Corner Frequency		1		kHz	
Output Noise Spectral Density		150		nV/√Hz	Measured at 10 kHz, midscale output, 10 V range
AC PSRR		−75		dB	200 mV 50 Hz/60 Hz sine wave superimposed on power supply voltage
Current Output					
Output Current Settling Time		10		µs	16 mA step to 0.1% FSR
		40		µs	16 mA step to 0.1% FSR, L = 1 mH
AC PSRR		−75		dB	200 mV 50 Hz/60 Hz sine wave superimposed on power supply voltage

[1] Guaranteed by characterization, not production tested.

TIMING CHARACTERISTICS

AV_{DD} = 10.8 V to 26.4 V, AV_{SS} = −26.4 V to −3 V/0 V, AV_{DD} + |AV_{SS}| < 52.8V, GND = 0 V, REFIN = +5 V external; DV_{CC} = 2.7 V to 5.5 V. V_{OUT}: R_{LOAD} = 1 kΩ, C_L = 200 pF, I_{OUT}: R_{LOAD} = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
WRITE MODE			
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK low time
t_3	13	ns min	SCLK high time
t_4	13	ns min	LATCH delay time
t_5	40	ns min	LATCH high time
t_5	5	µs min	LATCH high time (after a write to the control register)
t_6	5	ns min	Data setup time
t_7	5	ns min	Data hold time
t_8	40	ns min	LATCH low time
t_9	20	ns min	CLEAR pulse width
t_{10}	5	µs max	CLEAR activation time
READBACK MODE			
t_{11}	90	ns min	SCLK cycle time
t_{12}	40	ns min	SCLK low time
t_{13}	40	ns min	SCLK high time
t_{14}	13	ns min	LATCH delay time
t_{15}	40	ns min	LATCH high time
t_{16}	5	ns min	Data setup time
t_{17}	5	ns min	Data hold time
t_{18}	40	ns min	LATCH low time
t_{19}	35	ns max	Serial output delay time ($C_{L\,SDO}$[4] = 15 pF)
t_{20}	35	ns max	LATCH rising edge to SDO tristate ($C_{L\,SDO}$[4] = 15 pF)
DAISY-CHAIN MODE			
t_{21}	90	ns min	SCLK cycle time
t_{22}	40	ns min	SCLK low time
t_{23}	40	ns min	SCLK high time
t_{24}	13	ns min	LATCH delay time
t_{25}	40	ns min	LATCH high time
t_{26}	5	ns min	Data setup time
t_{27}	5	ns min	Data hold time
t_{28}	40	ns min	LATCH low time
t_{29}	35	ns max	Serial output delay time ($C_{L\,SDO}$[4] = 15 pF)

[1] Guaranteed by characterization; not production tested.
[2] All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.
[3] See Figure 2, Figure 3, and Figure 4.
[4] $C_{L\,SDO}$ = capacitive load on SDO output.

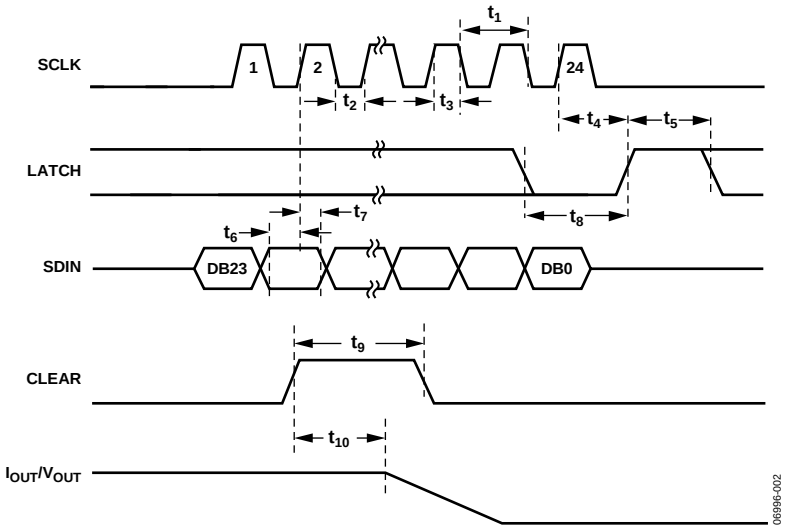


Figure 2. Write Mode Timing Diagram

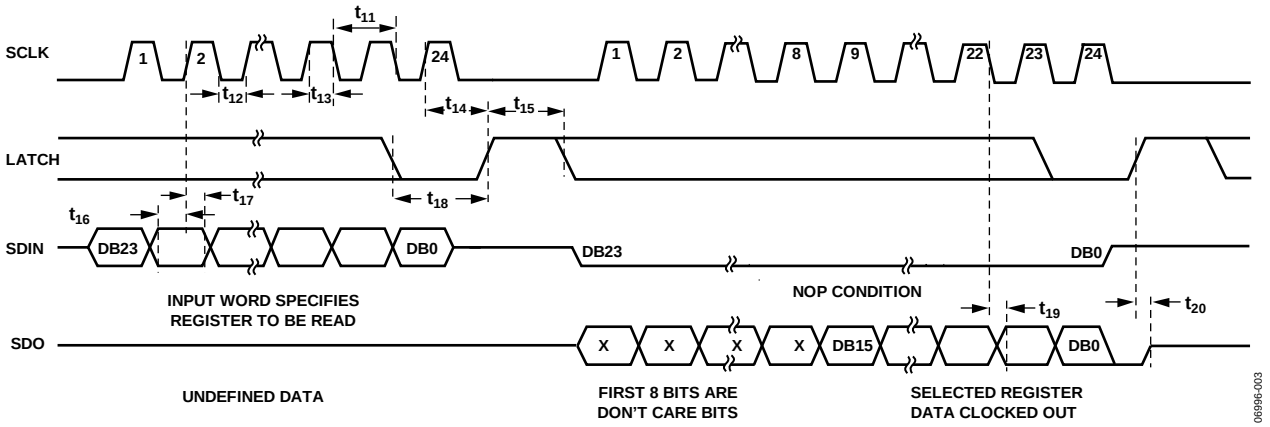


Figure 3. Readback Mode Timing Diagram

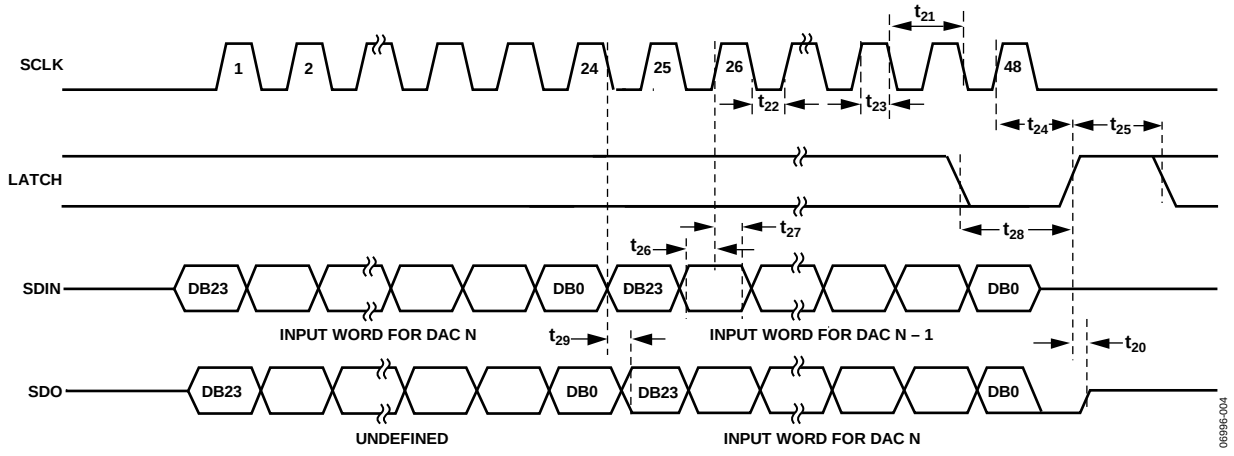


Figure 4. Daisy-Chain Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 80 mA do not cause SCR latch-up.

Table 5.

Parameter	Rating
AV_{DD} to GND	−0.3 V to +48 V
AV_{SS} to GND	+0.3 V to −28 V
AV_{DD} to AV_{SS}	−0.3 V to +60 V
DV_{CC} to GND	−0.3 V to +7 V
Digital Inputs to GND	−0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
Digital Outputs to GND	−0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
REFIN/REFOUT to GND	−0.3 V to +7 V
V_{OUT} to GND	AV_{SS} to AV_{DD}
I_{OUT} to GND	−0.3 V to AV_{DD}
Operating Temperature Range (T_A)	
Industrial[1]	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
24-Lead TSSOP Package	
θ_{JA} Thermal Impedance	42°C/W
40-Lead LFCSP Package	
θ_{JA} Thermal Impedance	28°C/W
Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020
ESD (Human Body Model)	2 kV

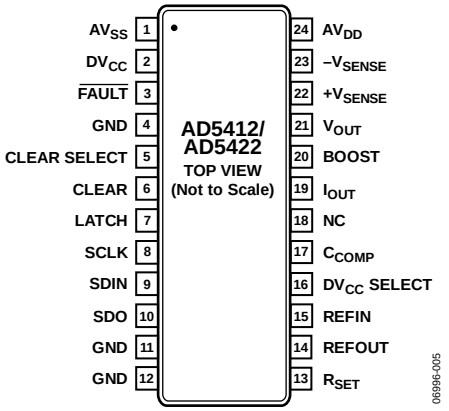
[1] Power dissipated on chip must be derated to keep the junction temperature below 125°C, assuming that the maximum power dissipation condition is sourcing 24 mA into GND from I_{OUT} with a 4 mA on-chip current.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

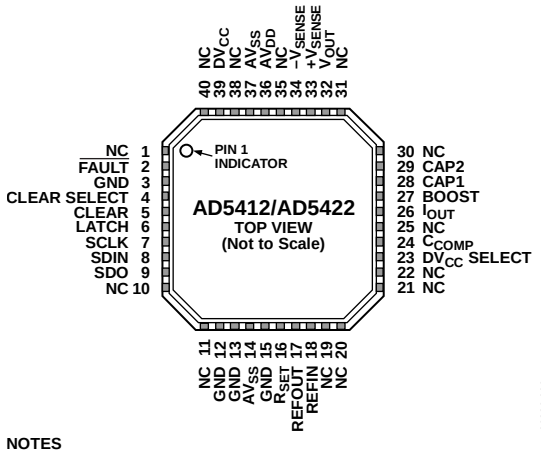
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT
2. THE PADDLE CAN BE CONNECTED TO 0V IF THE OUTPUT VOLTAGE RANGE IS UNIPOLAR. THE PADDLE CAN BE LEFT ELECTRICALLY UNCONNECTED PROVIDED THAT A SUPPLY CONNECTION IS MADE AT THE AV_{SS} PIN. IT IS RECOMMENDED THAT THE PADDLE BE THERMALLY CONNECTED TO A COPPER PLANE FOR ENHANCED THERMAL PERFORMANCE.

Figure 5. TSSOP Pin Configuration



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PADDLE CAN BE CONNECTED TO 0V IF THE OUTPUT VOLTAGE RANGE IS UNIPOLAR. THE EXPOSED PADDLE CAN BE LEFT ELECTRICALLY UNCONNECTED PROVIDED THAT A SUPPLY CONNECTION IS MADE AT THE AV_{SS} PIN. IT IS RECOMMENDED THAT THE PADDLE BE THERMALLY CONNECTED TO A COPPER PLANE FOR ENHANCED THERMAL PERFORMANCE.

Figure 6. LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	14, 37	AV_{SS}	Negative Analog Supply Pin. Voltage ranges from –3 V to –24 V. This pin can be connected to 0 V if the output voltage range is unipolar.
2	39	DV_{CC}	Digital Supply Pin. Voltage ranges from 2.7 V to 5.5 V.
3	2	$\overline{FAULT}$	Fault Alert. This pin is asserted low when an open circuit is detected in current mode or an overtemperature is detected. Open drain output must be connected to a pull-up resistor.
4, 12	3, 15	GND	These pins must be connected to 0 V.
18	1, 10, 11, 19, 20, 21, 22, 25, 30, 31, 35, 38, 40	NC	No Connection. Do not connect to these pins.
5	4	CLEAR SELECT	Selects the voltage output clear value, either zero-scale or midscale code (see Table 21).
6	5	CLEAR	Active High Input. Asserting this pin sets the current output to the bottom of the selected range or sets the voltage output to the user selected value (zero-scale or midscale).
7	6	LATCH	Positive Edge Sensitive Latch. A rising LATCH edge parallel loads the input shift register data into the DAC register, also updating the output.
8	7	SCLK	Serial Clock Input. Data is clocked into the shift register on the rising edge of SCLK. This operates at clock speeds of up to 30 MHz.
9	8	SDIN	Serial Data Input. Data must be valid on the rising edge of SCLK.
10	9	SDO	Serial Data Output. Used to clock data from the serial register in daisy-chain or readback mode. Data is valid on the rising edge of SCLK (see Figure 3 and Figure 4).
11	12, 13	GND	Ground Reference Pin.
13	16	R_{SET}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT} temperature drift performance. See the AD5412/AD5422 Features section.
14	17	REFOUT	Internal Reference Voltage Output. REFOUT = 5 V ± 2 mV.
15	18	REFIN	External Reference Voltage Input. Reference input range is 4 V to 5 V. REFIN = 5 V for a specified performance.

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
16	23	DV_{CC} SELECT	When connected to GND, this pin disables the internal supply, and an external supply must be connected to the DV_{CC} pin. Leave this pin unconnected to enable the internal supply. See the AD5412/AD5422 Features section.
17	24	C_{COMP}	Optional compensation capacitor connection for the voltage output buffer. Connecting a 4 nF capacitor between this pin and the V_{OUT} pin allows the voltage output to drive up to 1 µF. It should be noted that the addition of this capacitor reduces the bandwidth of the output amplifier, increasing the settling time.
19	26	I_{OUT}	Current Output Pin.
20	27	BOOST	Optional External Transistor Connection. Connecting an external transistor reduces the power dissipated in the AD5412/AD5422. See theAD5412/AD5422 Features section.
N/A	28, 29	CAP1, CAP2	Connection for Optional Output Filtering Capacitor. See the AD5412/AD5422 Features section.
21	32	V_{OUT}	Buffered Analog Output Voltage. The output amplifier is capable of directly driving a 1 kΩ, 2000 pF load.
22	33	$+V_{SENSE}$	Sense connection for the positive voltage output load connection.
23	34	$-V_{SENSE}$	Sense connection for the negative voltage output load connection.
24	36	AV_{DD}	Positive Analog Supply Pin. Voltage ranges from 10.8 V to 60 V.
25 (EPAD)	41 (EPAD)	Exposed paddle	Negative Analog Supply Pin. Voltage ranges from –3 V to –24 V. This paddle can be connected to 0 V if the output voltage range is unipolar. The paddle can be left electrically unconnected provided that a supply connection is made at the AV_{SS} pin. It is recommended that the paddle be thermally connected to a copper plane for enhanced thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

GENERAL

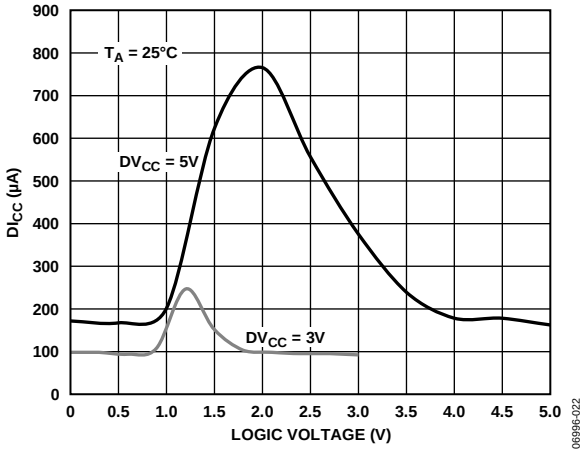


Figure 7. DI_{CC} vs. Logic Input Voltage

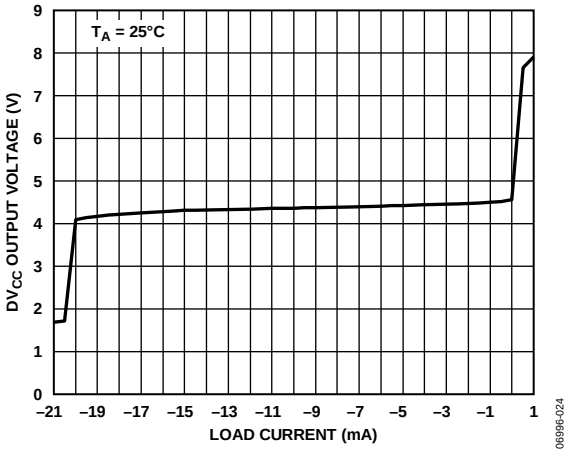


Figure 10. DV_{CC} Output Voltage vs. Load Current

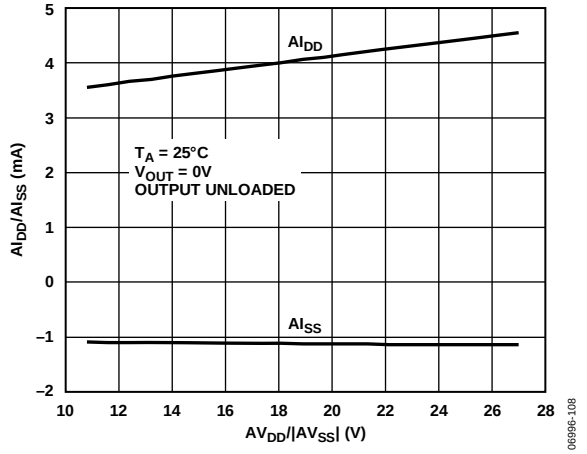


Figure 8. AI_{DD}/AI_{SS} vs. $AV_{DD}/|AV_{SS}|$

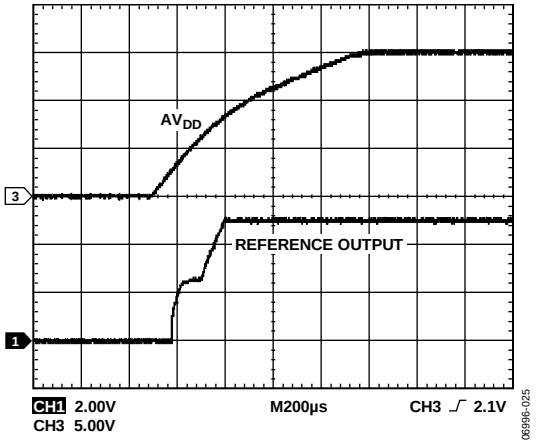


Figure 11. REFOUT Turn-on Transient

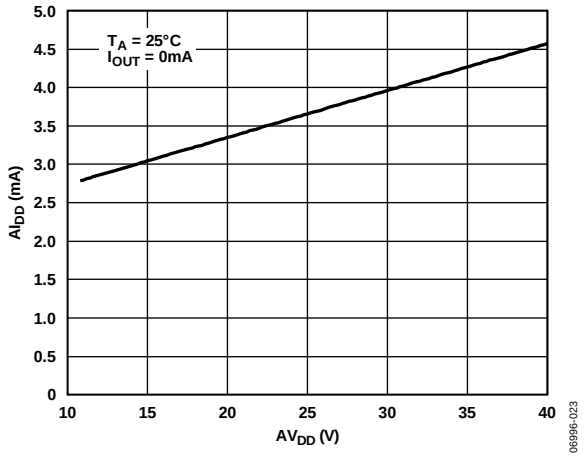


Figure 9. AI_{DD} vs. AV_{DD}

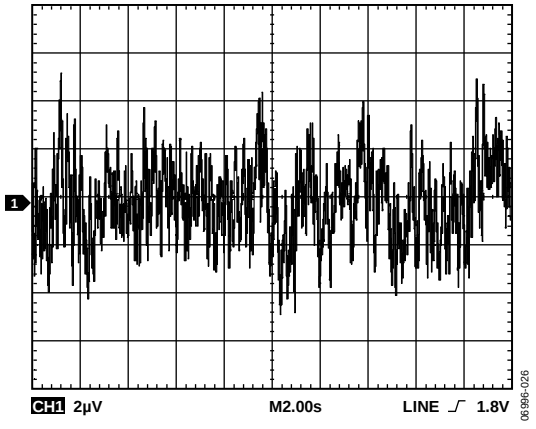


Figure 12. REFOUT Output Noise (0.1 Hz to 10 Hz Bandwidth)

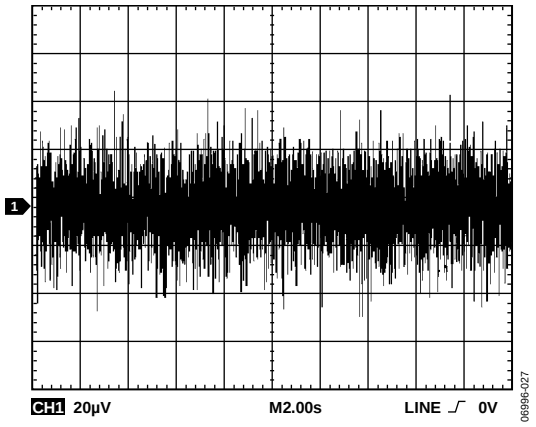


Figure 13. REFOUT Output Noise (100 kHz Bandwidth)

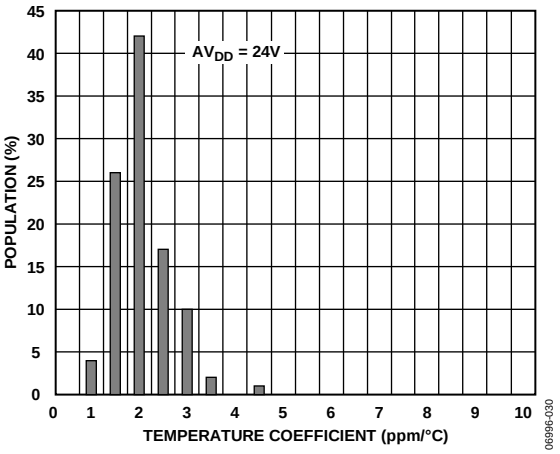


Figure 15. Reference Temperature Coefficient Histogram

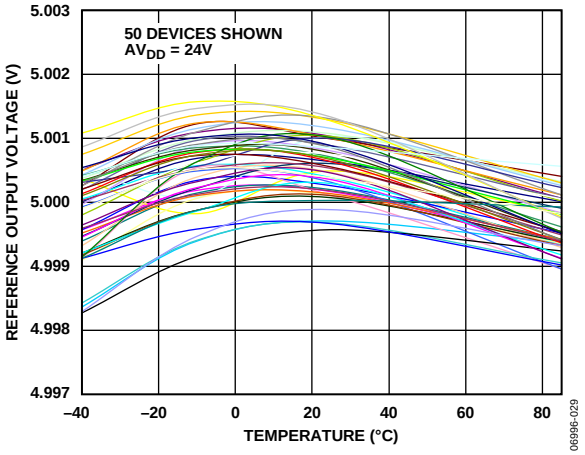


Figure 14. Reference Voltage vs. Temperature

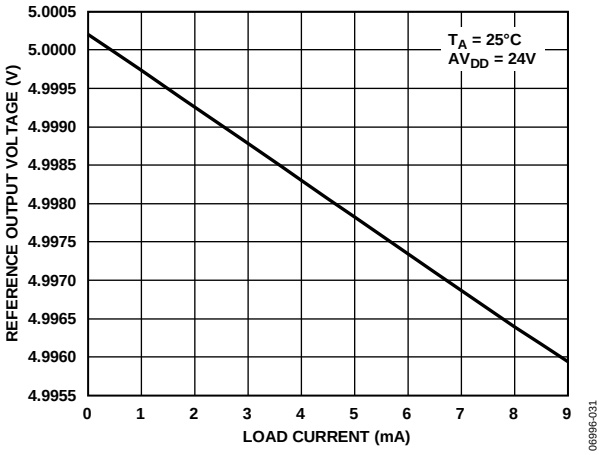


Figure 16. Reference Voltage vs. Load Current

VOLTAGE OUTPUT

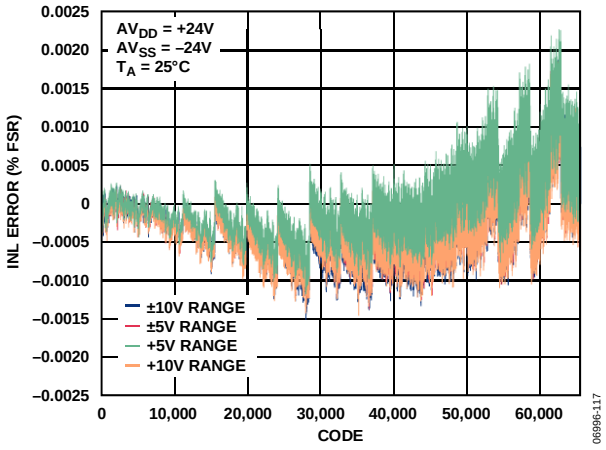


Figure 17. Integral Nonlinearity Error vs. DAC Code, Dual Supply

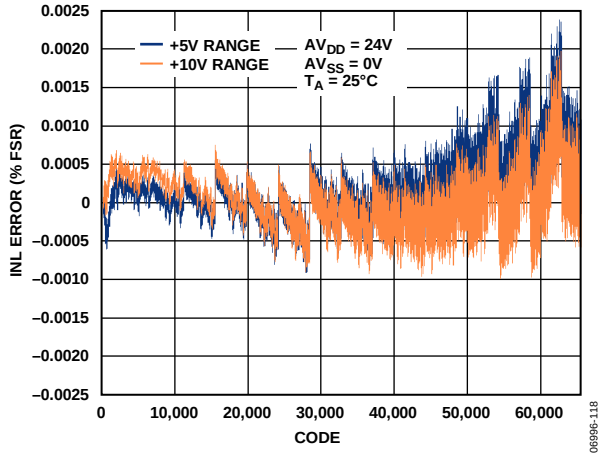


Figure 18. Integral Nonlinearity Error vs. DAC Code, Single Supply

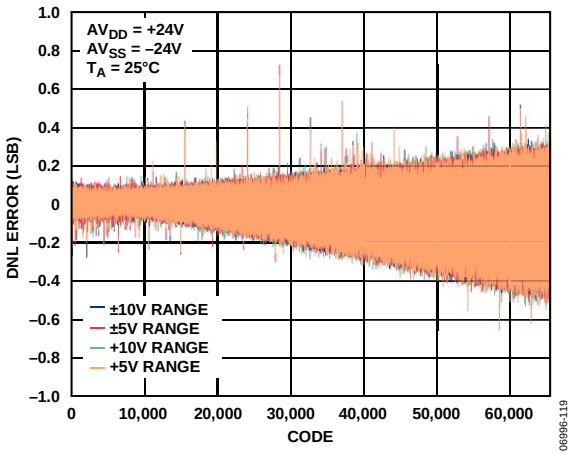


Figure 19. Differential Nonlinearity Error vs. DAC Code, Dual Supply

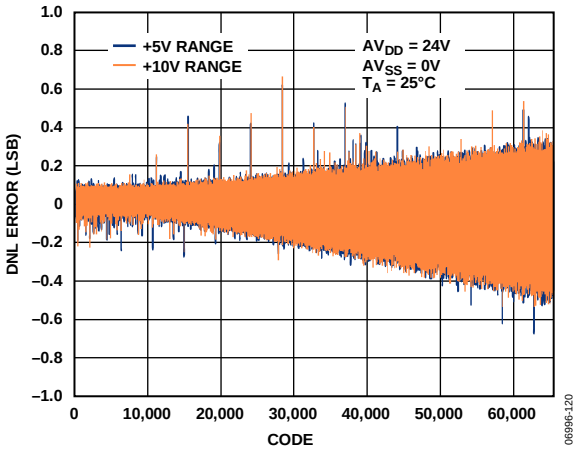


Figure 20. Differential Nonlinearity Error vs. DAC Code, Single Supply

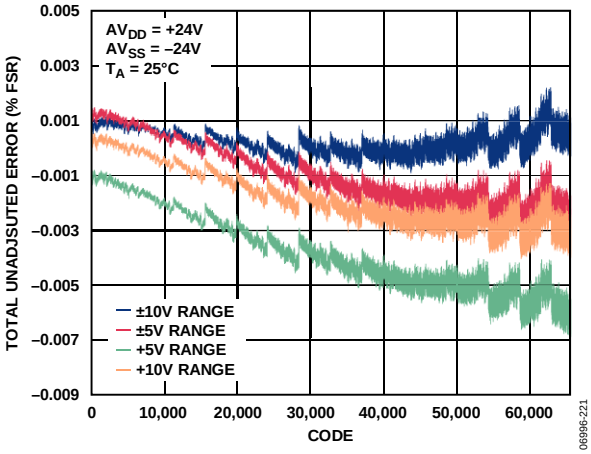


Figure 21. Total Unadjusted Error vs. DAC Code, Dual Supply

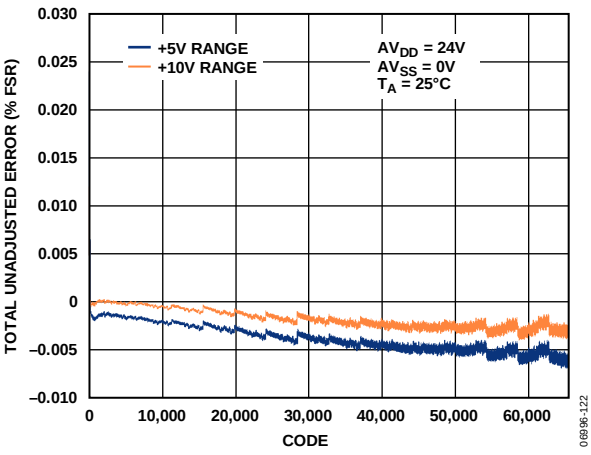


Figure 22. Total Unadjusted Error vs. DAC Code, Single Supply

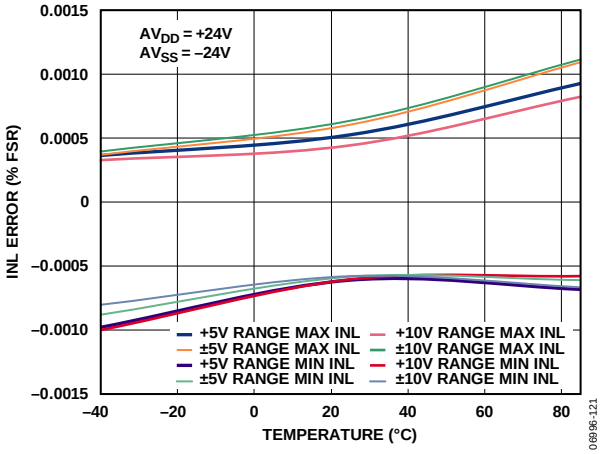


Figure 23. Integral Nonlinearity Error vs. Temperature

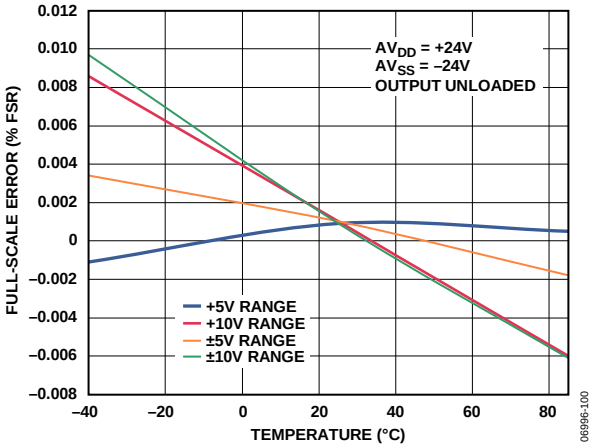


Figure 26. Full-Scale Error vs. Temperature

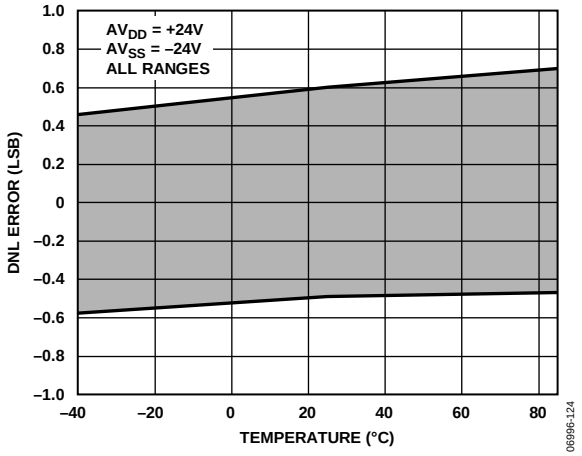


Figure 24. Differential Nonlinearity Error vs. Temperature

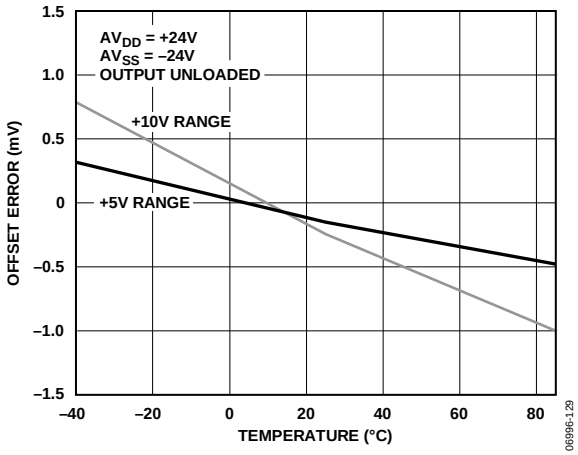


Figure 27. Offset Error vs. Temperature

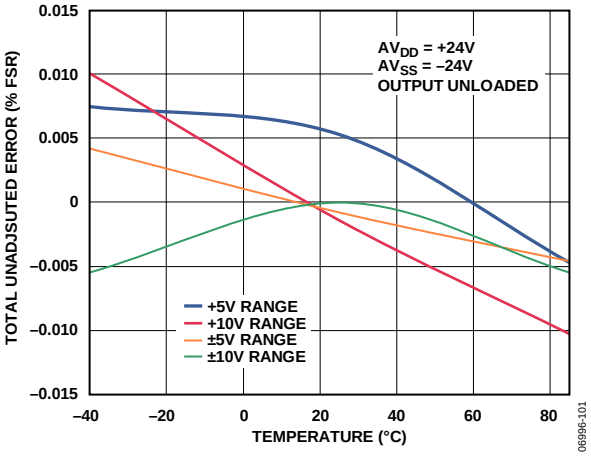


Figure 25. Total Unadjusted Error vs. Temperature

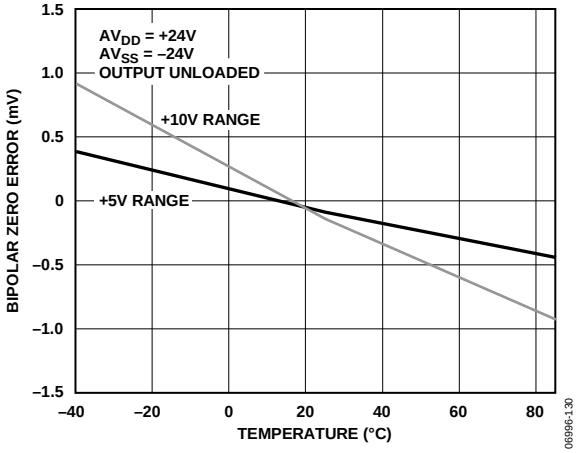


Figure 28. Bipolar Zero Error vs. Temperature

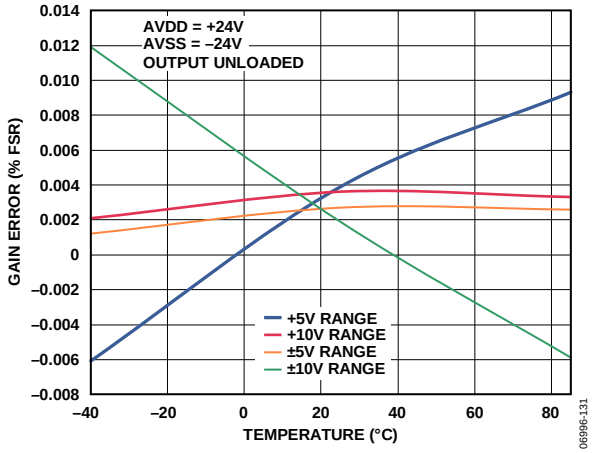


Figure 29. Gain Error vs. Temperature

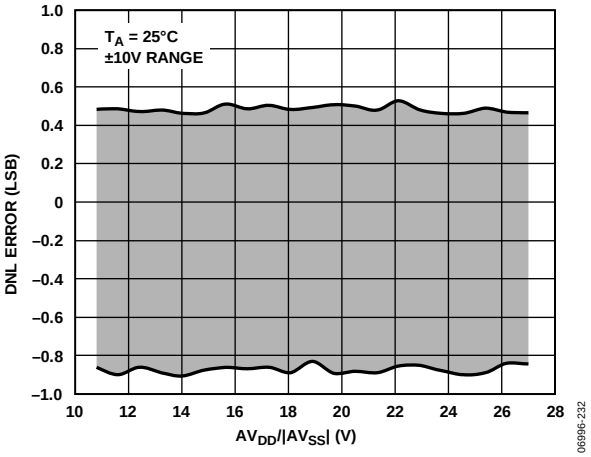


Figure 32. Differential Nonlinearity Error vs. $AV_{DD}/|AV_{SS}|$

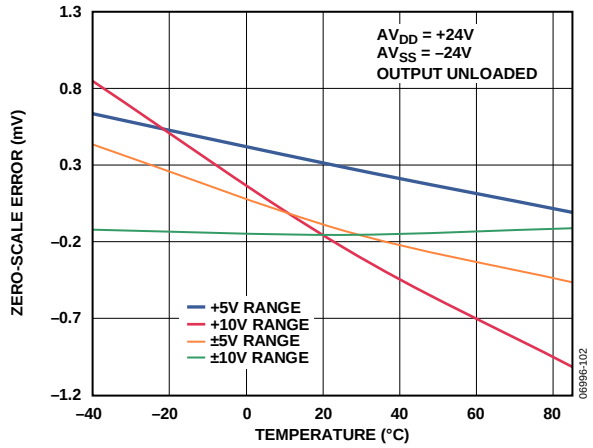


Figure 30. Zero-Scale Error vs. Temperature

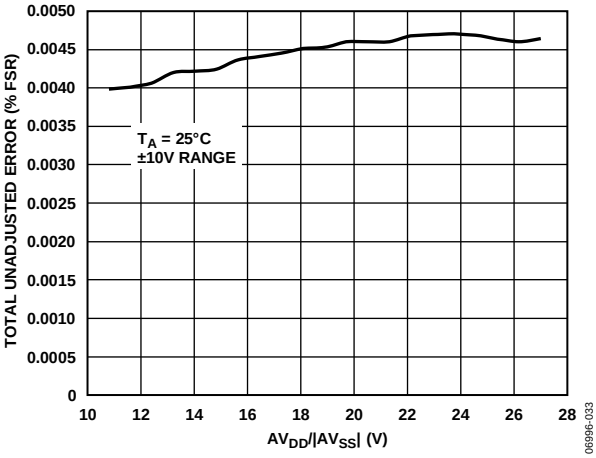


Figure 33. Total Unadjusted Error vs. $AV_{DD}/|AV_{SS}|$

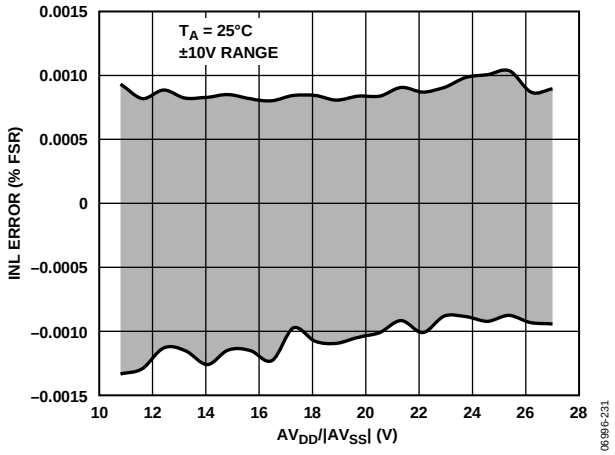


Figure 31. Integral Nonlinearity Error vs. $AV_{DD}/|AV_{SS}|$

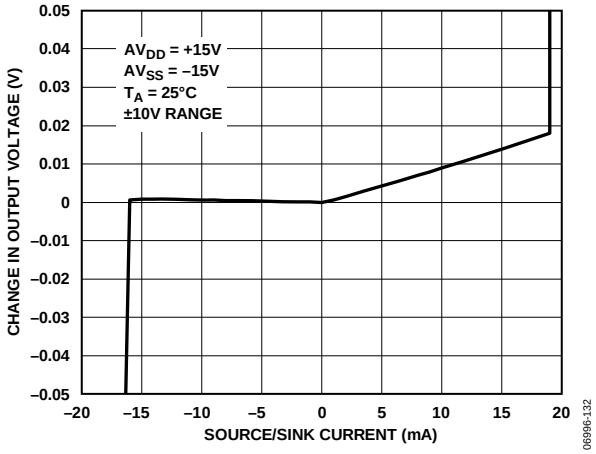


Figure 34. Source and Sink Capability of Output Amplifier, Full-Scale Code Loaded

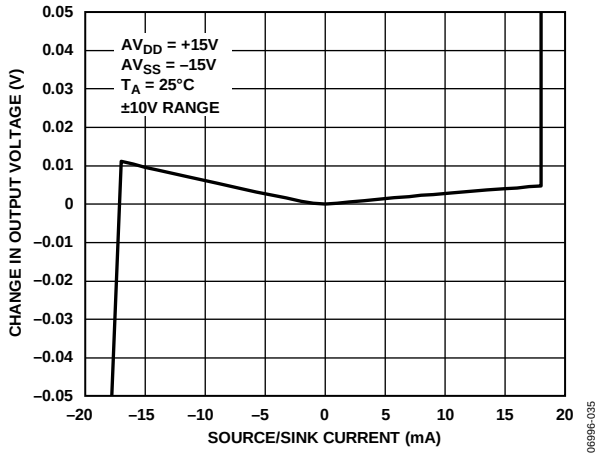


Figure 35. Source and Sink Capability of Output Amplifier, Zero-Scale Loaded

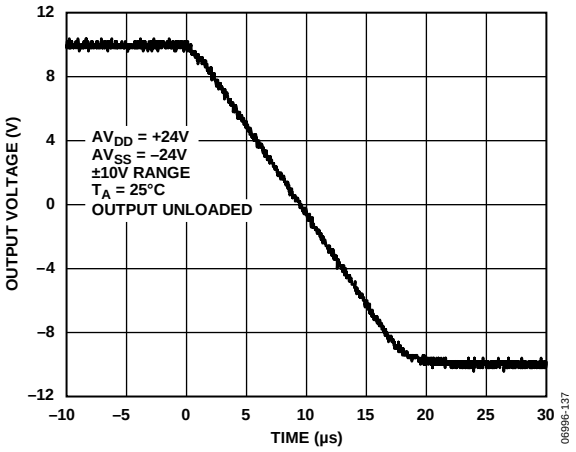


Figure 37. Full-Scale Negative Step

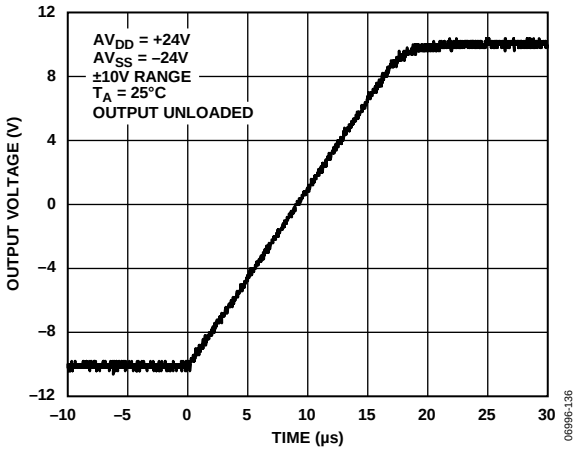


Figure 36. Full-Scale Positive Step

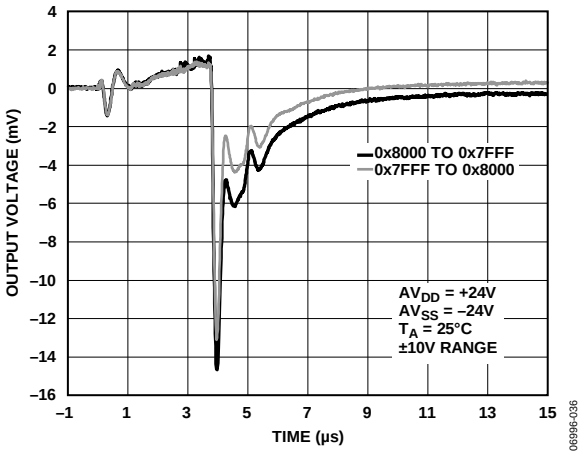


Figure 38. Digital-to-Analog Glitch

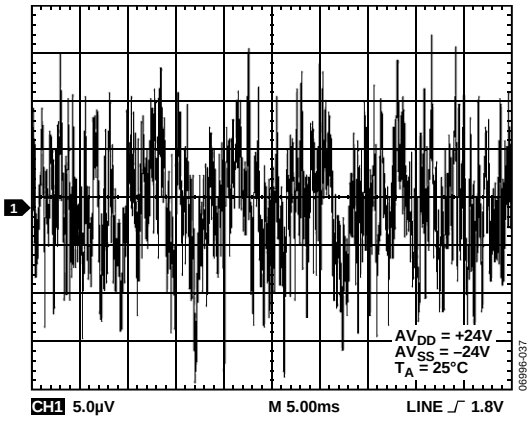


Figure 39. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

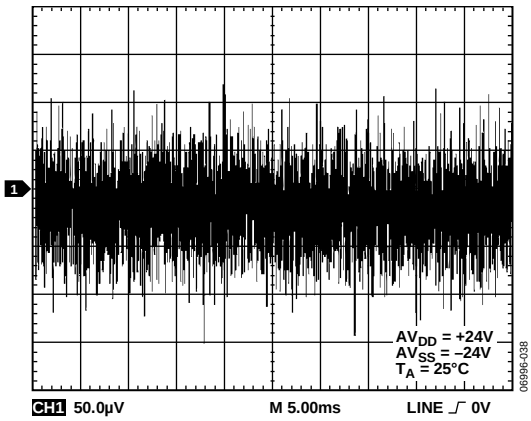


Figure 40. Peak-to-Peak Noise (100 kHz Bandwidth)

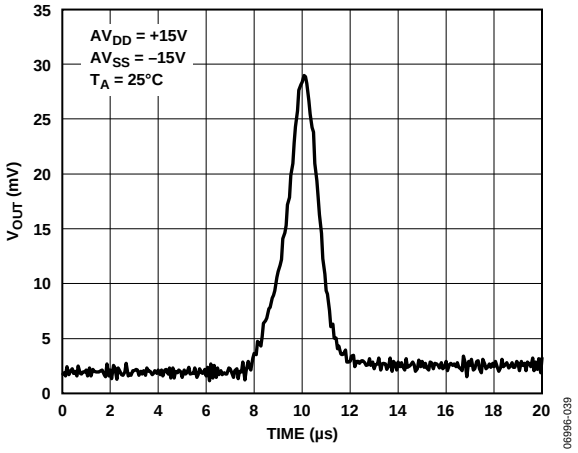


Figure 41. V_{OUT} vs. Time on Power-Up

CURRENT OUTPUT

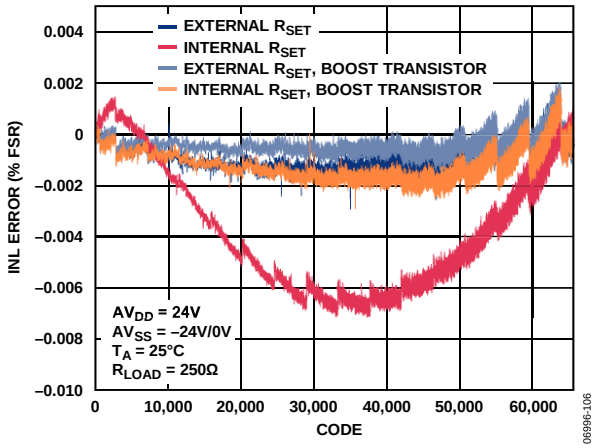


Figure 42. Integral Nonlinearity vs. Code

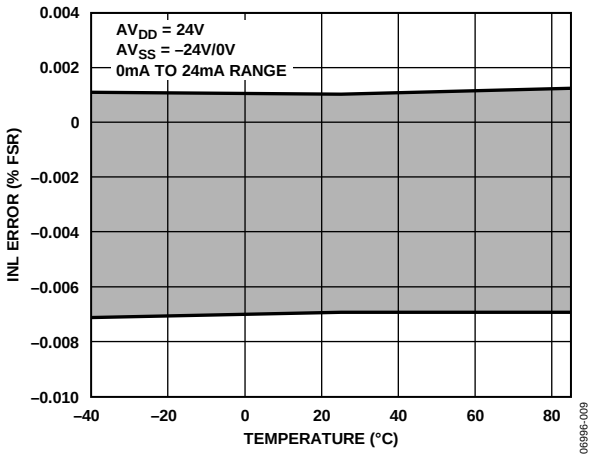


Figure 45. Integral Nonlinearity vs. Temperature, Internal R_{SET}

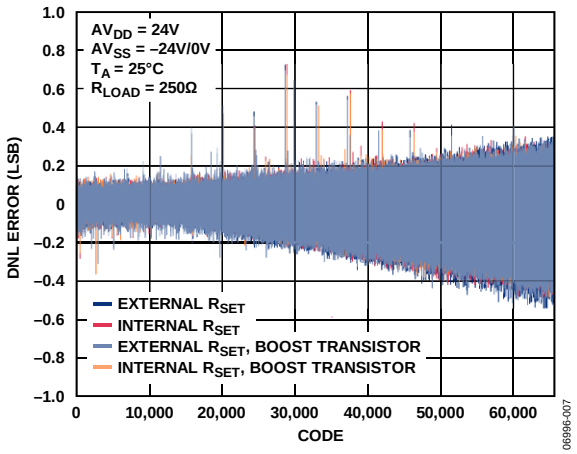


Figure 43. Differential Nonlinearity vs. Code

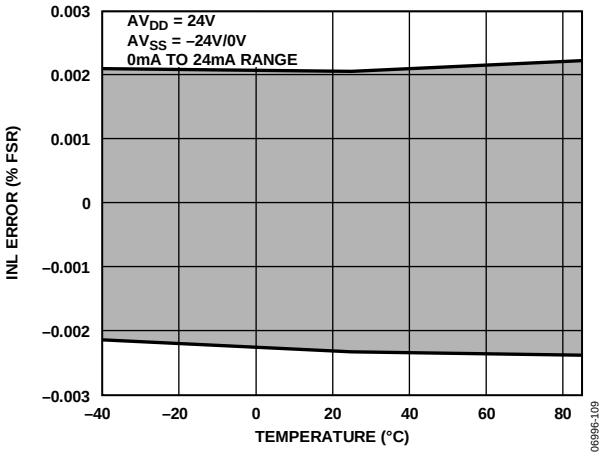


Figure 46. Integral Nonlinearity vs. Temperature, External R_{SET}

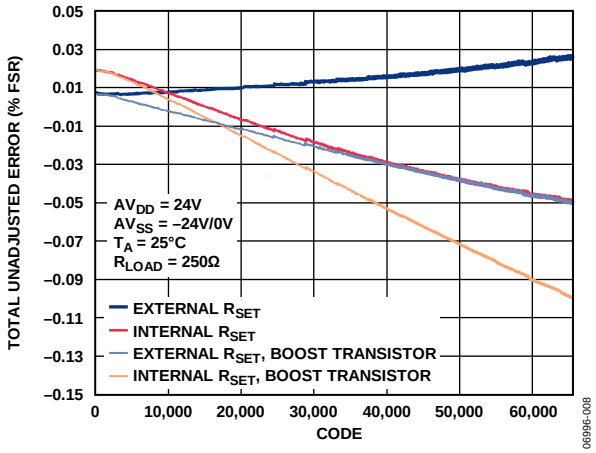


Figure 44. Total Unadjusted Error vs. Code

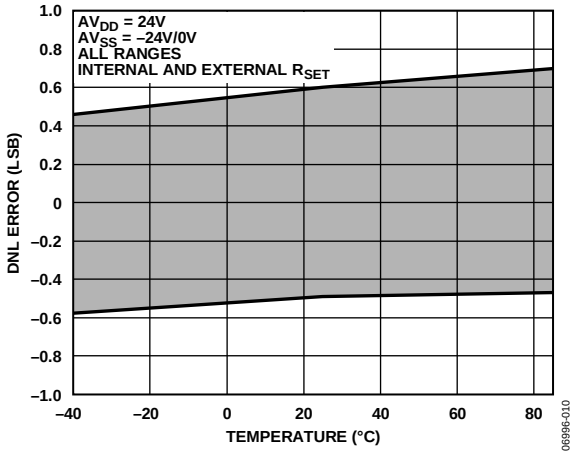


Figure 47. Differential Nonlinearity vs. Temperature

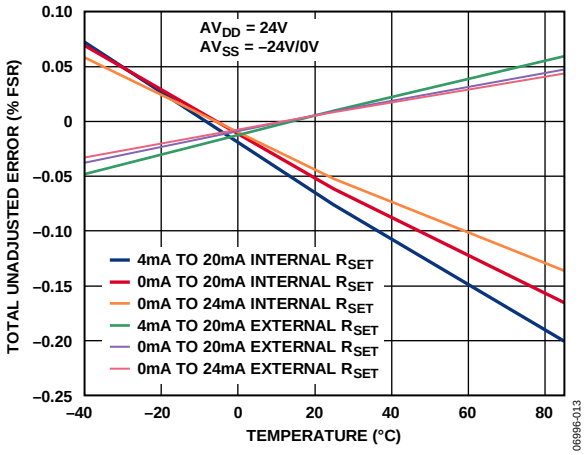


Figure 48. Total Unadjusted Error vs. Temperature

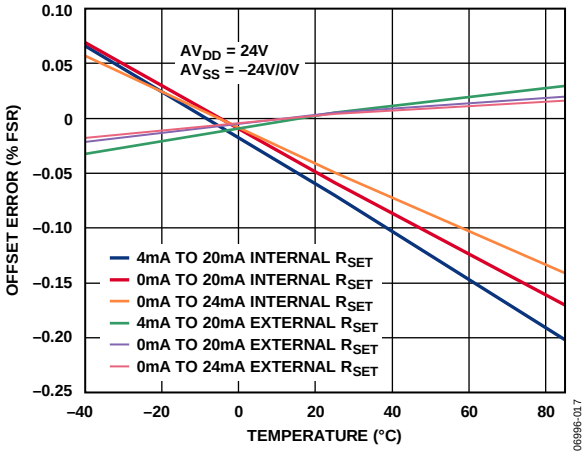


Figure 49. Offset Error vs. Temperature

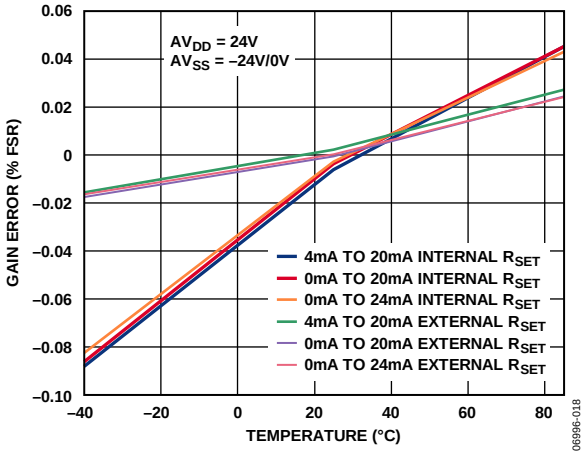


Figure 50. Gain Error vs. Temperature

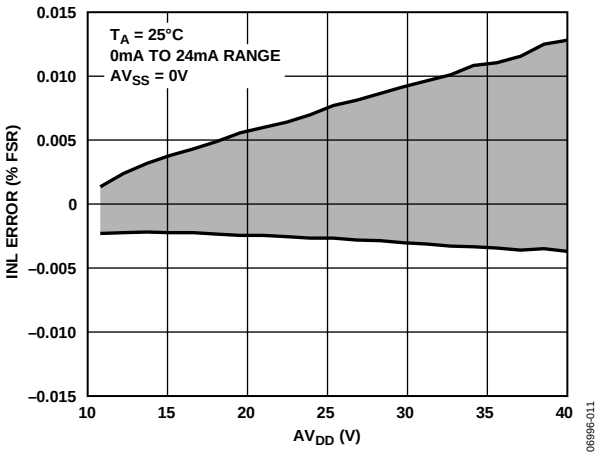


Figure 51. Integral Nonlinearity Error vs. AV_{DD}, External R_{SET}

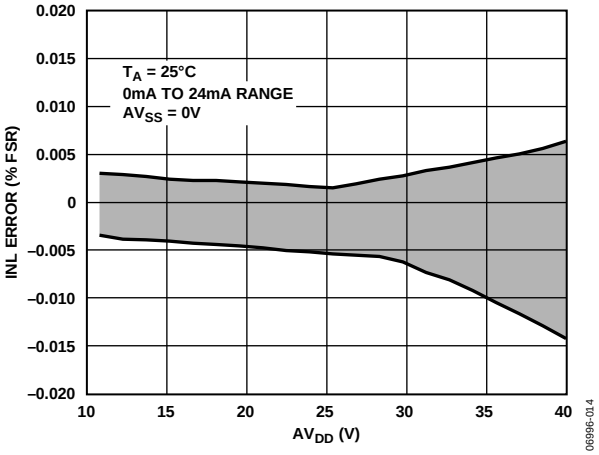


Figure 52. Integral Nonlinearity Error vs. AV_{DD}, Internal R_{SET}

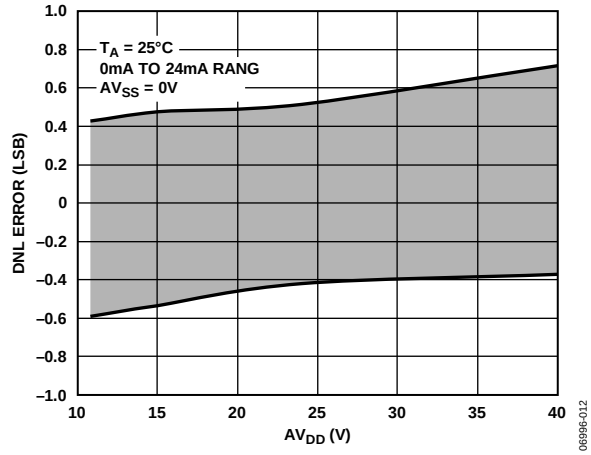


Figure 53. Differential Nonlinearity Error vs. AV_{DD}, External R_{SET}

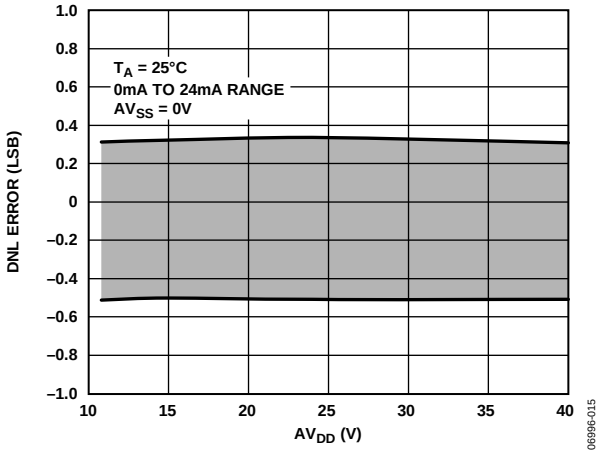


Figure 54. Differential Nonlinearity Error vs. AV_{DD}, Internal R_{SET}

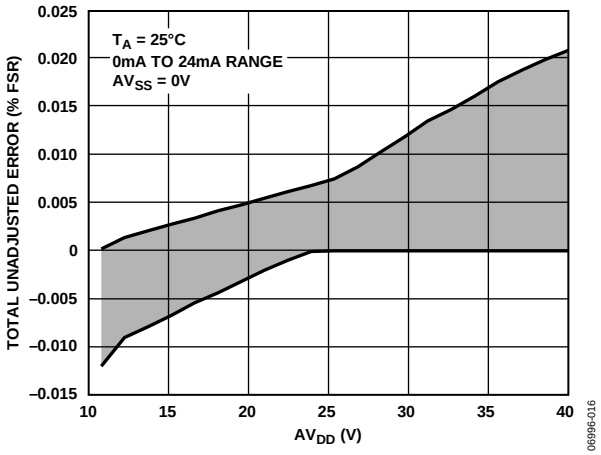


Figure 55. Total Unadjusted Error vs. AV_{DD}, External R_{SET}

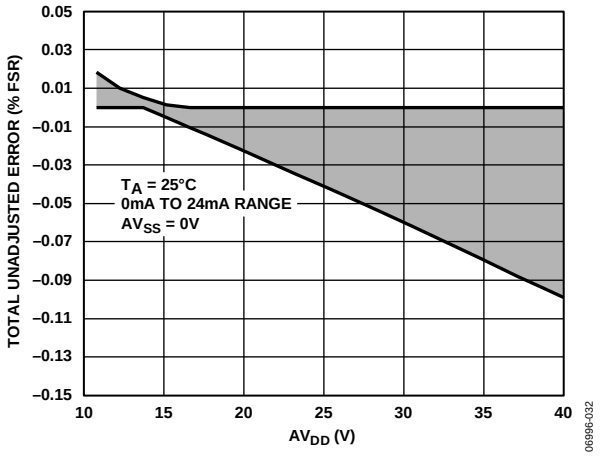


Figure 56. Total Unadjusted Error vs. AV_{DD}, Internal R_{SET}

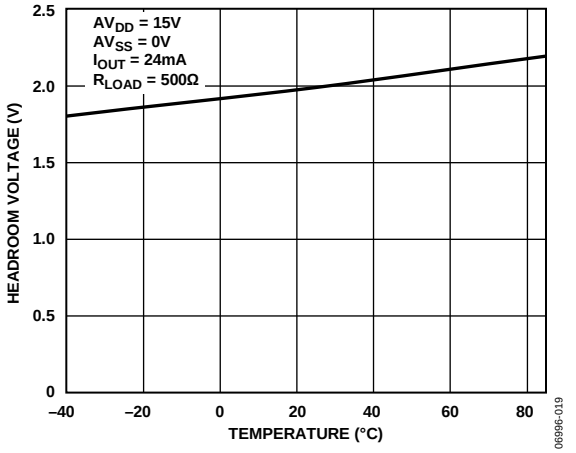


Figure 57. Compliance Voltage Headroom vs. Temperature

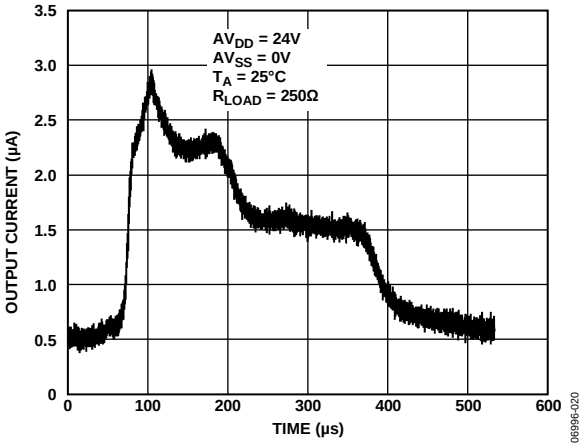


Figure 58. Output Current vs. Time on Power-Up

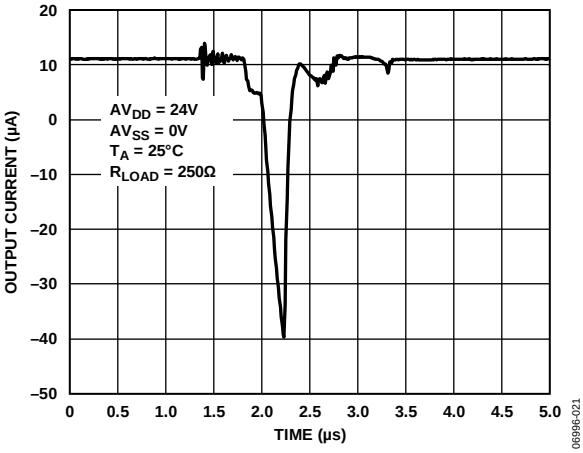


Figure 59. Output Current vs. Time on Output Enable

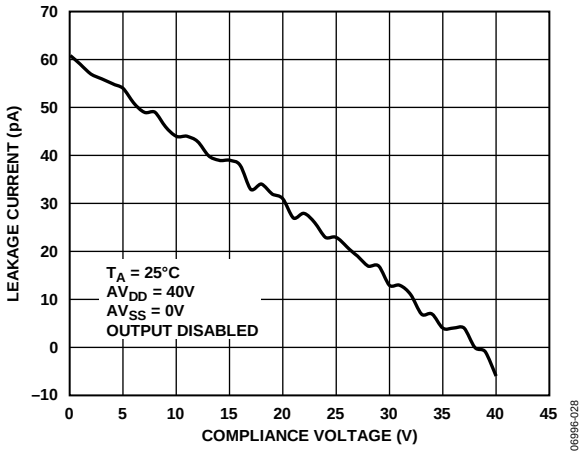


Figure 60. Output Leakage Current vs. Compliance Voltage

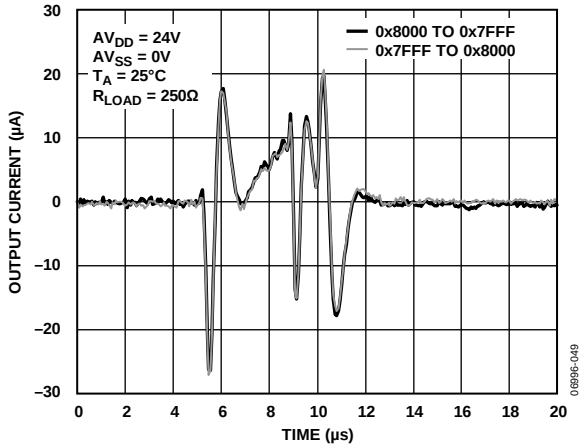


Figure 61. Digital to Analog Glitch

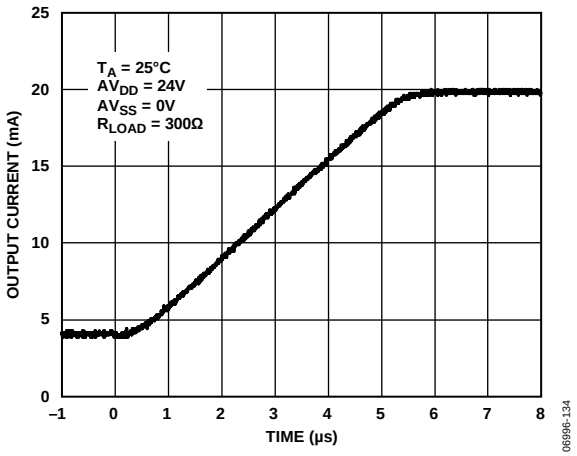


Figure 62. 4 mA to 20 mA Output Current Step

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy, or INL, is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 17.

Differential Nonlinearity (DNL)
DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 19.

Monotonicity
A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5412/AD5422 are monotonic over their full operating temperature range.

Bipolar Zero Error
Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the DAC register is loaded with 0x8000 (straight binary coding) or 0x0000 (twos complement coding). A plot of bipolar zero error vs. temperature can be seen in Figure 28.

Bipolar Zero Temperature Coefficient (TC)
Bipolar zero TC is a measure of the change in the bipolar zero error with a change in temperature. It is expressed in ppm FSR/°C.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code is loaded to the DAC register. Ideally, the output should be full-scale − 1 LSB. Full-scale error is expressed in percent of full-scale range (% FSR).

Negative Full-Scale Error/Zero-Scale Error
Negative full-scale error is the error in the DAC output voltage when 0x0000 (straight binary coding) or 0x8000 (twos complement coding) is loaded to the DAC register. Ideally, the output voltage should be negative full-scale − 1 LSB. A plot of zero-scale error vs. temperature can be seen in Figure 30.

Zero-Scale Temperature Coefficient (TC)
Zero-scale TC is a measure of the change in zero-scale error with a change in temperature. Zero-scale error TC is expressed in ppm FSR/°C.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

Slew Rate
The slew rate of a device is a limitation in the rate of change of the output voltage. The output slewing speed of a voltage-output DAC is usually limited by the slew rate of the amplifier used at its output. Slew rate is measured from 10% to 90% of the output signal and is expressed in V/µs.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed in % FSR. A plot of gain error vs. temperature can be seen in Figure 29.

Gain Error Temperature Coefficient (TC)
Gain error TC is a measure of the change in gain error with changes in temperature. Gain error TC is expressed in ppm FSR/°C.

Total Unadjusted Error (TUE)
TUE is a measure of the output error taking all the various errors into account, namely INL error, offset error, gain error, and output drift over supplies, temperature, and time. TUE is expressed in % FSR.

Current Loop Voltage Compliance
The maximum voltage at the I_{OUT} pin for which the output current is equal to the programmed value.

Power-On Glitch Energy
Power-on glitch energy is the impulse injected into the analog output when the AD5412/AD5422 is powered on. It is specified as the area of the glitch in nV-sec. See Figure 41 and Figure 58.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state, but the output voltage remains constant. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 38 and Figure 61.

Glitch Impulse Peak Amplitude
Glitch impulse peak amplitude is the peak amplitude of the impulse injected into the analog output when the input code in the DAC register changes state. It is specified as the amplitude of the glitch in millivolt and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 38 and Figure 61.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus.

Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the power supply voltage.

Voltage Reference TC
Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C, as follows:

$$TC = \left[\frac{V_{REFmax} - V_{REFmin}}{V_{REFnom} \times TempRange} \right] \times 10^6$$

where:
V_{REFmax} is the maximum reference output measured over the total temperature range.
V_{REFmin} is the minimum reference output measured over the total temperature range.
V_{REFnom} is the nominal reference output voltage, 5 V.
TempRange is the specified temperature range, −40°C to +85°C.

Load Regulation
Load regulation is the change in reference output voltage due to a specified change in load current. It is expressed in ppm/mA.

THEORY OF OPERATION

The AD5412/AD5422 are precision digital-to-current loop and voltage output converters designed to meet the requirements of industrial process control applications. They provide a high precision, fully integrated, low cost single-chip solution for generating current loop and unipolar/bipolar voltage outputs. Current ranges are 0 mA to 20 mA, 0 mA to 24 mA, and 4 mA to 20 mA; the voltage ranges available are 0 V to 5 V, ±5 V, 0 V to 10 V, and ±10 V; a 10% overrange is available on all voltage output ranges. The current and voltage outputs are available on separate pins, and only one is active at any time. The desired output configuration is user selectable via the control register.

ARCHITECTURE

The DAC core architecture of the AD5412/AD5422 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 63. The four MSBs of the 12-/16-bit data-word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either ground or the reference buffer output. The remaining 8/12 bits of the data-word drive the S0 to S7/S11 switches of an 8-/12-bit voltage mode R-2R ladder network.

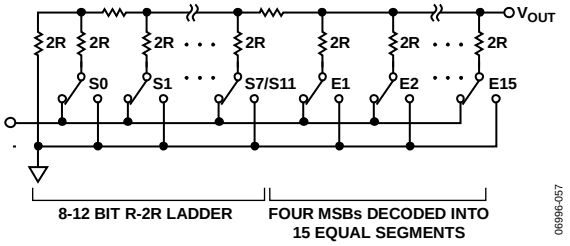


Figure 63. DAC Ladder Structure

The voltage output from the DAC core is either converted to a current (see Figure 64) which is then mirrored to the supply rail so that the application simply sees a current source output with respect to ground or it is buffered and scaled to output a software selectable unipolar or bipolar voltage range (see Figure 65). The current and voltage are output on separate pins and cannot be output simultaneously.

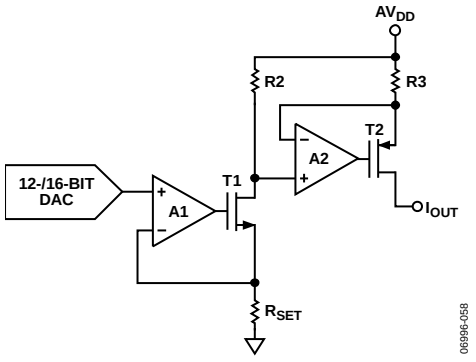


Figure 64. Voltage-to-Current Conversion Circuitry

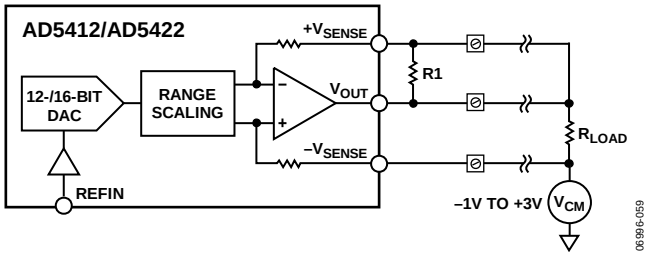


Figure 65. Voltage Output

Voltage Output Amplifier

The voltage output amplifier is capable of generating both unipolar and bipolar output voltages. It is capable of driving a load of 1 kΩ in parallel with 1 µF (with an external compensation capacitor) to GND. The source and sink capabilities of the output amplifier can be seen in Figure 35. The slew rate is 1 V/µs with a full-scale settling time of 25 µs maximum (10 V step). Figure 65 shows the voltage output driving a load, R_{LOAD}, on top of a common-mode voltage (V_{CM}) of −1 V to +3 V. In output module applications where a cable could possibly become disconnected from $+V_{SENSE}$, resulting in the amplifier loop being broken and possibly resulting in large destructive voltages on V_{OUT}, include an optional resistor (R1) between $+V_{SENSE}$ and V_{OUT}, as shown in Figure 65, of a value between 2 kΩ and 5 kΩ to ensure the amplifier loop is kept closed. If remote sensing of the load is not required, connect $+V_{SENSE}$ directly to V_{OUT} and connect $-V_{SENSE}$ directly to GND. When changing ranges on the voltage output, a glitch may occur. For this reason, it is recommended that the output be disabled by setting the OUTEN bit of the control register to logic low before changing the output voltage range; this prevents a glitch from occurring.

Driving Large Capacitive Loads

The voltage output amplifier is capable of driving capacitive loads of up to 1 µF with the addition of a nonpolarized 4 nF compensation capacitor between the C_{COMP} and V_{OUT} pins. Without the compensation capacitor, up to 20 nF capacitive loads can be driven.

SERIAL INTERFACE

The AD5412/AD5422 are controlled over a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz. It is compatible with SPI, QSPI™, MICROWIRE, and DSP standards.

Input Shift Register

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK. Data is clocked in on the rising edge of SCLK. The input register consists of eight address bits and 16 data bits, as shown in Table 7. The 24-bit word is unconditionally latched on the rising edge of the LATCH pin. Data continues to be clocked in irrespective of the state of LATCH. On the rising edge of LATCH, the data that is present in the input register is latched; in other words, the last 24 bits to be clocked in before the rising edge of LATCH is the data that is latched. The timing diagram for this operation is shown in Figure 2.

Table 7. Input Shift Register Format

MSB	LSB
D23 to D16	**D15 to D0**
Address byte	Data-word

Table 8. Address Byte Functions

Address Word	Function
00000000	No operation (NOP)
00000001	Data register
00000010	Readback register value as per read address (see Table 9)
01010101	Control register
01010110	Reset register

Standalone Operation

The serial interface works with both a continuous and noncontinuous serial clock. A continuous SCLK source can be used only if LATCH is taken high after the correct number of data bits have been clocked in. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and LATCH must be taken high after the final clock to latch the data. The rising edge of SCLK that clocks in the MSB of the data-word marks the beginning of the write cycle. Exactly 24 rising clock edges must be applied to SCLK before LATCH is brought high. If LATCH is brought high before the 24th rising SCLK edge, the data written is invalid. If more than 24 rising SCLK edges are applied before LATCH is brought high, the input data is also invalid.

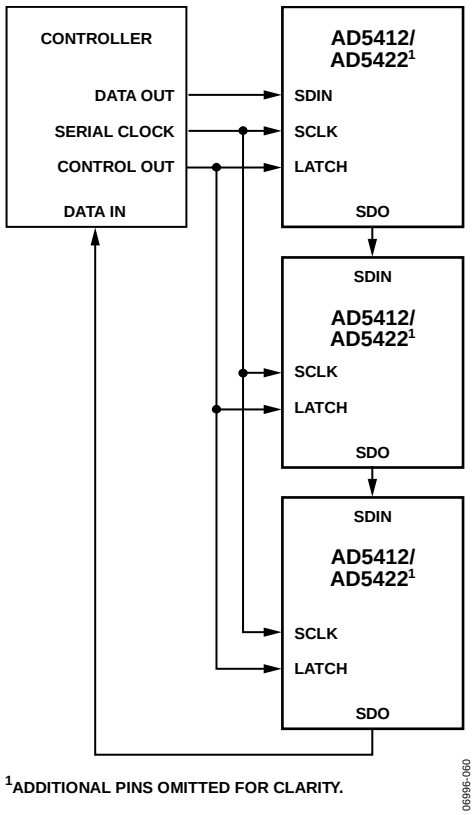


Figure 66. Daisy Chaining the AD5412/AD5422

Daisy-Chain Operation

For systems that contain several devices, the SDO pin can be used to daisy-chain the devices together as shown in Figure 66. This daisy-chain mode can be useful in system diagnostics and in reducing the number of serial interface lines. Daisy-chain mode is enabled by setting the DCEN bit of the control register to 1. The first rising edge of SCLK that clocks in the MSB of the data-word marks the beginning of the write cycle. SCLK is continuously applied to the input shift register. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is valid on the rising edge of SCLK, having been clocked out on the previous falling SCLK edge. By connecting the SDO of the first device to the SDIN input of the next device in the chain, a multidevice interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24 × n, where n is the total number of AD5412/AD5422 devices in the chain. When the serial transfer to all devices is complete, LATCH is taken high. This latches the input data in each device in the daisy chain. The serial clock can be a continuous or a gated clock.

A continuous SCLK source can be used only if LATCH is taken high after the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and LATCH must be taken high after the final clock to latch the data (see Figure 4 for a timing diagram).

Readback Operation

Readback mode is invoked by setting the address byte and read address when writing to the input register (see Table 9 and Table 11). The next write to the AD5412/AD5422 should be a NOP command, which clocks out the data from the previously addressed register as shown in Figure 3.

By default the SDO pin is disabled after having addressed the AD5412/AD5422 for a read operation; a rising edge on LATCH enables the SDO pin in anticipation of data being clocked out. After the data has been clocked out on SDO, a rising edge on LATCH disables (tristate) the SDO pin. To read back the data register, for example, implement the following sequence:

1. Write 0x020001 to the input register. This configures the part for read mode with the data register selected.
2. Follow this with a second write: a NOP condition, which is 0x000000. During this write, the data from the register is clocked out on the SDO line.

Table 9. Read Address Decoding

Read Address	Function
00	Read status register
01	Read data register
10	Read control register

POWER-ON STATE

During power-on of the AD5412/AD5422, the power-on-reset circuit ensures that all registers are loaded with zero-code. As such, both outputs are disabled; that is, the V_{OUT} and I_{OUT} pins are in tristate. The $+V_{SENSE}$ pin is internally connected to ground through a 40 kΩ resistor. Therefore, if the V_{OUT} and $+V_{SENSE}$ pins are connected together, V_{OUT} is effectively clamped to ground through a 40 kΩ resistor. Also upon power-on, internal calibration registers are read, and the data is applied to internal calibration circuitry. For a reliable read operation, there must be sufficient voltage on the AV_{DD} supply when the read event is triggered by the DV_{CC} power supply powering up. Powering up the DV_{CC} supply after the AV_{DD} supply ensures this. If DV_{CC} and AV_{DD} are powered up simultaneously or the internal DV_{CC} is enabled, the supplies should be powered up at a rate greater than, typically, 500 V/sec or 24 V/50 ms. If this cannot be achieved, issue a reset command to the AD5412/AD5422 after power-on; this performs a power-on-reset event, reading the calibration registers and ensures specified operation of the AD5412/AD5422.

Voltage Output

For a unipolar voltage output range, the output voltage can be expressed as

$$V_{OUT} = V_{REFIN} \times Gain\left[\frac{D}{2^N}\right]$$

For a bipolar voltage output range, the output voltage can be expressed as

$$V_{OUT} = V_{REFIN} \times Gain\left[\frac{D}{2^N}\right] - \frac{Gain \times V_{REFIN}}{2}$$

where:
D is the decimal equivalent of the code loaded to the DAC.
N is the bit resolution of the DAC.
V_{REFIN} is the reference voltage applied at the REFIN pin.
Gain is an internal gain whose value depends on the output range selected by the user as shown in Table 10.

Table 10. Internal Gain Value

Output Range	Gain Value
+5 V	1
+10 V	2
±5 V	2
±10 V	4

Current Output

For the 0 mA to 20 mA, 0 mA to 24 mA, and 4 mA to 20 mA current output ranges, the output current is respectively expressed as

$$I_{OUT} = \left[\frac{20\text{ mA}}{2^N}\right] \times D$$

$$I_{OUT} = \left[\frac{24\text{ mA}}{2^N}\right] \times D$$

$$I_{OUT} = \left[\frac{16\text{ mA}}{2^N}\right] \times D + 4\text{ mA}$$

where:
D is the decimal equivalent of the code loaded to the DAC.
N is the bit resolution of the DAC.

Table 11. Input Shift Register Contents for a Read Operation

MSB										LSB
D23	D22	D21	D20	D19	D18	D17	D16	D15 to D2	D1	D0
0	0	0	0	0	0	1	0	X[1]	Read address	

[1] X = don't care.

DATA REGISTER

The data register is addressed by setting the address word of the input shift register to 0x01. The data to be written to the data register is entered in the D15 to D4 positions for the AD5412 and the D15 to D0 positions for the AD5422, as shown in Table 12 and Table 13.

Table 12. Programming the AD5412 Data Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
12-bit data-word												X	X	X	X

Table 13. Programming the AD5422 Data Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
16-bit data-word															

CONTROL REGISTER

The control register is addressed by setting the address word of the input shift register to 0x55. The data to be written to the control register is entered in the D15 to D0 positions, as shown in Table 14. The control register functions are shown in Table 15.

Table 14. Programming the Control Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CLRSEL	OVRRNG	REXT	OUTEN	SR clock				SR step			SREN	DCEN	R2	R1	R0

Table 15. Control Register Functions

Option	Description
CLRSEL	See Table 21 for a description of the CLRSEL operation.
OVRRNG	Setting this bit increases the voltage output range by 10% (see the AD5412/AD5422 Features section).
REXT	Setting this bit selects the external current setting resistor (see the AD5412/AD5422 Features section).
OUTEN	Output enable. This bit must be set to enable the outputs. The range bits select which output is functional.
SR clock	Digital slew rate control (see the AD5412/AD5422 Features section).
SR step	Digital slew rate control (see the AD5412/AD5422 Features section).
SREN	Digital slew rate control enable.
DCEN	Daisy chain enable.
R2, R1, R0	Output range select (see Table 16).

Table 16. Output Range Options

R2	R1	R0	Output Range Selected
0	0	0	0 V to 5 V voltage range
0	0	1	0 V to 10 V voltage range
0	1	0	±5 V voltage range
0	1	1	±10 V voltage range
1	0	1	4 mA to 20 mA current range
1	1	0	0 mA to 20 mA current range
1	1	1	0 mA to 24 mA current range

RESET REGISTER

The reset register is addressed by setting the address word of the input shift register to 0x56. The data to be written to the reset register is entered in the D0 position as shown in Table 17. The reset register options are shown in Table 17 and Table 18.

Table 17. Programming the Reset Register

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reserved															Reset

Table 18. Reset Register Functions

Option	Description
Reset	Setting this bit performs a reset operation, restoring the AD5412/AD5422 to its power-on state.

STATUS REGISTER

The status register is a read-only register. The status register functionality is shown in Table 19 and Table 20.

Table 19. Decoding the Status Register

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reserved													I_{OUT} fault	Slew active	Over temp

Table 20. Status Register Functions

Option	Description
I_{OUT} Fault	This bit is set if a fault is detected on the I_{OUT} pin.
Slew Active	This bit is set while the output value is slewing (slew rate control enabled).
Over Temp	This bit is set if the AD5412/AD5422 core temperature exceeds ~150°C.

Table 24. Programmable Slew Time Values in Seconds for a Full-Scale Change on Any Output Range

Update Clock Frequency (Hz)	Step Size (LSB)							
	1	**2**	**4**	**8**	**16**	**32**	**64**	**128**
257,730	0.25	0.13	0.06	0.03	0.016	0.008	0.004	0.0020
198,410	0.33	0.17	0.08	0.04	0.021	0.010	0.005	0.0026
152,440	0.43	0.21	0.11	0.05	0.027	0.013	0.007	0.0034
131,580	0.50	0.25	0.12	0.06	0.031	0.016	0.008	0.0039
115,740	0.57	0.28	0.14	0.07	0.035	0.018	0.009	0.0044
69,440	0.9	0.47	0.24	0.12	0.06	0.03	0.015	0.007
37,590	1.7	0.87	0.44	0.22	0.11	0.05	0.03	0.014
25,770	2.5	1.3	0.64	0.32	0.16	0.08	0.04	0.020
20,160	3.3	1.6	0.81	0.41	0.20	0.10	0.05	0.025
16,030	4.1	2.0	1.0	0.51	0.26	0.13	0.06	0.03
10,290	6.4	3.2	1.6	0.80	0.40	0.20	0.10	0.05
8280	7.9	4.0	2.0	1.0	0.49	0.25	0.12	0.06
6900	9.5	4.8	2.4	1.2	0.59	0.30	0.15	0.07
5530	12	5.9	3.0	1.5	0.74	0.37	0.19	0.09
4240	15	7.7	3.9	1.9	0.97	0.48	0.24	0.12
3300	20	9.9	5.0	2.5	1.24	0.62	0.31	0.16

APPLICATIONS INFORMATION

DRIVING INDUCTIVE LOADS

When driving inductive or poorly defined loads, connect a 0.01 µF capacitor between I_{OUT} and GND. This ensures stability with loads above 50 mH. There is no maximum capacitance limit. The capacitive component of the load may cause slower settling. The digital slew rate control feature may also prove useful in this situation.

TRANSIENT VOLTAGE PROTECTION

The AD5412/AD5422 contain ESD protection diodes that prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. To protect the AD5412/AD5422 from excessively high voltage transients, external power diodes and a surge current limiting resistor are required, as shown in Figure 73. The constraint on the resistor value is that, during normal operation, the output level at I_{OUT} must remain within its voltage compliance limit of AV_{DD} – 2.5 V, and the two protection diodes and resistor must have appropriate power ratings. Further protection can be provided with transient voltage suppressors or transorbs; these are available as both unidirectional suppressors (protect against positive high voltage transients) and bidirectional suppressors (protect against both positive and negative high voltage transients) and are available in a wide range of standoff and breakdown voltage ratings. It is recommended that all field connected nodes be protected.

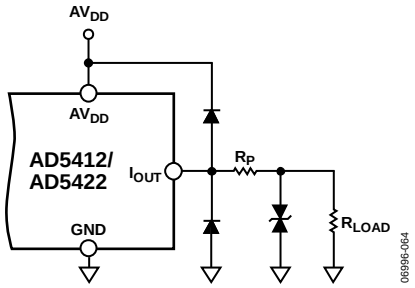


Figure 73. Output Transient Voltage Protection

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. The *i*Coupler® products from Analog Devices, Inc., provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5412/AD5422 makes the parts ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 74 shows a 4-channel isolated interface to the AD5412/AD5422 using an ADuM1400. For further information, visit http://www.analog.com/icouplers.

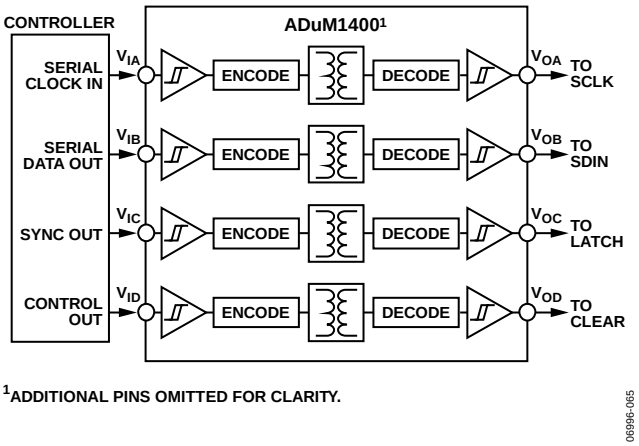


Figure 74. Isolated Interface

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5412/AD5422 is via a serial bus that uses a protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire minimum interface consisting of a clock signal, a data signal, and a latch signal. The AD5412/AD5422 require a 24-bit data-word with data valid on the rising edge of SCLK.

For all interfaces, the DAC output update is initiated on the rising edge of LATCH. The contents of the registers can be read using the readback function.

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. Design the printed circuit board (PCB) on which the AD5412/AD5422 is mounted so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5412/AD5422 is in a system where multiple devices require an analog ground-to-digital ground connection, make the connection at one point only. Establish the star ground point as close as possible to the device.

The AD5412/AD5422 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD5412/AD5422 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with a digital ground to avoid radiating noise to other parts of the board. Never run these near the reference inputs. A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between them (this is not required on a multilayer board that has a separate ground plane, but separating the lines helps). It is essential to minimize noise on the REFIN line because it couples through to the DAC output.

Avoid crossover of digital and analog signals. Traces on opposite sides of the PCB should run at right angles to each other. This reduces the effects of feed through the board. A microstrip technique is by far the best but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane, and signal traces are placed on the solder side.

THERMAL AND SUPPLY CONSIDERATIONS

The AD5412/AD5422 are designed to operate at a maximum junction temperature of 125°C. It is important that the devices not be operated under conditions that cause the junction temperature to exceed this value. Excessive junction temperature can occur if the AD5412/AD5422 are operated from the maximum AV_{DD} while driving the maximum current (24 mA) directly to ground. In this case, control the ambient temperature or reduce AV_{DD}. The conditions depend on the device package.

At the maximum ambient temperature of 85°C, the 24-lead TSSOP package can dissipate 950 mW, and the 40-lead LFCSP package can dissipate 1.42 W.

To ensure that the junction temperature does not exceed 125°C while driving the maximum current of 24 mA directly into ground (also adding an on-chip current of 3 mA), reduce AV_{DD} from the maximum rating to ensure that the package is not required to dissipate more power than previously stated (see Table 25, Figure 75, and Figure 76).

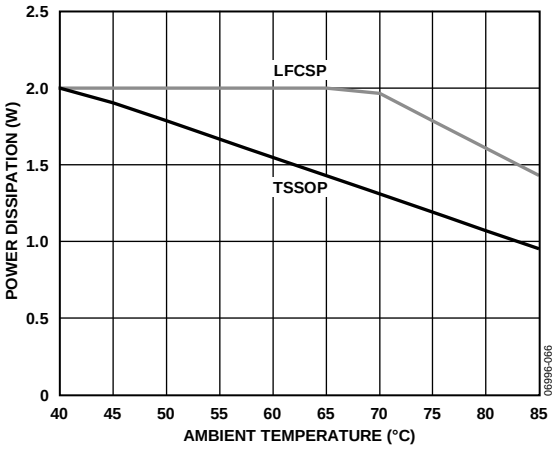


Figure 75. Maximum Power Dissipation vs. Ambient Temperature

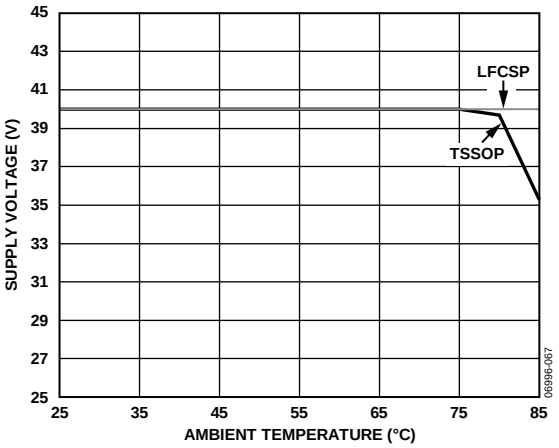
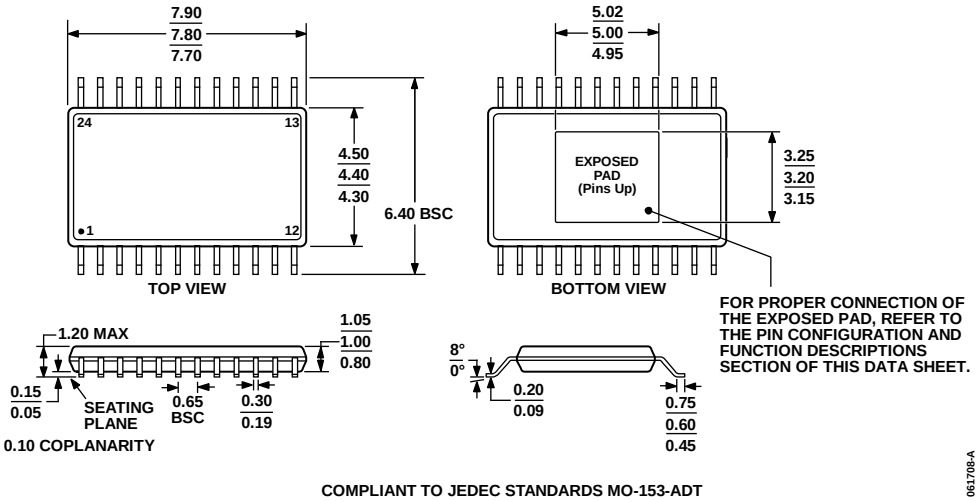


Figure 76. Maximum Supply Voltage vs. Ambient Temperature

Table 25. Thermal and Supply Considerations for Each Package

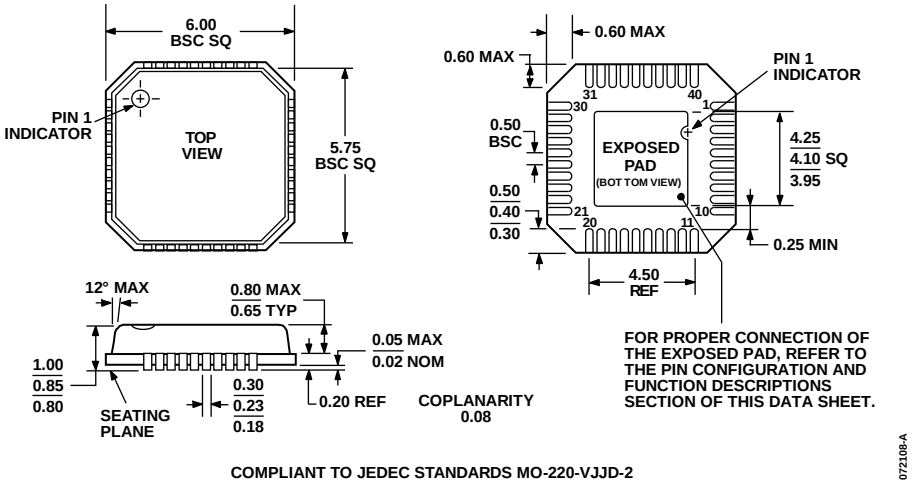
Considerations	TSSOP	LFCSP
Maximum Allowed Power Dissipation When Operating at an Ambient Temperature of 85°C	$\frac{T_J\ max - T_A}{\theta_{JA}} = \frac{125 - 85}{42} = 950\ \text{mW}$	$\frac{T_J\ max - T_A}{\theta_{JA}} = \frac{125 - 85}{28} = 1.42\ \text{W}$
Maximum Allowed Ambient Temperature When Operating from a Supply of 40 V and Driving 24 mA Directly to Ground	$T_J\ max - P_D \times \theta_{JA} = 125 - (40 \times 0.028) \times 42 = 78°\text{C}$	$T_J\ max - P_D \times \theta_{JA} = 125 - (40 \times 0.028) \times 28 = 94°\text{C}$
Maximum Allowed Supply Voltage When Operating at an Ambient Temperature of 85°C and Driving 24 mA Directly to Ground	$\frac{T_J\ max - T_A}{AI_{DD} \times \theta_{JA}} = \frac{125 - 85}{0.028 \times 42} = 34\ \text{V}$	$\frac{T_J\ max - T_A}{AI_{DD} \times \theta_{JA}} = \frac{125 - 85}{0.028 \times 28} = 51\ \text{V}$

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-ADT

Figure 78. 24-Lead Thin Shrink Small Outline Package, Exposed Pad [TSSOP_EP]
(RE-24)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-2

Figure 79. 40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
6 mm × 6 mm Body, Very Thin Quad
(CP-40-1)
Dimensions shown in millimeters

NOTES