

Letter explaining changes between AD9122 R1 and R2

The AD9122 is dual-channel, 16-bit DACs (digital-to-analog converters) that support the high data rates and complex modulation schemes required by customers using advanced multi-carrier wireless and broadband communications equipment.

In order to improve the AD9122 AC performance, a die revision, R2, has been implemented to the part. This change, its introduction schedule and its implication for the customer are fully documented in the PCN #10_0010 and repeated in Table 1. AD9122 R2 will be available for customers to test in their applications by the middle of January 2010 and released Early April 2010. AD9122 R2 samples can be ordered before its release under the part number AD9122AXCPZ.

Although with this R2 die revision, customers will only see an improvement in the AD9122 performance and behavior, we would like to highlight a critical element of this PCN:

- In our preliminary AD9122 datasheet, pins 71 and 72 were defined as no connects while the release AD9122 datasheet defines these pins as CVDD (1.8V). Although, both configuration were acceptable with AD9122 R1, this change is imperative for AD9122 R2 as the part will not function properly otherwise.

In case customers cannot implement this PCB configuration for the AD9122 when the R2 is introduced in production (April 12th 2010), they could contact us to buy AD9122 R1 for a limited time under the special part number AD80255. This will allow customers to temporarily continue production with the old PCB configuration before they can switch to the new implementation and use AD9122 R2.





Etienne Moulin
Product Manager
Phone: 781 937 1910
Fax: 781 937 1069
etienne.moulin@analog.com

Table 1: Changes between AD9122 R1 and R2

	AD9122 R1	AD9122 R2
Samples		01/18/2010
Release	Now	04/01/2010
Pin 71 - 72	CVDD (1.8V)	CVDD (1.8V)
IOVDD	1.8 to 2.5V+/-10%.	1.8V to 3.3V+/-10%.
Register 0x0B, Bit 5	Enable VCO	Inactive bit. The VCO is now enabled when the PLL is enabled.
DCI Delay Register 0x16, Bits[1:0]	None	4 options, see Table 2
Version ID: Register 0x7F	0x04	0x0C

Table 2: DCI Delay setting in New AD9122

Delay Setting	0	1	2	3
DCI Delay (ns)	0.35	0.59	0.8	0.925
Setup (ns)	-0.05	-0.22	-0.37	-0.47
Hold (ns)	0.65	0.96	1.23	1.38
KOW (ns)	0.60	0.74	0.86	0.91

<p>AD9122 REV1 possible package branding Part Order #: AD80255BCPZ</p>	<p>AD9122 REV2 possible package branding Part order #: AD9122AXCPZ before 4/12/2010 AD9122BCPZ after 4/12/2010</p>
<p>AD9122 released part prior to Jan 2010</p>  <p>Any date code smaller than #1001 is REV1</p>	<p>AD9122 un-released part before 4/12/2010</p>  <p>AD9122AXCPZ specifies that part is REV2</p>
<p>AD9122 released part with Special part# AD80255</p>  <p>AD80255 specifies that AD9122 is REV1</p>	<p>AD9122 released part after 4/12/2010</p>  <p>Any date code larger than #1001 is REV2</p>