



Reliability Report

Report Title: ADL5372 Die Revision (R2)

Report Number: 8037

Revision: A

Date: 1 June 2009

Summary

This report documents the successful completion of the reliability qualification requirements for release of the ADL5372 R2 die revision to improve ESD performance. The ADL5372 is a member of the fixed-gain quadrature modulator (F-MOD) family designed for use from 1500 MHz to 2500 MHz.

Table 1: ADL5372 Product Characteristics

Die/Fab

Die ID	ADL5372 R2
Die Size (mm)	1.89 x 1.58
Wafer Fabrication Site	ADI-Wilmington
Wafer Fabrication Process	XFCB3
Transistor Count	110
Passivation Layer	doped-oxide/SiN
Bond Pad Metal Composition	AlCu

Package/Assembly

Available Package	24-LFCSP
Body Size (mm)	4.00 x 4.00 x 0.85
Assembly Location	Amkor-K
Molding Compound	Sumitomo G700
Wire Type	Gold
Wire Diameter (mils)	1.00
Die Attach	Ablestik 8290
Lead Frame Material	Copper
Lead Finish	Tin Plate
Moisture Sensitivity Level	3
Maximum Peak Reflow Temperature (°C)	260

Description / Results of Tests Performed

Tables 2 and 3 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 2: Package Qualification Test Results

Test Name	Specification	Conditions	Device	Package	Lot #	Sample Size	Qty. Failures
Autoclave (AC) ¹	JESD22-A102	121°C, 100%RH, 2atm, 96 hours	AD8295	16-LFCSP	Q7327.6	77	0
					Q7327.7	77	0
					Q7327.8	77	0
			ADG758	20-LFCSP	R86307.1	45	0
					ADG936	AA89032.1	45
			ADL5570	16-LFCSP	Q6311.1	77	0
			ADP5588	24-LFCSP	Q7272.2	77	0
					Q7272.3	77	0
					Q7272.4	77	0
Highly Accelerated Temperature & Humidity Stress (HAST) ¹	JESD22-A110	130°C, 85%RH, 2atm, Biased 96 hours	AD8557	16-LFCSP	Q6117.7	45	0
					Q6117.8	45	0
			ADF4350	32-LFCSP	f161375.17	45	0
					f161485.10	45	0
					Q6725.17	45	0
			ADM8830	20-LFCSP	AA88878.1	45	0
			ADL5355	20-LFCSP	Q7623.12	45	0
					Q7623.17	45	0
					Q7623.3	45	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1000 hours	AD7147	24-LFCSP	f160106.5	72	0
					f160345.3	76	0
			ADL5355	20-LFCSP	Q7623.11	77	0
			ADL5570	16-LFCSP	Q6311.7	77	0
Temperature Cycling (TC) ¹	JESD22-A104	-65°C / +150°C, 500 cycles	ADA4937-2	24-LFCSP	Q6847.7	77	0
					Q6847.8	77	0
					Q6847.9	77	0
					Q6866.7	77	0
					Q6866.8	77	0
			ADG936	20-LFCSP	AA89033.1	45	0
					ADP5020	Q7578.1	77
			Q7578.2	77	0		

¹ These Samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following:

- Bake: 24 hrs @ 125°C
- Soak: Unbiased Soak: 192 hrs @ 30°C
- Reflow: 3 passes through an oven with a peak temperature of 260°C

Table 3: Process Qualification Test Results

Test Name	Specification	Conditions	Device	Fab Process	Lot #	Sample Size	Qty. Failures
Early Life Failure Rate (ELFR)	MIL-STD-883, Method 1015	T _A = 125°C, Biased, 48 hours	AD8344	XFCB3	f157442.4	100	0
					Q4817.1	150	0
					Q4817.2	150	0
					Q4817.3	150	0
			ADCMP572		AA88718.1	80	0
					AA88718.2	80	0
					AA88718.3	80	0
					AA88718.4	80	0
					AA88718.5	80	0
					AA88718.6	50	0
					AA88947.1	450	0
					AA88947.2	83	0
					AA88947.3	83	0
					AA88947.4	83	0
					AA88947.5	83	0
					AA88947.6	83	0
					R86212.1	85	0
					R86212.2	85	0
					R86212.3	85	0
					R86212.4	85	0
			R86212.5		85	0	
			R86212.6		85	0	
			R86360.1		80	0	
R86360.2	80	0					
R86360.3	80	0					
R86360.4	80	0					
R86360.5	33	0					
High Temperature Operating Life (HTOL)	JESD22-A108	125°C < T _j < 135°C, Biased 1,000 hours	ADATE209	XFCB3	Q6859.3	45	0
		150°C < T _j < 175°C, Biased 500 hours	ADA4857-1		Q6859.4	45	0
					Q6859.5	45	0
					Q6676.11	77	0
			Q6676.12		77	0	
			Q6676.3		77	0	
			ADA4938-1		Q6422.7	77	0
					Q6422.8	77	0
					Q6422.9	77	0
			AD8318		Q7048.3	77	0
		Q7048.4			77	0	

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

ESD Test Results

The results of ESD testing are summarized in the ESD Results Table. ADI measures ESD results using stringent test procedures based on the specifications listed in Table 4. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link at <http://www.analog.com>).

Table 4: ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	24-LFCSP	ANSI/ESD STM5.3.1-1999	1 Ω , Cpkg	\pm 750V	\pm 1000V	C5
HBM		ANSI/ESD STM5.1-2007	1.5k Ω , 100pF	\pm 3000V	NA	2

Approvals

Reliability Engineer: Kevin Manning

This report has been approved by electronic means (4.0)

Additional Information

Data sheets and other additional information are available on Analog Devices' web site:
<http://www.analog.com>