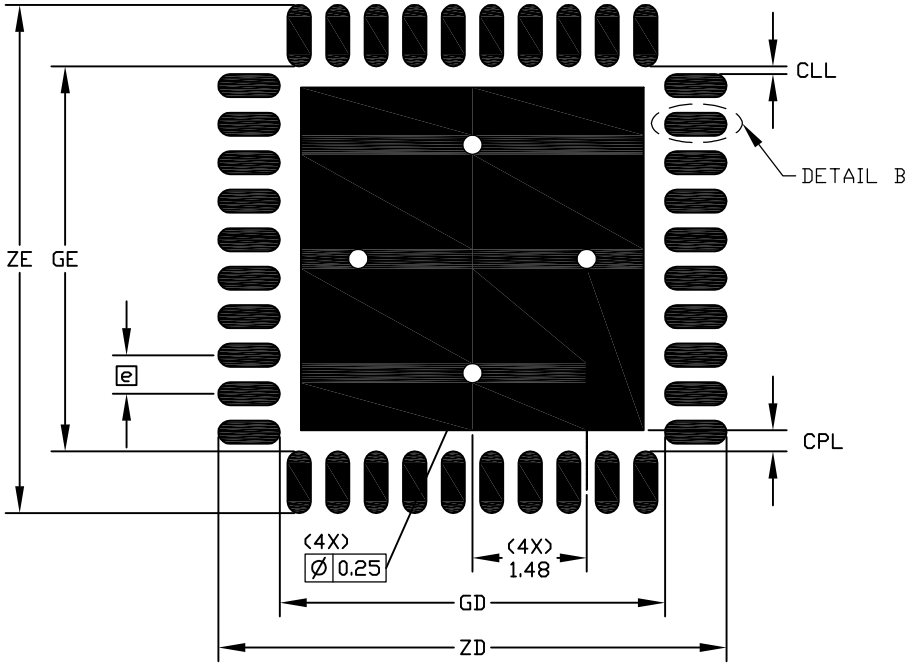
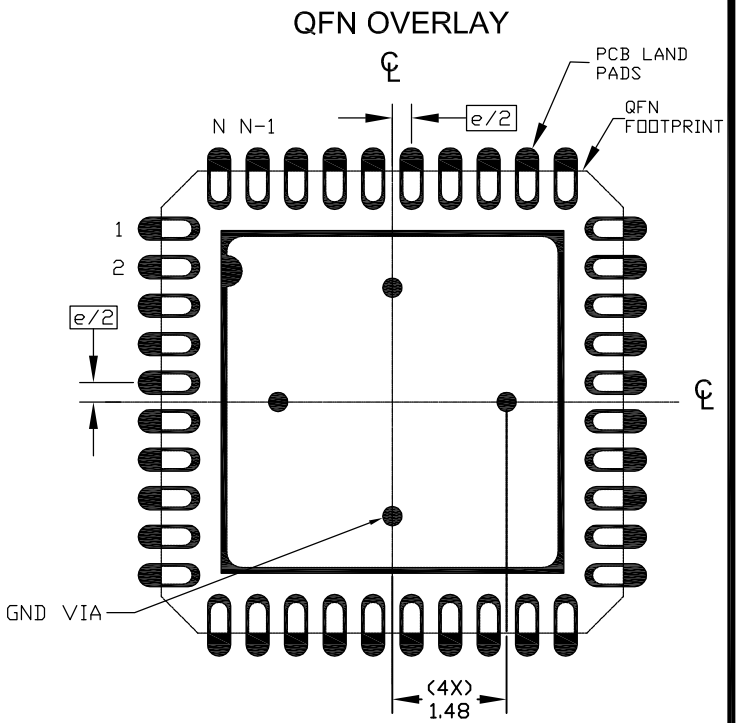
RECOMMENDED LAND PATTERN



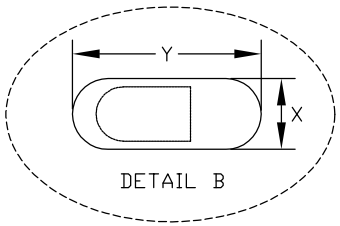
QFN OVERLAY



NOTES:

1. REFERENCE PKG. OUTLINE: 21-1010
2. LAND PATTERN COMPLIES TO: IPC7351A.
3. TOLERANCE: +/- 0.02 MM.
4. ALL DIMENSIONS APPLY TO PBFREE (+) PKG. CODE ONLY.
5. ALL DIMENSIONS IN MM.
6. ALL FOUR GND VIAS MUST BE CONNECTED TO GND (APPROXIMATE LOCATIONS SHOWN).
7. NO-CLEAN SOLDER PASTE MUST BE USED TO AVOID TRAPPED RESIDUES UNDER THE DEVICE.
8. THE STENCIL USED FOR APPLYING NO-CLEAN PASTE MUST BE 5 MILS THICK OR LESS. THIS WILL ENSURE THAT THE CORRECT AMOUNT OF SOLDER IS APPLIED TO THE PIN CONNECTIONS.

= GND VIA



	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
CLL		0.10 REF			0.004 REF	
CPL		0.28 REF			0.011 REF	
e		0.50 BSC			0.020 BSC	
GD		5.00 REF			0.197 REF	
GE		5.00 REF			0.197 REF	
N		40 PINS			40 PINS	
X		0.30 TYP			0.012 TYP	
Y		0.80 TYP			0.031 TYP	
ZD		6.60 REF			0.260 REF	
ZE		6.60 REF			0.260 REF	

—DRAWING NOT TO SCALE—

maxim integrated™

This document (including dimensions, notes & specs) is a recommendaton based on typical circuit board manufacturing parameters. Since land pattern design depend on many factors unknown to Maxim (eg. user's board manufacturing specs), user must determine suitability for use.
This document is subject to change without notice.
Contact technical support at http://www.maximintegrated.com/support for further questions.

TITLE:
PACKAGE LAND PATTERN,
[G4066+3] PUNCH QFN

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	90-0514	A	1/1