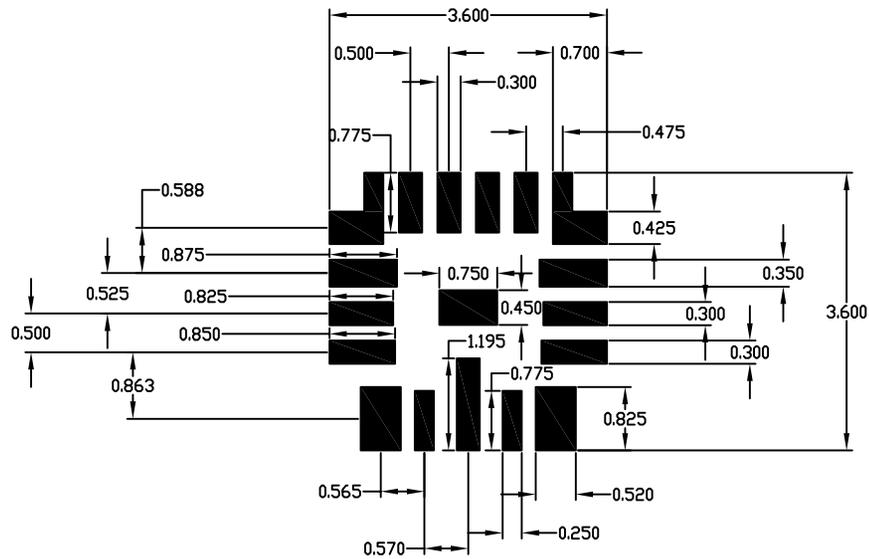




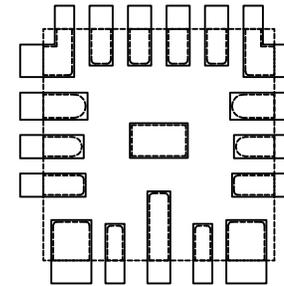
**DOCUMENT TYPE:** PLP  
**DOCUMENT ID #:** 90-100271  
**REVISION:** A-000  
**DOCUMENT TITLE:** PACKAGE LAND PATTERN, [F1733F+1F / F1733  
**EFFECTIVE DATE:** 07/29/2024  
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**CHANGE NUMBER:** 1213824  
**ORIGINATOR:** Aurelio Giron Jr.

**REASON FOR CHANGE:**  
INITIAL RELEASE

## RECOMMENDED LAND PATTERN



## PACKAGE OVERLAY



### NOTES:

1. REFERENCE PKG. OUTLINE: 21-100774 / 21-100775
2. LAND PATTERN COMPLIES TO: IPC7351A.
3. TOLERANCE: +/- 0.02 MM.
4. ALL DIMENSIONS APPLY TO LEADED, PbFREE PACKAGES.
5. ALL DIMENSIONS IN MM.

—DRAWING NOT TO SCALE—



This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depend on many factors unknown to Analog Devices Inc. (eg. user's board manufacturing specs), user must determine suitability for use. This document is subject to change without notice. Contact technical support at <https://www.analog.com/en/support> for further questions.

TITLE: PACKAGE LAND PATTERN, [F1733F+1F / F1733FY+1F] FC2QFN			
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