



Synchronizing systems with a high number of ADCs/DACs

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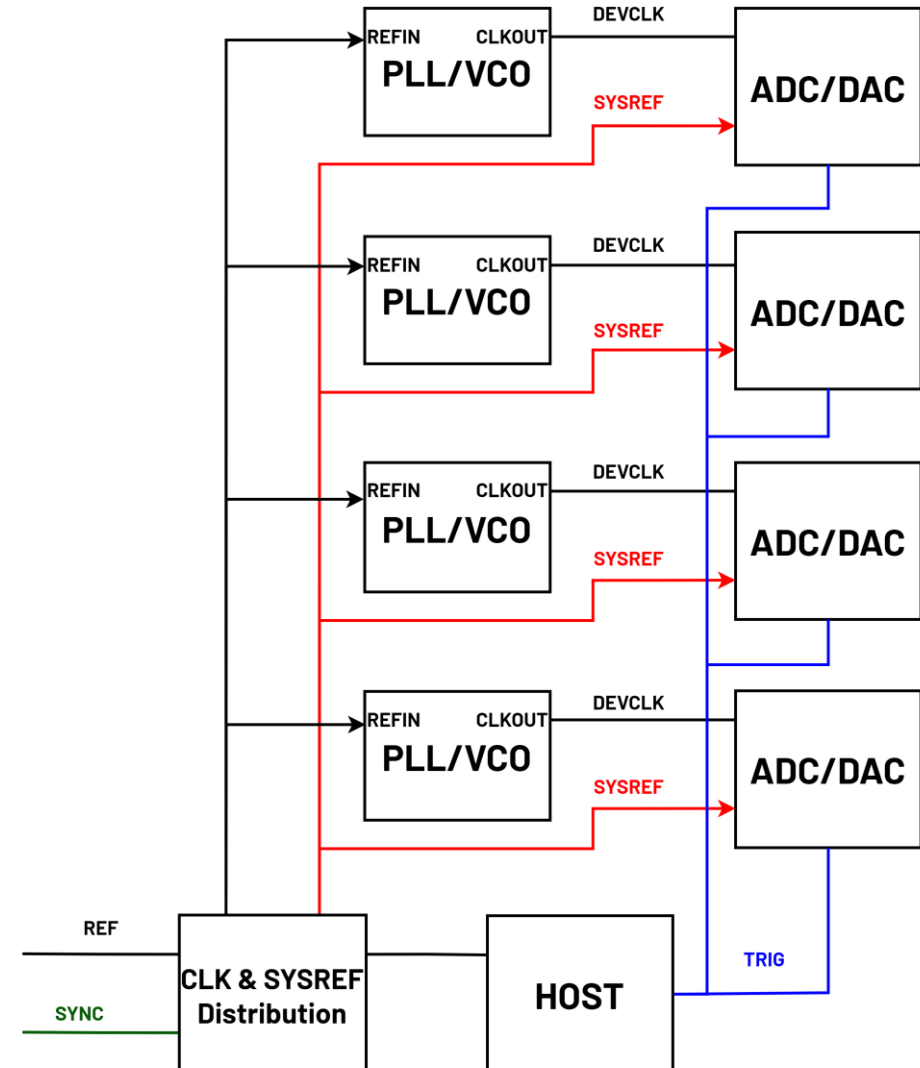
Author/Presenter: Emrecan Gidik, Analog Devices

Synchronization of High Number of ADCs/DACs

Traditional Way

Challenges

- Aligning the references to each PLL/VCO
- Aligning SYSREFs to ADCs/DACs
- Setup/Hold Time Constraints at higher frequencies
- Temperature Drift of each component should be estimated
- Length of each cables and PCB traces should be estimated



Synchronization of High Number of ADCs/DACs

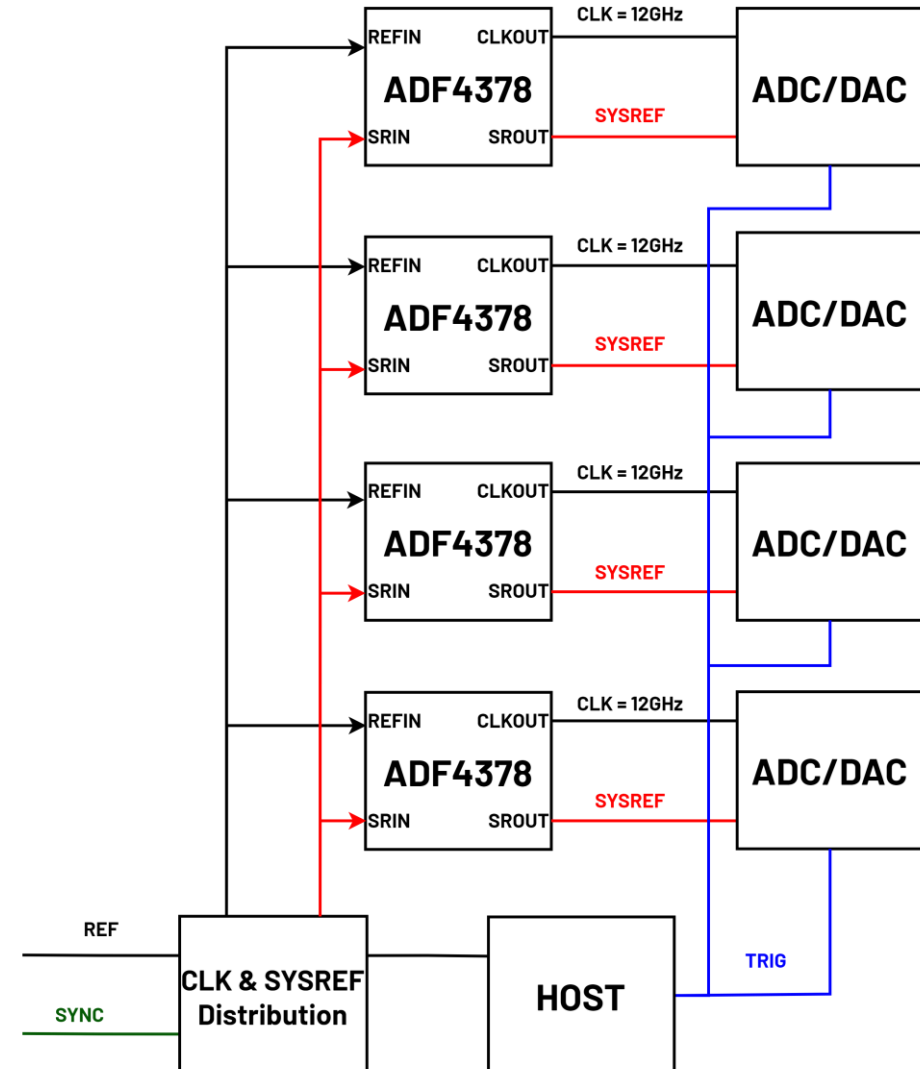
Traditional Way with A Pulse Retimer

ADF4378 Pulse Retimer turns a 12GHz setup/hold timing issue into a <250 MHz timing issue.

Synchronization results within one DEVCLK period
 Low Temp. Coeff. <0.03ps/C

Challenges

- Aligning the references to each PLL/VCO
- Temperature Drift of each component should be estimated for reference distribution
- Length of each cables and PCB traces should be estimated



Synchronization of High Number of ADCs/DACs

Bi-Directional Synchronization With ADF4030

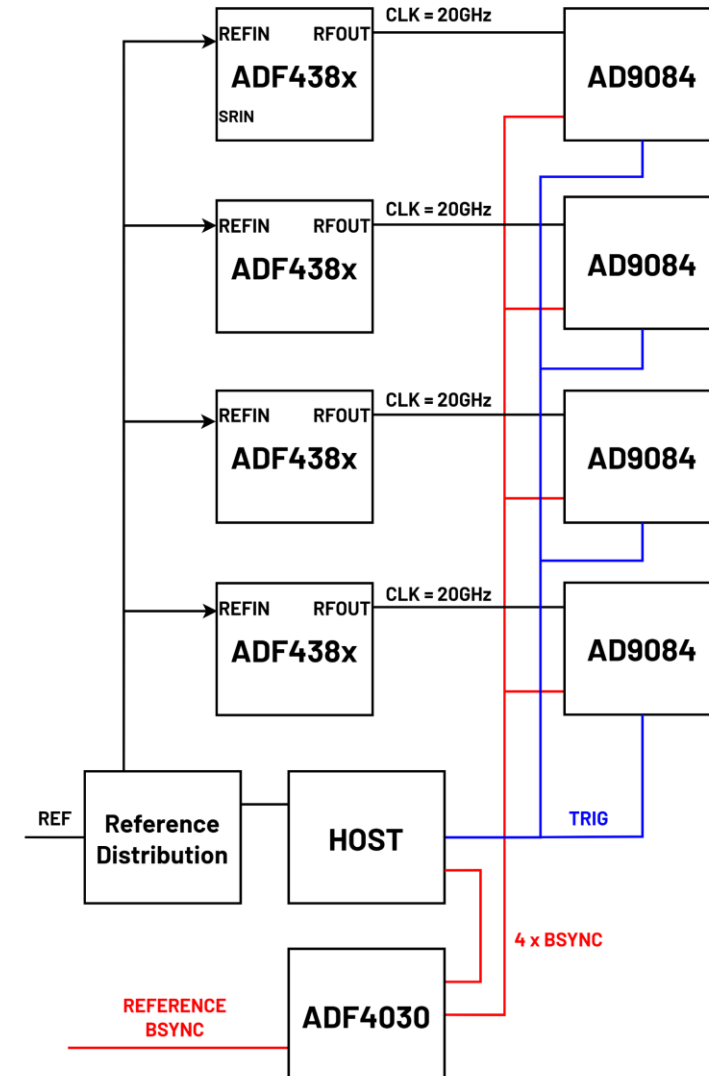
Precision Multi Chip Synchronization using BSYNC and TDC

ADF4382 + ADF4030 + AD9084 Creates an ecosystem

ADF4030 can fix alignment issues, creates well-aligned signals ($< \pm 5$ ps)

AD9084 interfaces with ADF438x to align 20GHZ clock

On -the-fly calibration and temperature compensation on software/firmware level



Bringing ADF4030's Advantages to ADCs/DACs

There are many ADCs and DACs that require SYSREF and they cannot loop it back

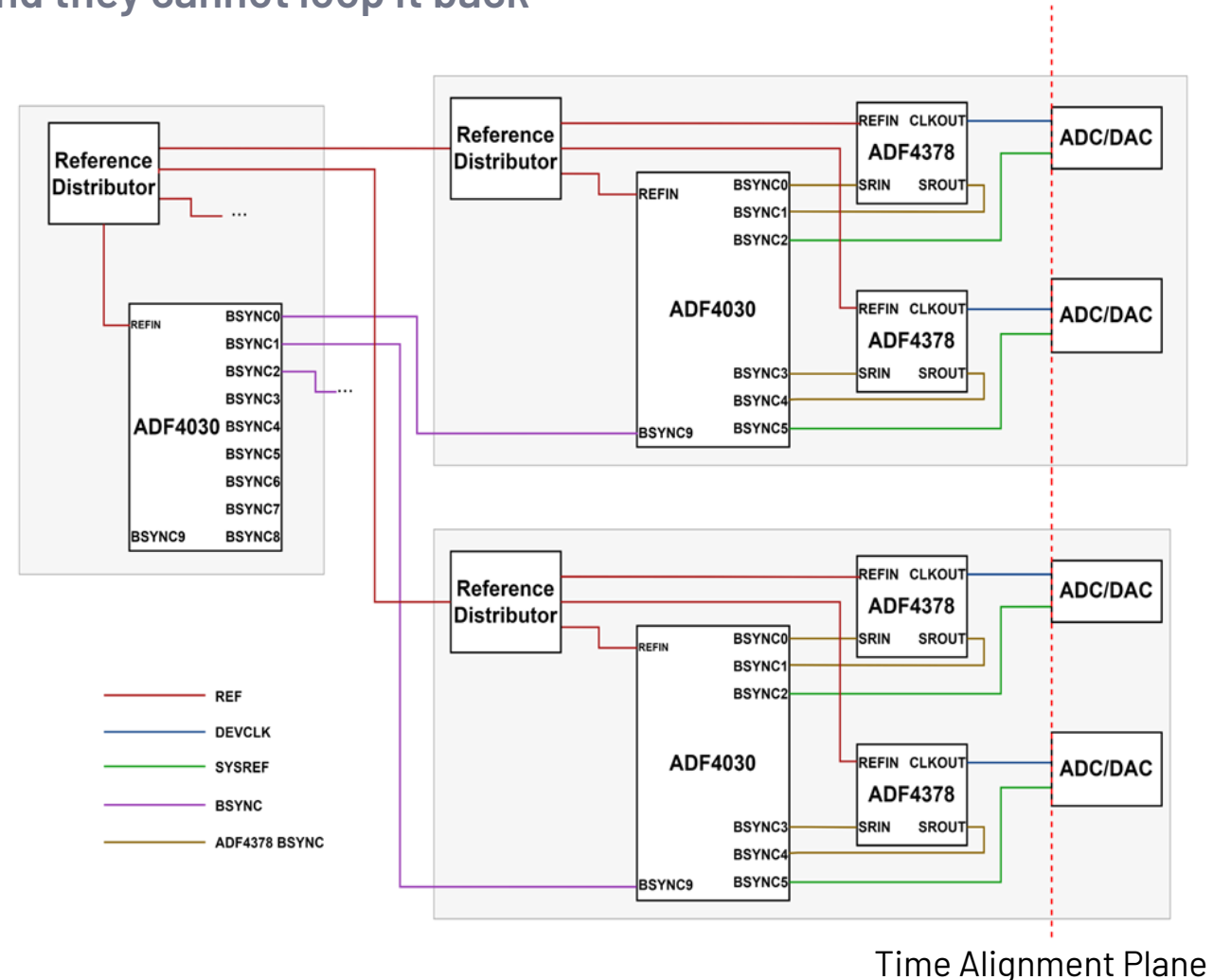
ADF4030 + ADF4378 removes need for reference and SYSREF alignment

Brings on-the-fly calibration and temperature compensation to older MxFE's

Up to 12.8GHz Clock generation

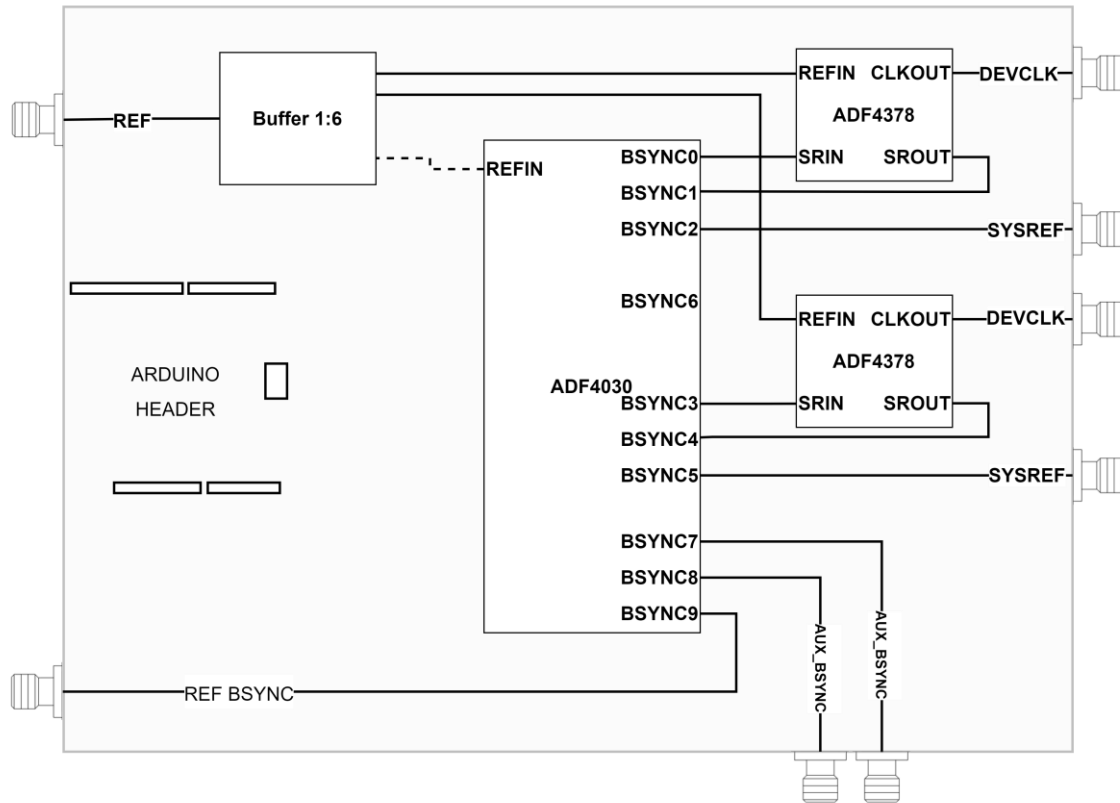
- In-Band 1/f PhN FOM -147dBc/Hz
- In-Band PhN floor = -239dBc/Hz
- Output PhN Floor <-160dBc/Hz @12GHz
- Low Temp. Coeff. <0.03ps/C

Time alignment plane can be shifted to the input of ADCs/DACs by only characterizing the board.



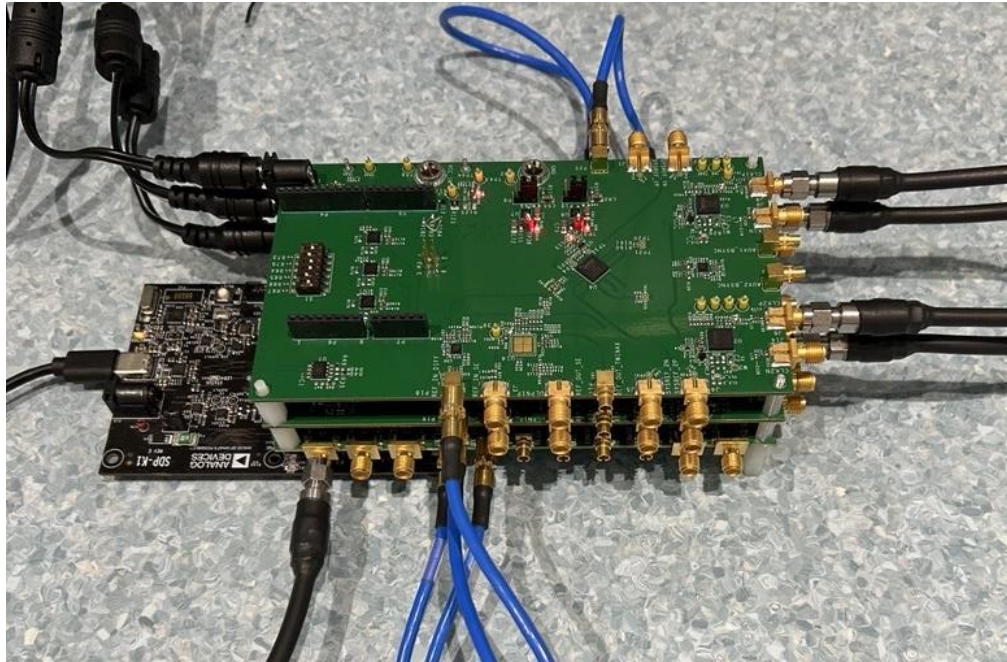
Time Alignment Plane

Demo Circuit Overview

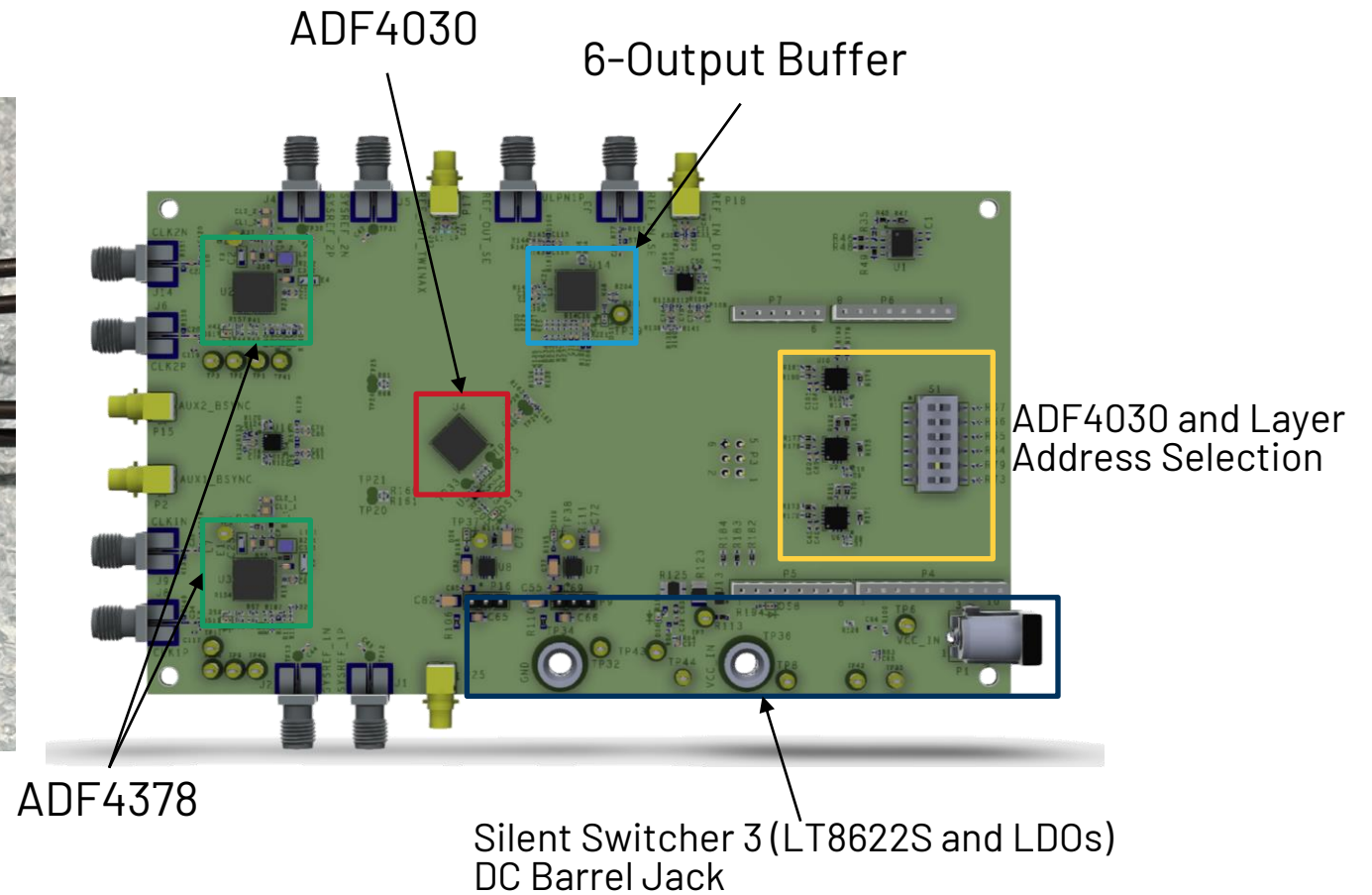


- Features:
 - ADF4378 12.8GHz PLL/VCO with pulse retimer
 - ADF4030 Precision Synchronizer
 - 2 Device clock outputs
 - 2 BSYNC SYSREF outputs
 - 2 Auxiliary BSYNC outputs
 - 1 Reference BSYNC
 - Suitable for cascade or tree architectures
 - Arduino Header

Hardware



Stackable with Arduino Headers
Up to 4 Layer



Key Features and Benefits

Suitable for ADCs/DACs without BSYNC capability

Multi Chip Sync and Sub cycle clock alignment

No need for reference alignment

Superior PLL/VCO Performance

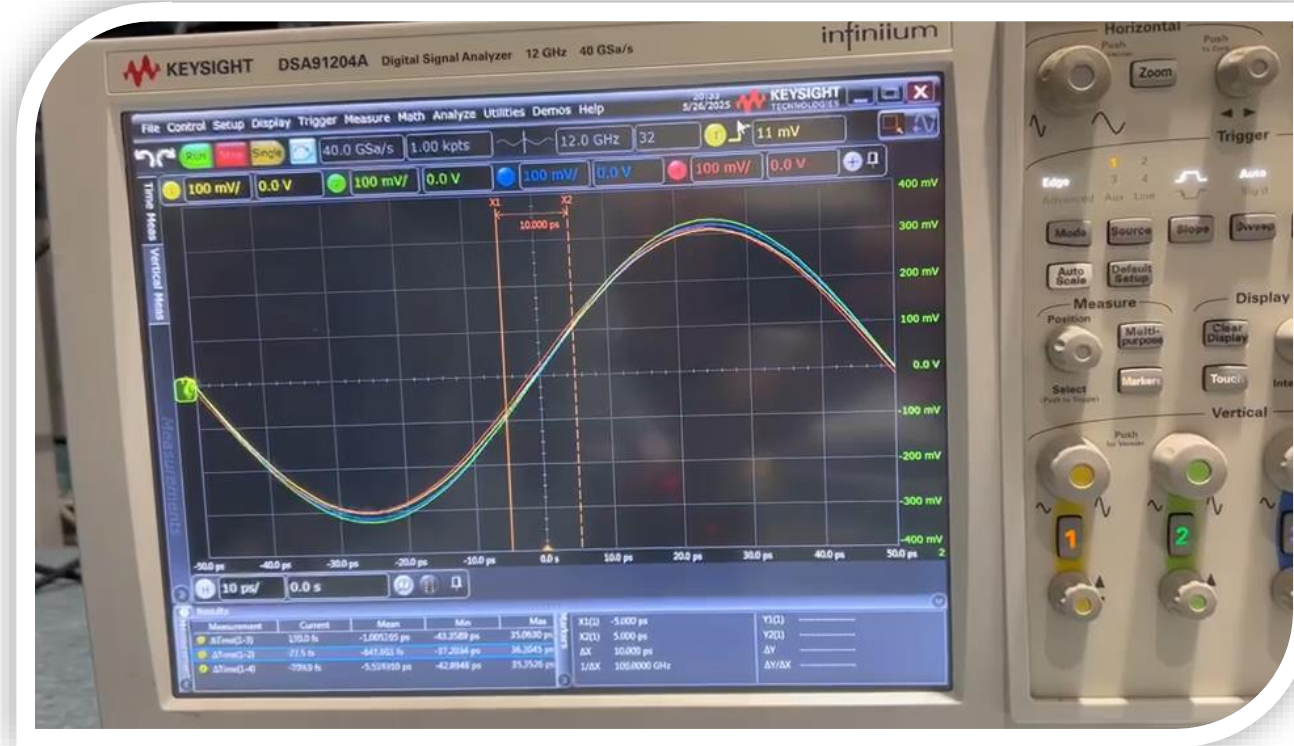
800 MHz – 12.8 GHz Frequency range

18fs wideband integrated RMS Jitter

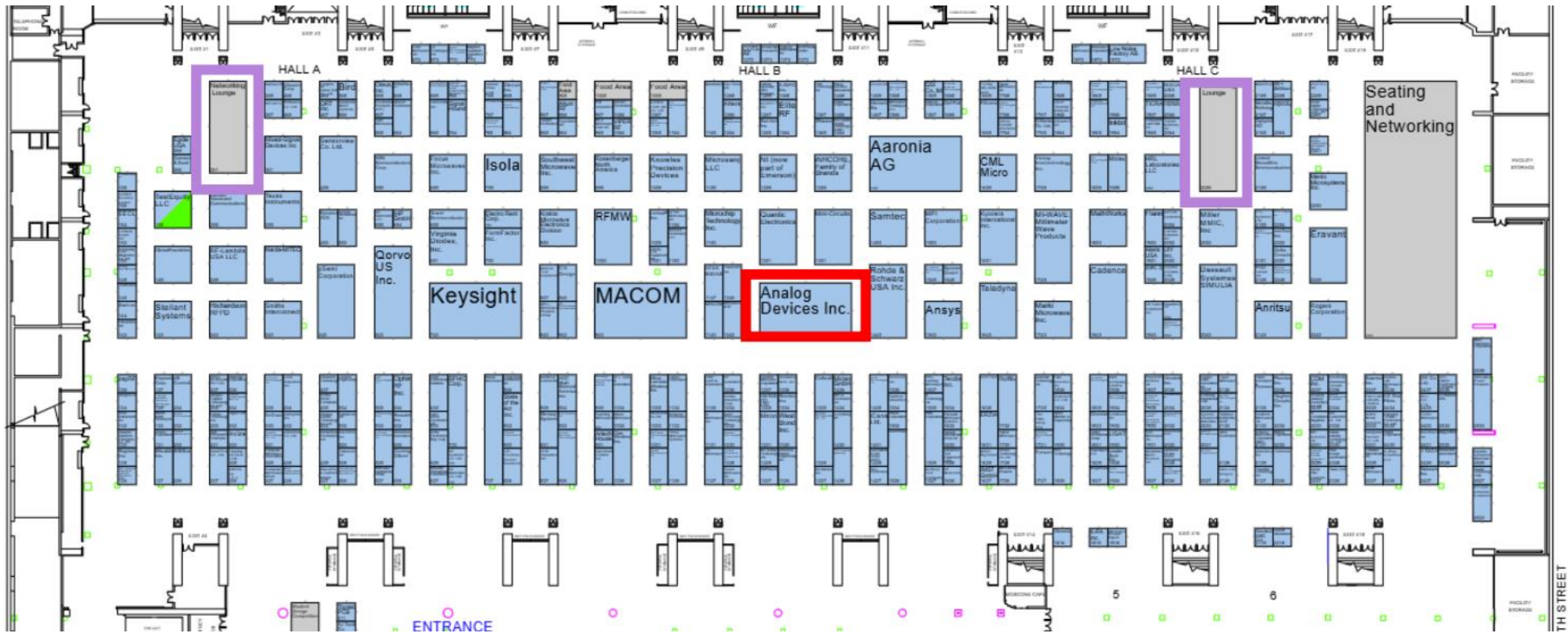
Suitable for both Cascade or Tree architectures

Removes calibration burden from users

Self-calibration and temperature compensation



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