ANALOG DEVICES

X-BAND DIGITAL BEAMFORMING PLATFORM USING HIGH-DENSITY DIRECT RF SAMPLING

ADVANCED DATA CONVERTERS GROUP

IMS2026

analog.com

Apollo MxFE™

8T8R AD9088

8-channel, 10GSPS receive, 16GSPS transmit

RF bandwidth: 0.1GHz to 16GHz

Frequency agile across L-, S-, C-, and X-band

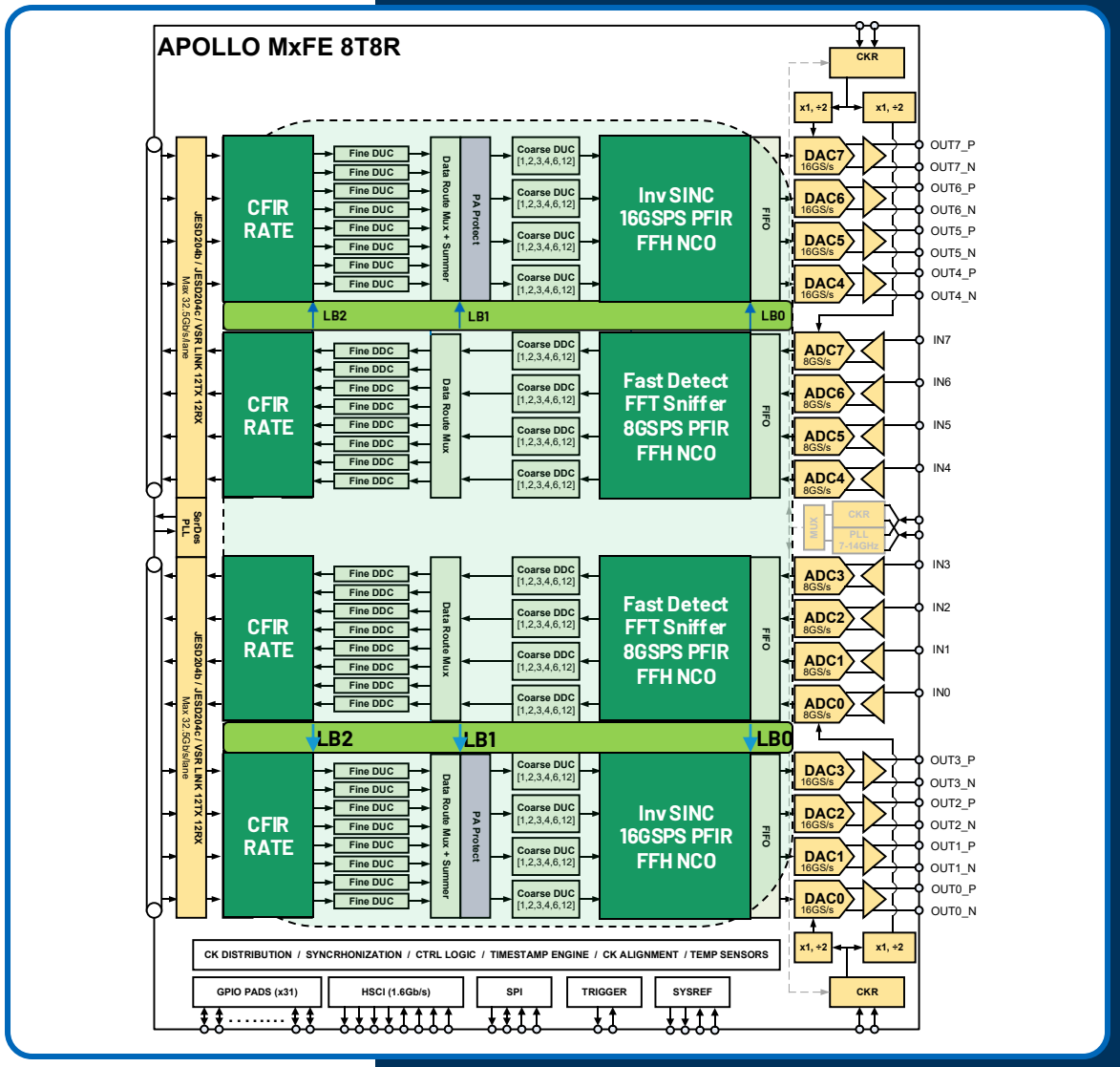
- iBW: ~4GHz/channel in full bandwidth mode (4T4R)
- iBW: ~2GHz/channel with DSP enabled (8T8R)

Programmable and dynamically reconfigurable DSP

- Coarse and fine decimation/interpolation 1× to 768×
- Coarse and fine independent FFH NCOs

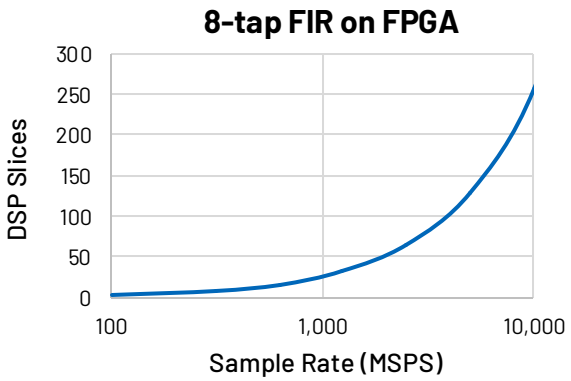
Integrated balun 50Ω single-ended input

Release: CY26Q1



Apollo MxFE™ Hardened DSP

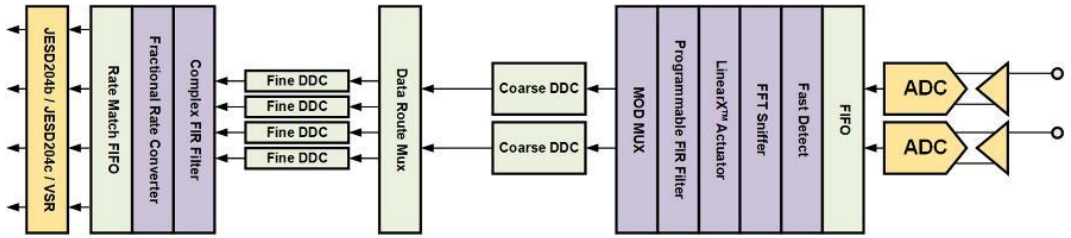
Receive Path



As sample rates increase, more FPGA resources are used for upconversion/downconversion

Narrow-band channelization can consume most of the available DSP slices in multichannel, high-GSPS systems

Apollo MxFE—Receive Signal Path

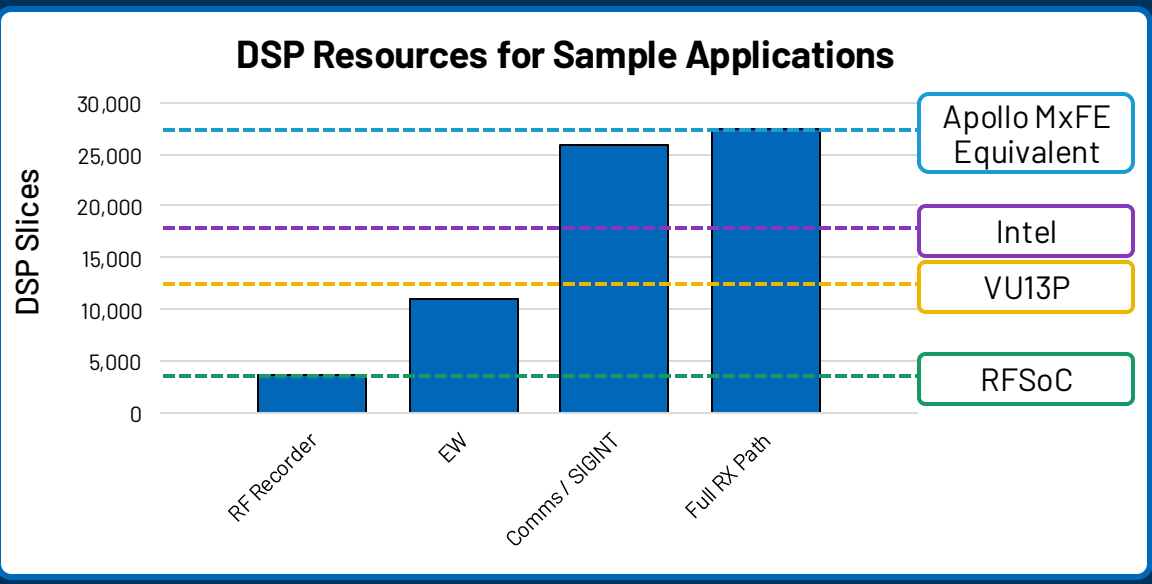


Apollo MxFE offloads compute for common signal processing blocks, saving power, and FPGA resources

Example Design

DSP slices required to implement Apollo MxFE 4T4R hardened IP for 4-channel receive at 20 GSPS in Xilinx Virtex Ultrascale+

Apollo MxFE RX Digital Block	Virtex U+ DSP Slices
FFT Sniffer	1,460
Programmable FIR (PFILT)	2,048
Coarse DDC (CDDC)	3,600
Fast-Hopping Fine DDC (FDDC)	2,864
Complex FIR (CFIR)	1,024
Fractional Sample Rate Converter (FSRC)	16,384
Total	**27,380**



AD9088-MX-SW5/AD9088-TX-SW3

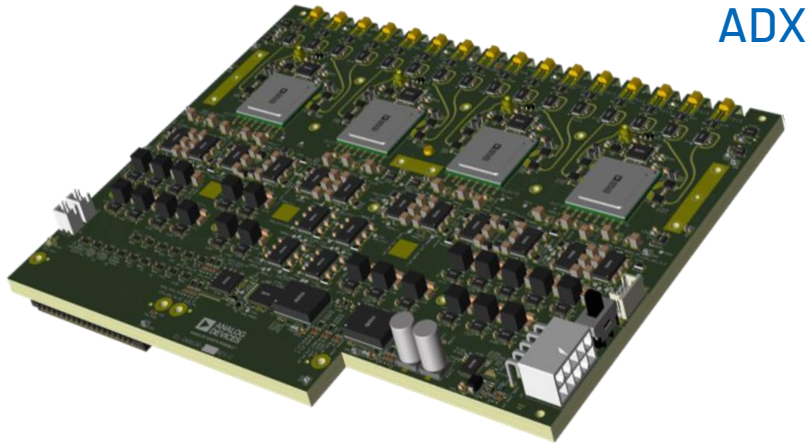
Product Features	AD9088-MX-SW5	AD9088-TX-SW3
Product Variants Offered **MX** = ADC/DAC; **DF**: Differential ADC Input; **SE**: Single-Ended ADC Input; **RX**: ADC Only; **TX**: DAC Only	MX-SE	TX only
Coarse Digital Downconversion/Coarse Digital Upconversion **CDDC/CDUC**	1 per data converter w/ 1, 2, 4, 6, 12 dec/int rates	1 per data converter w/ 1, 2, 4, 6, 12 dec/int rates
Fine Digital Downconversion/Fine Digital Upconversion **FDDC/FDUC**	2 per data converter w/ 1, 2, 4, 6, 16, 32, 64 dec/int rates	2 per data converter w/ 1, 2, 4, 6, 16, 32, 64 dec/int rates
Fine Frequency Hopping Coarse NCO **FFH CNCO**	16× LUTs, 32-bit freq and 32-bit phase tuning steps	16× LUTs, 32-bit freq and 32-bit phase tuning steps
Fine Frequency Hopping Fine NCO **FFH FNCO**	32× LUTs, 32-bit freq and 16-bit phase tuning steps	32× LUTs, 32-bit freq and 16-bit phase tuning steps
RX and TX Programmable FIR Filter **PFILT**	4× LUTs, 32 taps per pair of converters at rate	4× LUTs, 32 taps per pair of converters at rate: Tx only
Complex FIR Filter **CFIR**	2× LUTs, up to 128 taps; 16 non-zero taps sparse mode	2× LUTs, up to 128 taps; 16 non-zero taps sparse mode
Fractional Sample Rate Conversion **FSRC**	1× to 2× fractional dec/int data rate adjust	1× to 2× fractional dec/int data rate adjust
Dynamic Reconfiguration	Up to 4 links remain locked during DSP path changes	Up to 4 links remain locked during DSP path changes
FFT Sniffer and Loopbacks	512 pt FFT; 3 loopbacks; shortest latency 45ns	Not applicable
Active DACs	8	8
1k Book Price ($U.S.) as of February 2026 ECCN	$2,695 (MX-SE) 3A001.a.5.a.3	$2,363 (TX only) 3A001.a.5.b.2

AD9088: MX Concept

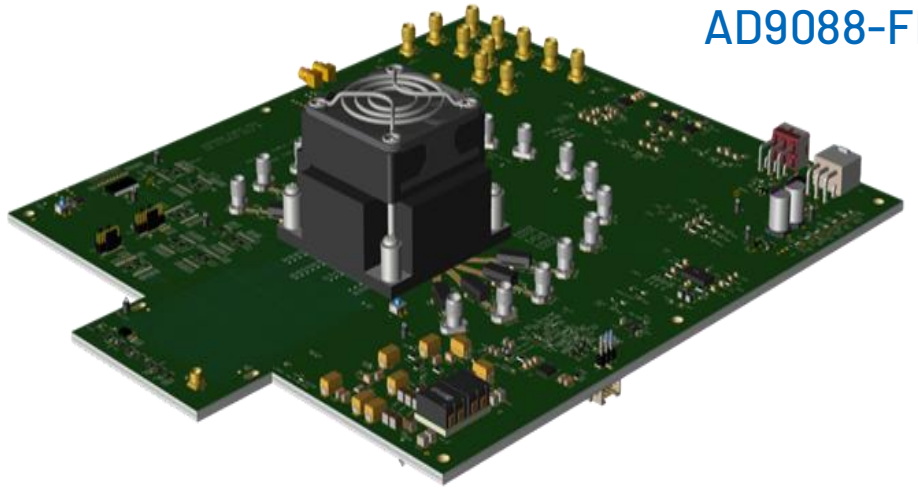
32-Transmit/32-Receive Direct X-Band Sampled Phased Array/Radar/Satcom Development Platform

- **16-transmit/16-receive** already exists: ADXBAND16EBZ, a multichannel, wideband system development platform using Apollo MxFE™ (AD9084)
- The 8-transmit/8-receive variant of the Apollo MxFE (AD9088) extends this concept to a **32-transmit/32-receive** complete development platform
- The AD9088-FMCC-EBZ evaluation board demonstrates this concept, showing calibration and performance

ADXBAND16EBZ



AD9088-FMCC-EBZ



AHEAD OF WHAT'S POSSIBLE

analog.com