



NEXT-GEN HIGH-SPEED ADC PERFORMANCE WITH ON-CHIP DSP ACCELERATION

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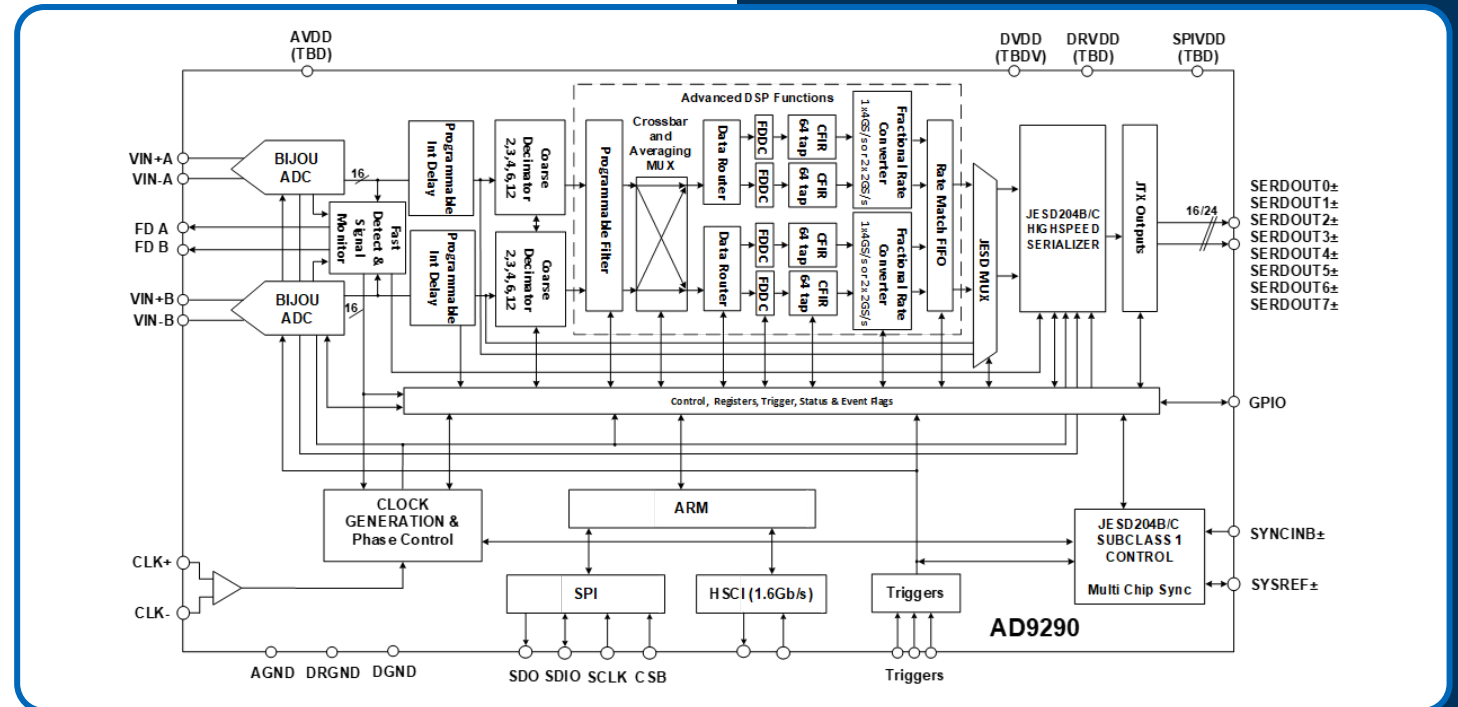
Dual -164dBFS/Hz NSD ADC, Integrated DSP with JESD204B/C

Value Proposition

- NSD as low as -164dBFS/Hz and IMD and SFDR exceeding -85dBFS at full scale
- Flexible configurability enabling common receiver data acquisition platforms
- Highly integrated DSP reducing over PCB footprint and system power

Advanced DSP

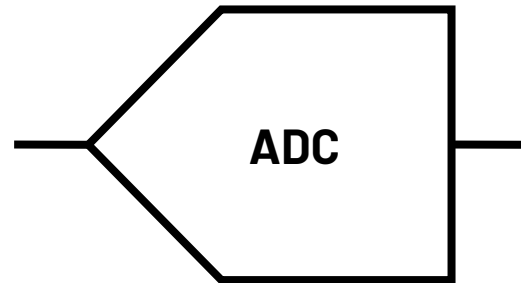
- 2× to 12× coarse decimator
- 64-tap programmable filter; max rate 4Gbps
- Crossbar mux with optional ADC averaging
- 2× to 64× fine DDC—48-bit NCO
- 64-tap complex FIR; max rate 4Gbps option
- Fractional sample rate converter; 1× to 2×



Feature Overview

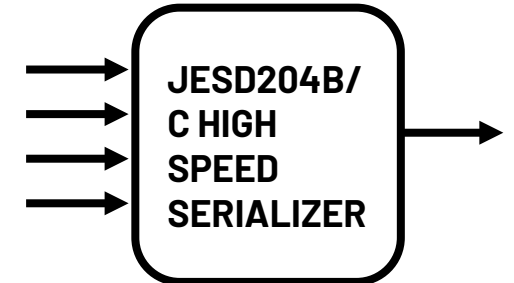
Low-Noise, Wideband ADC

- -164dBFS/Hz
- 10MHz to 1GHz
- 1W/core



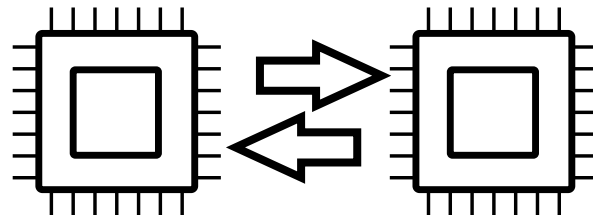
High-Throughput JESD204B/C

- Eight lanes
- Up to 28Gbps
- 260Gbps payload



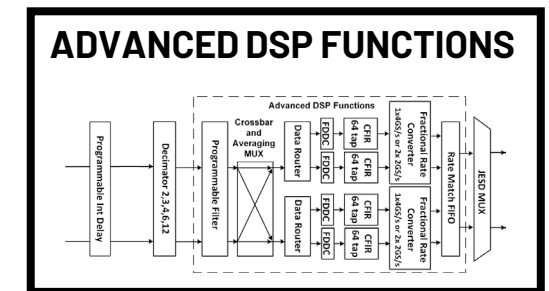
Deterministic Sync and Control

- Multichip sync
- Bidirectional SYSREF
- Fast reconfiguration



Flexible Integrated DSP

- Decimation
- DDC
- FIR
- $<125\text{ns}$ latency (bypass)

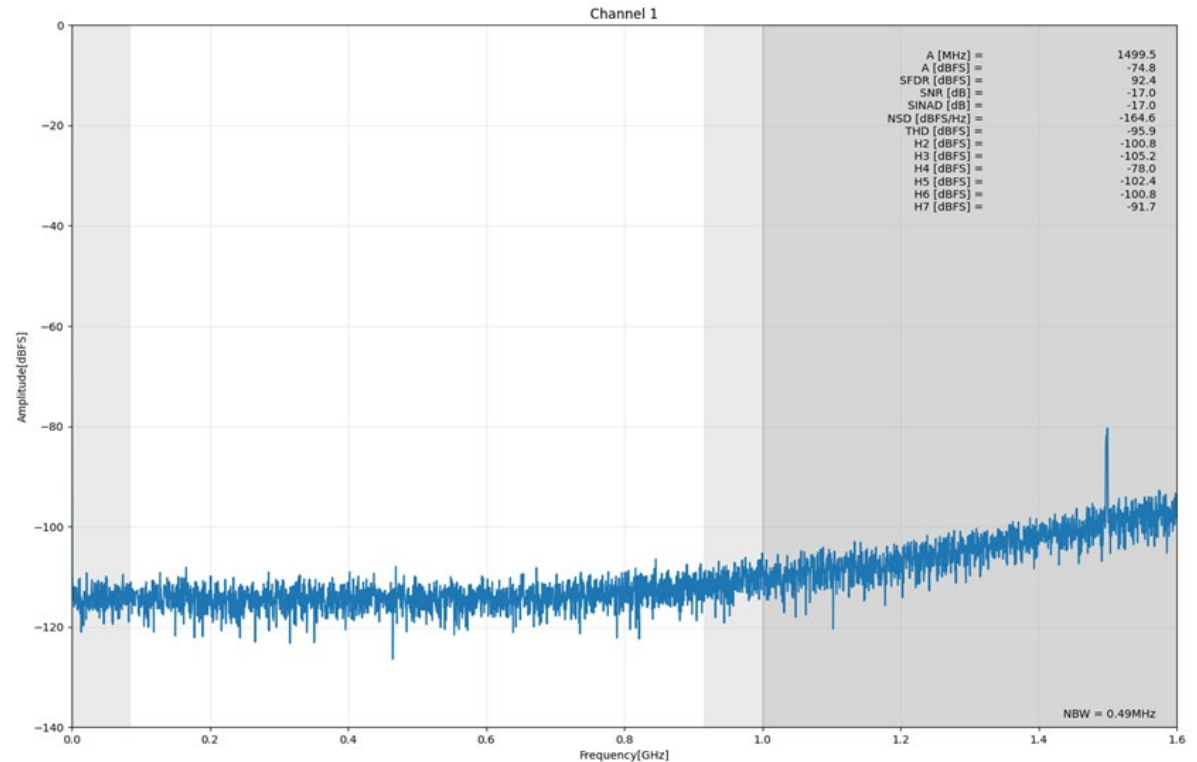


Groundbreaking NSD in 1GHz Bandwidth

The AD9290 boasts an impressive
-164dBFS/Hz noise spectral density
within a 1GHz bandwidth

Key applications where receive sensitivity
is critical:

- Next-generation desktop spectrum analyzers
- Doppler radar systems
- Communications channel emulators
- High-end data acquisition in factory automation systems
- Wired communications testing
- UHF/VHF communications direct sampling receivers



Note: Due to the FFT size of 8192, noise floor of this FFT sits around -107dBFS. This is expected, as the bin size is 490kHz.

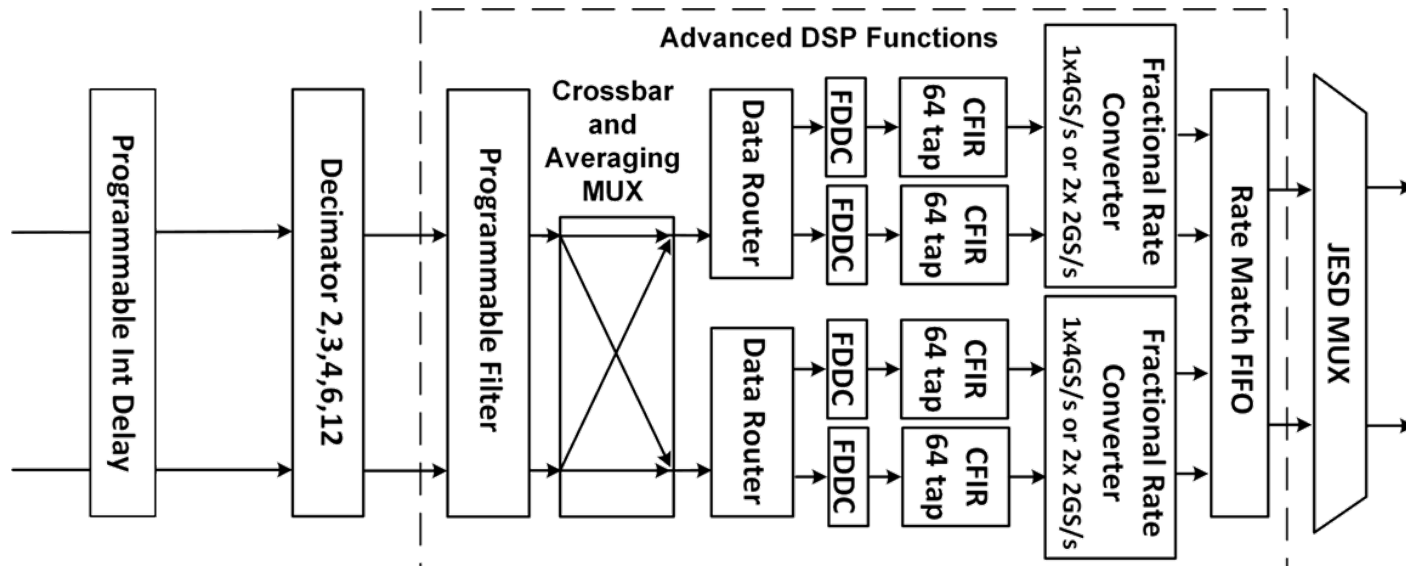
$$NSD_{FFT} = -164 + 10 \log_{10}(490,000) \cong -107 \text{dBFS}$$

Advanced On-Chip DSP

Flexible, real-time signal processing

The AD9290's advanced DSP features enable customers to:

- Dynamically reconfigure the receive path without interrupting operation
- Correct signal-chain impairments using programmable digital filters
- Isolate and process up to four carriers simultaneously using integrated digital downconverters (DDCs)
- Bridge systems operating at different clock rates through the fractional sample-rate converter



AHEAD OF WHAT'S POSSIBLE

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