ANALOG DEVICES

EM PLUGS FOR RF ICS PRACTICAL EM MODELS FOR FAST AND ACCURATE RF DESIGN

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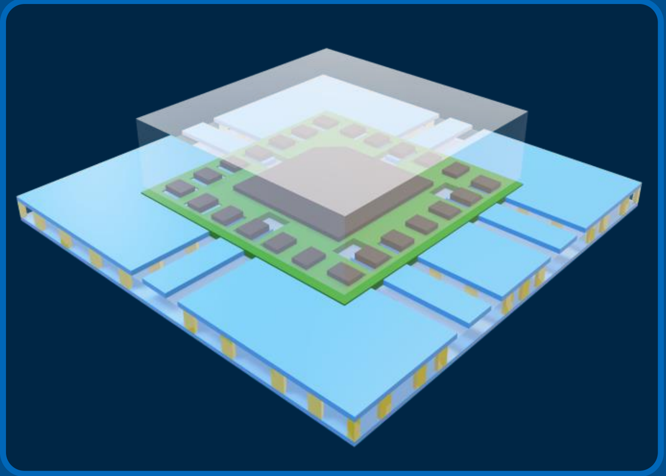
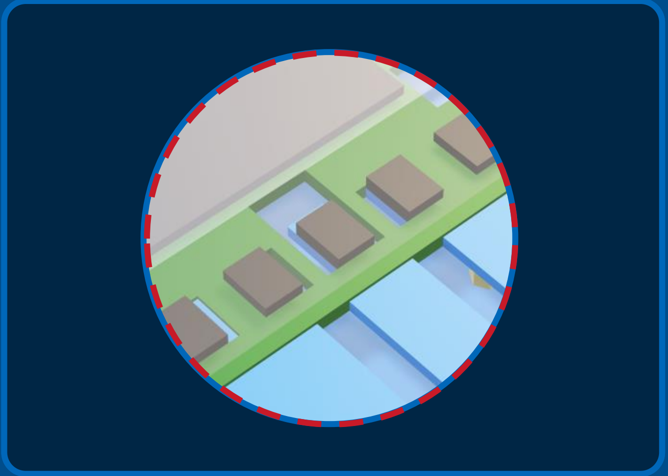
IMS2025

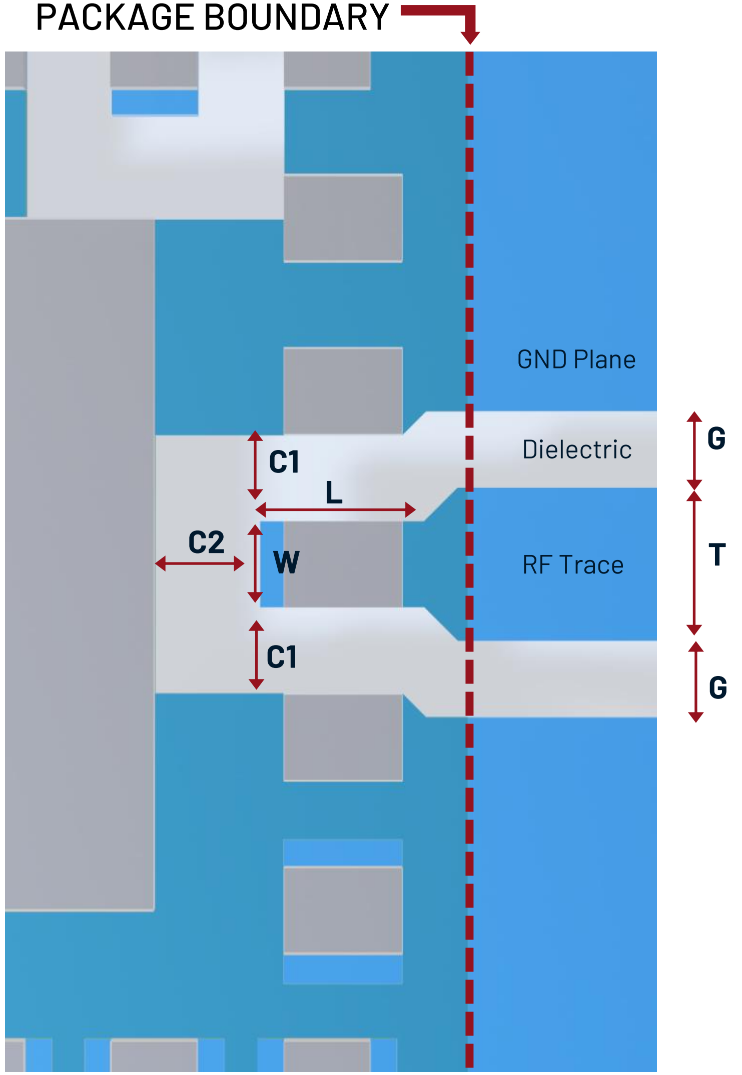
analog.com

Chip-to-Substrate Transition for RF ICs

- RF IC landing pattern parameters, such as **pad size and clearance**, tapering to RF trace or solder paste/mask profile, affect the performance significantly at high frequencies.
- For a **substrate height and properties** different than the IC vendor's reference design, pad parasitics may significantly change, and this directly reflects on overall return loss performance.
- **Traditional s-parameters are** usually offered with a reference plane at the chip boundary or 50 Ω trace finish, therefore **insufficient to simulate** these effects as the critical design parameters fall behind the reference plane.







EM Plugs Concept

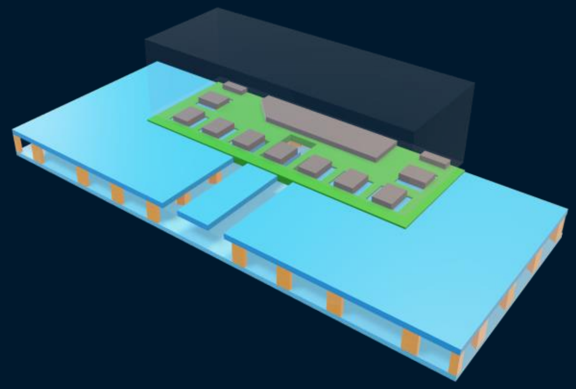
ADI introduces **unencrypted 3D models of the chip-to-substrate transition**, which are called **EM plugs.** EM plugs offer certain advantages over complete encrypted EM model

- EM Plugs are easy to work with and fast to simulate
- Not limited to a single EM tool, portable between simulation environments
- Can address high transistor count complicated EM designs

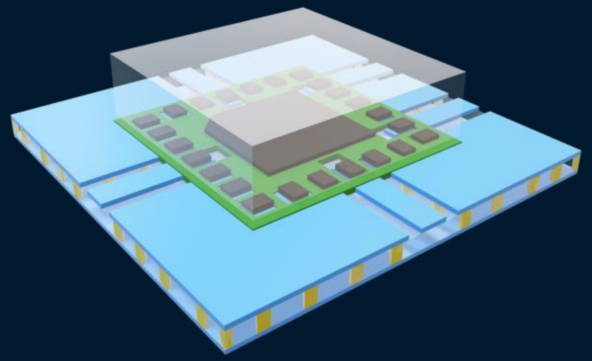
EM plugs incorporate

- Critical metal layers and vias of the die/package
- Dielectric layers of the die/package
- Bumps and solder structures or bond-wire transition
- PCB stack-up for metal, substrate, vias, etc...

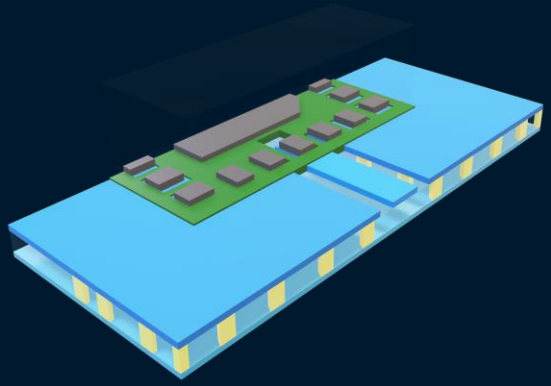
RF COMPONENT



INPUT EM TRANSITION



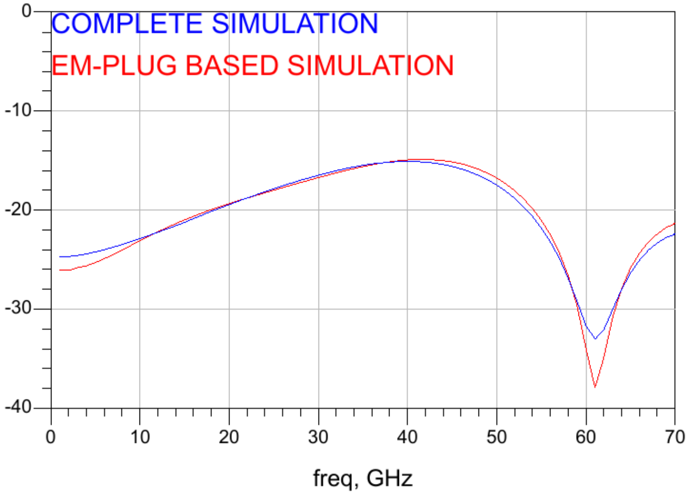
APPLICATION PCB



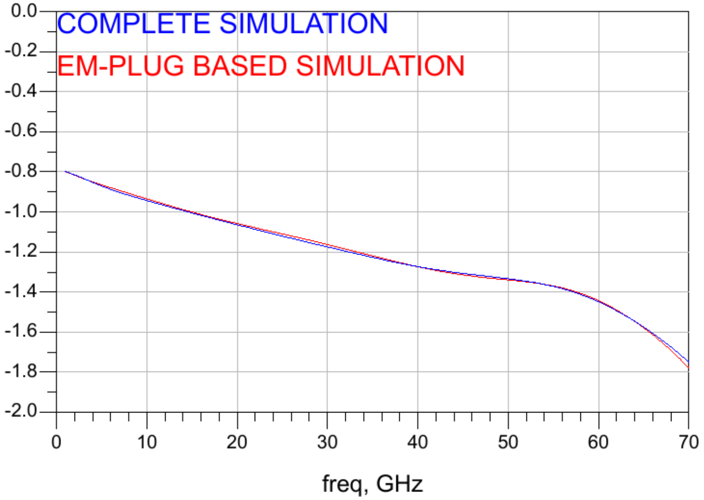
OUTPUT EM TRANSITION

EM Plugs Usage

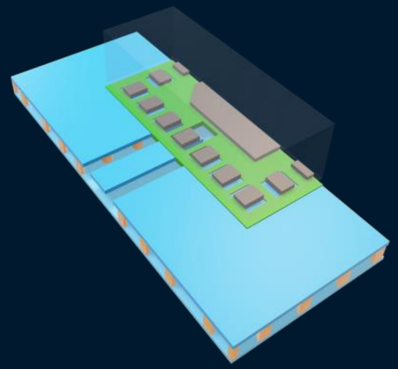
RETURN LOSS



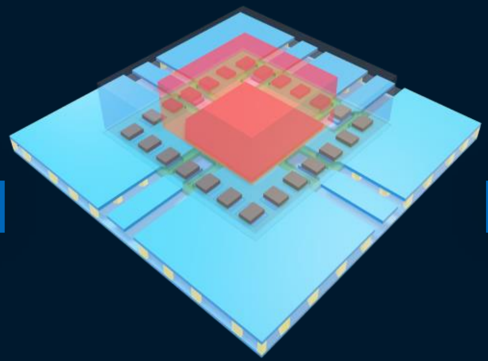
INSERTION LOSS



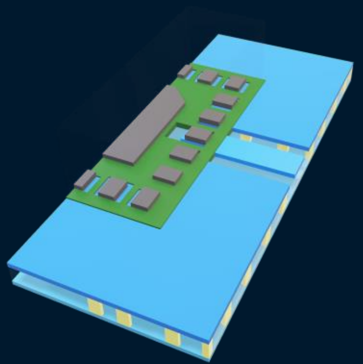
EM PLUGS CASCADED WITH THE RF CORE RESULTS ALMOST THE SAME WITH THE COMPLETE CHIP SIMULATION.



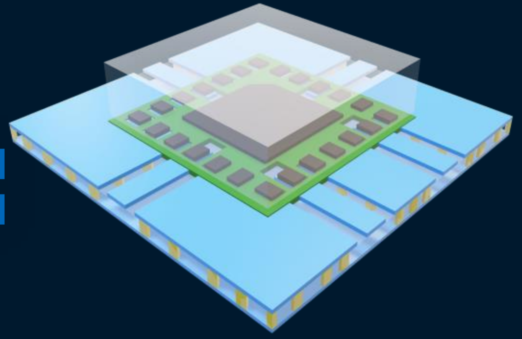
INPUT 3D EM-PLUG



RF-CORE TOUCHSTONE FILE (RED)



OUTPUT 3D EM PLUG

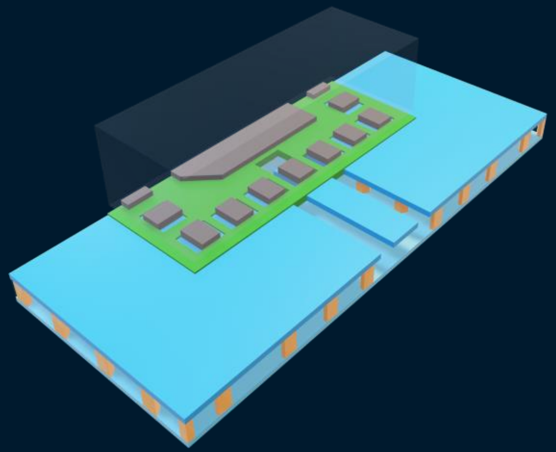


COMPLETE PERFORMANCE

EM Plug vs. Encrypted EM Model

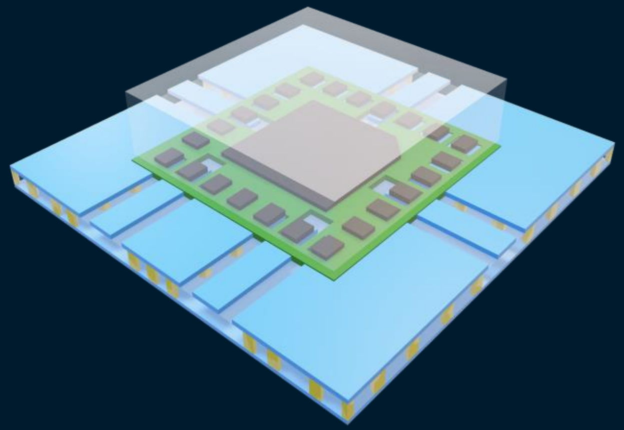
EM PLUG:
Die/package to PCB transition only.

- No IP, no encryption
- Tool independent (CST, HFSS, EMPro, etc.)
- Lightweight and modular:
  - Simulation time: Minutes on any computer
  - Enables assembly or tolerance sweeps
- Accuracy validated up to 90 GHz



ENCRYPTED EM MODEL:
Complete die/package modeled.

- Contains IP, requires encryption.
- Tool dependency due to encryption, bound to a single CAD tool.
- Simulation time: Multiple hours on powerful computer.
- **Can every part be modeled in EM?**



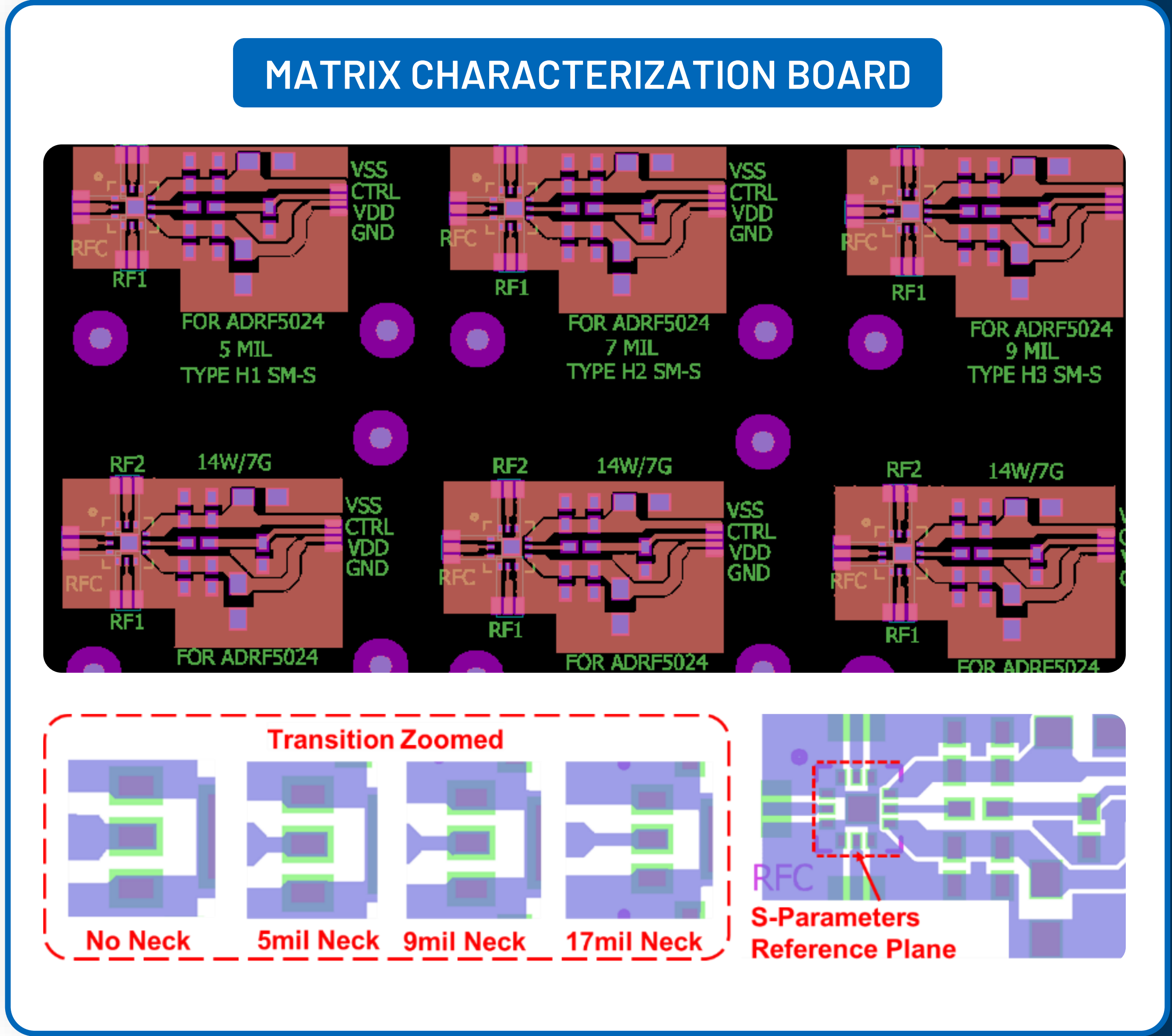
Traditional Way

- RF ICs are optimized for a specific reference substrate—but in real-world applications, they are mounted on various PCBs with different materials and transition styles

- Performance at high frequencies is significantly affected by:
  - Landing pattern geometry
  - PCB substrate properties (dielectric constant, thickness)
  - RF trace type (microstrip, coplanar waveguide, stripline)
  - Assembly rules (solder mask/paste type and thickness)

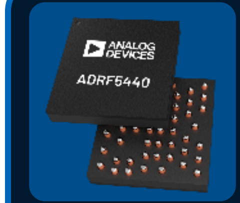
- Traditional method: Fabricate a matrix of possible transitions, test each, and select the best-performing one—time-consuming and costly.

- **Without EM modeling**: No easy way to simulate substrate and transition effects before hardware build.

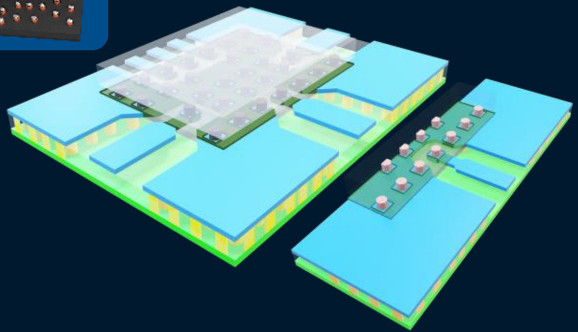


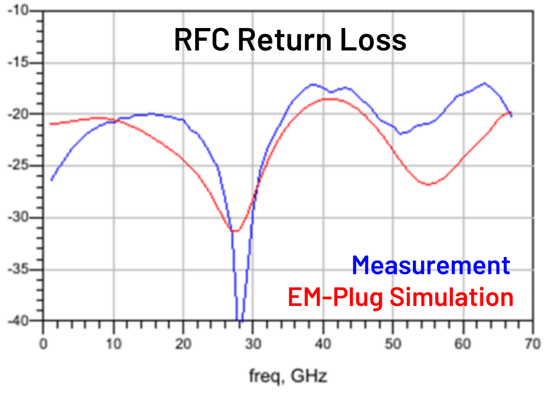
EM Plugs Examples for Different Package Types

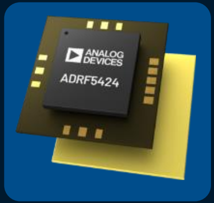
ADI EM models for RF components match closely with measurement results and offered for different package types



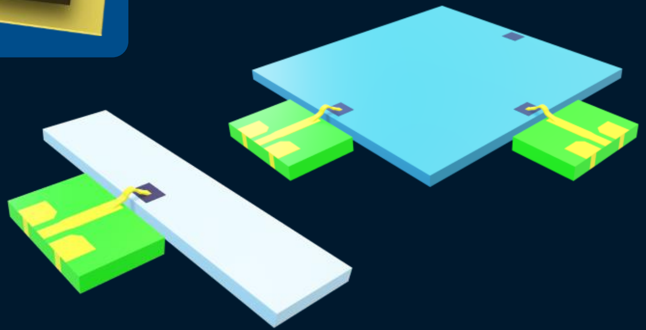
FLIP CHIP SMT

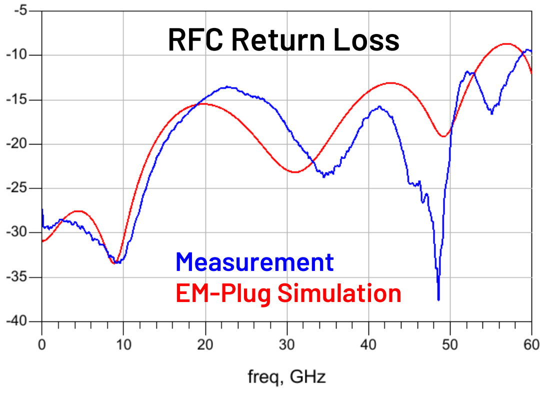




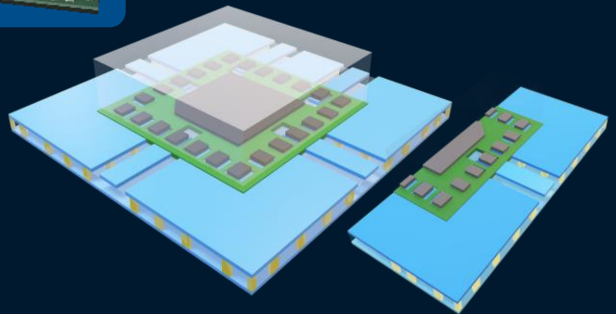


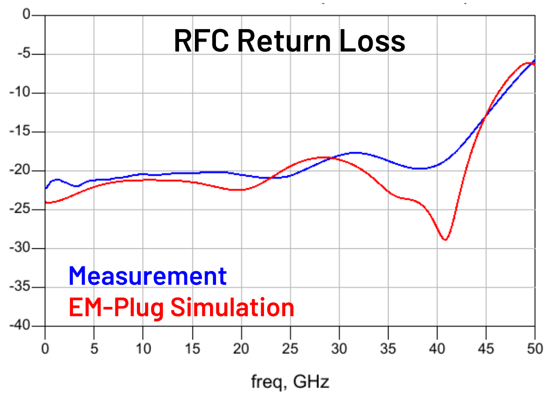
CHIP AND WIRE





LFCSP/LGA



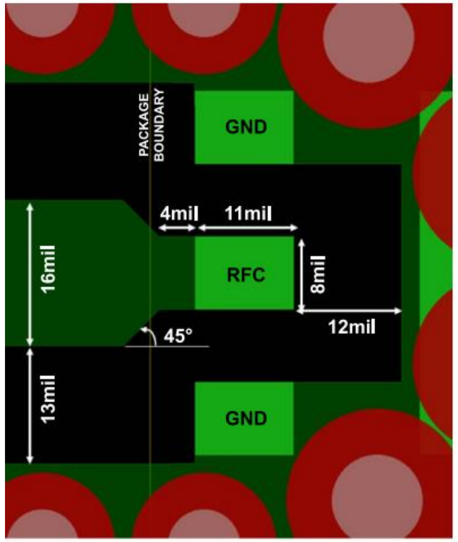


PCB Stack-Up Change, Designing New Transition

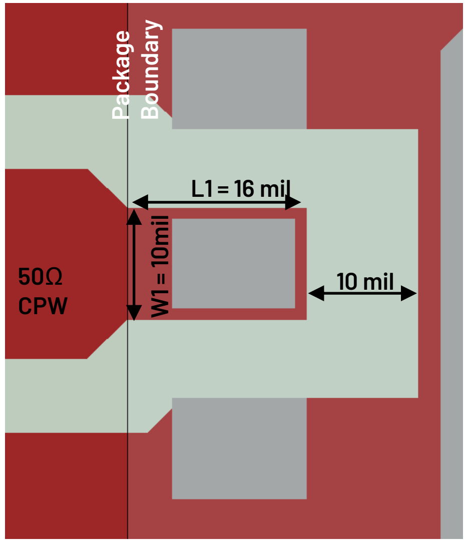
PROBLEM: Thicker/thinner substrate vs. the reference stack-up may degrade return loss when not compensated

SOLUTION: Optimize the device to PCB transition with EM plugs

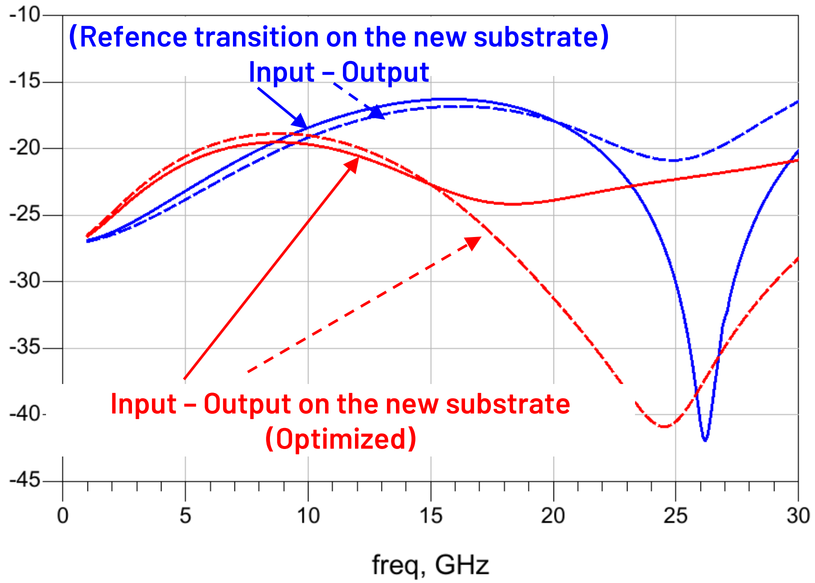
- Thicker RF substrate causes less pad capacitance; therefore, the RF pads should be compensated capacitively.
- Thinner RF substrate causes more pad capacitance; therefore, the RF pads should be compensated inductively.



Default recommended landing pattern on the reference substrate



Optimized landing pattern on new thicker substrate, wider PCB pads



PCB Manufacturing Tolerance Sensitivity Analysis

PROBLEM: What is pad transition sensitivity to PCB manufacturing tolerances ?

SOLUTION: Transition EM simulated with PCB manufacturing tolerances

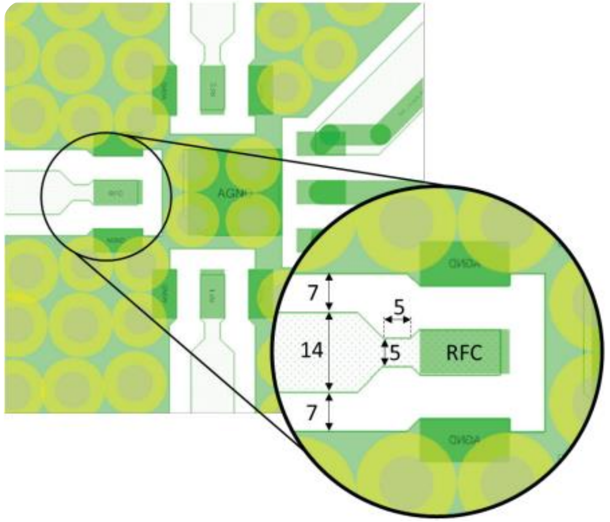
PCB TOLERANCES TO ANALYZE:

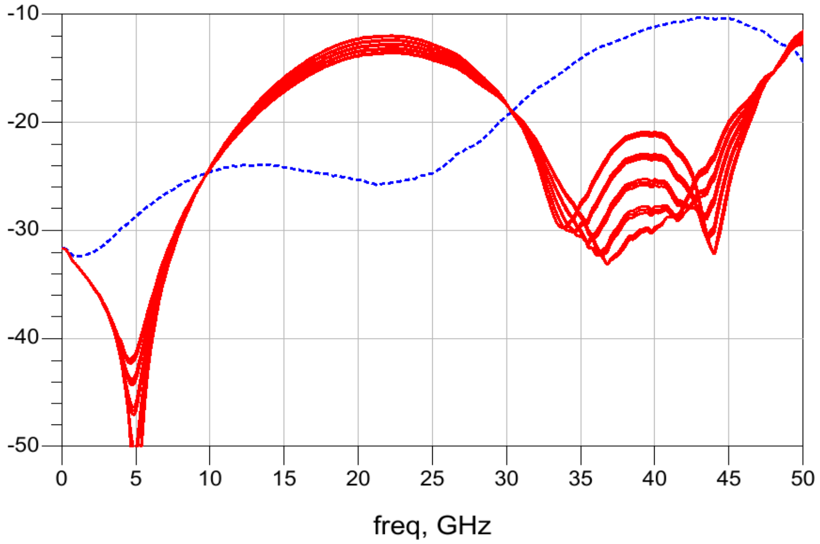
Typical dielectric tolerance = ±0.05

- Critical for 50 Ω trace and matching

Typical metal tolerance= ±1 mil or ±25 µm

- Critical for high frequency 50 Ω trace
- Critical for high frequency matching elements

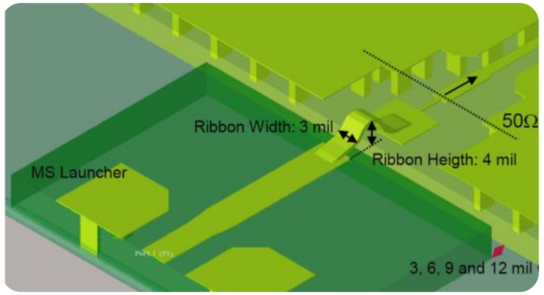


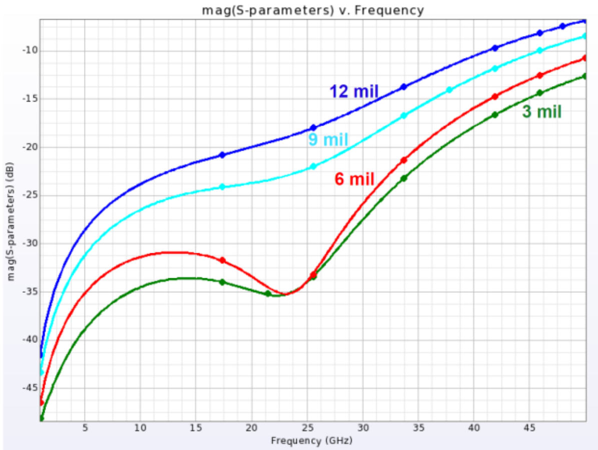


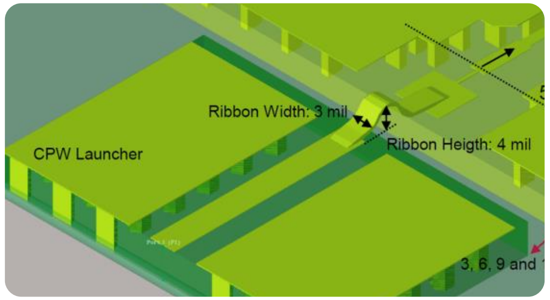
Assembly Variation Analysis

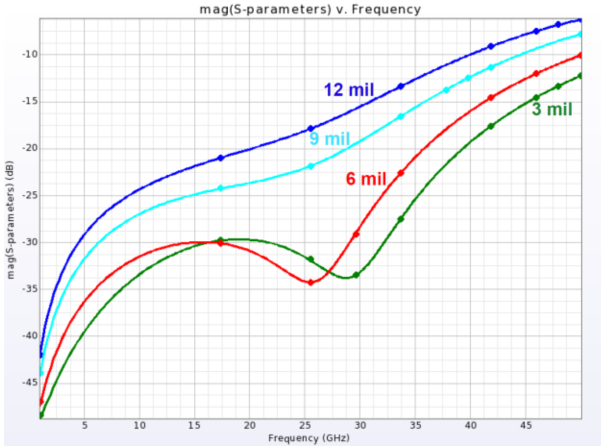
PROBLEM: How does the bond-wire transition's performance change with different wire-bond/ribbon lengths

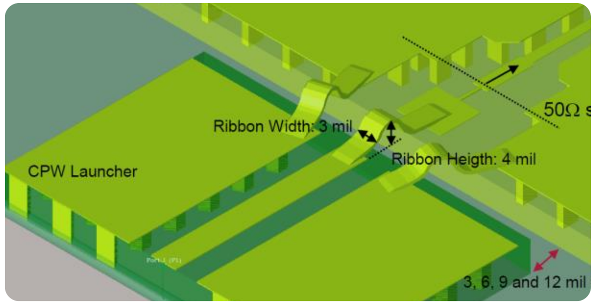
SOLUTION: Characterize assembly variations and different die to substrate spacing using EM Plugs

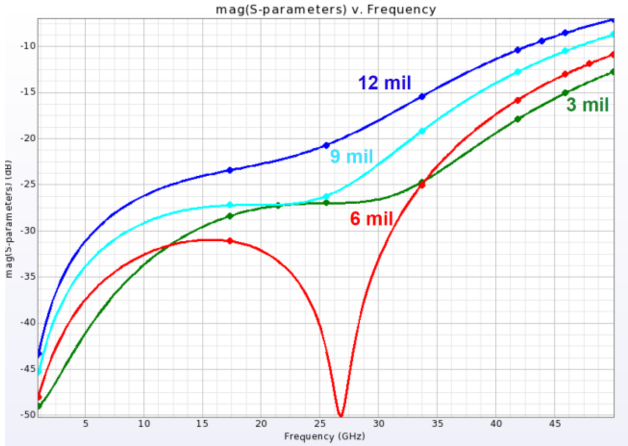






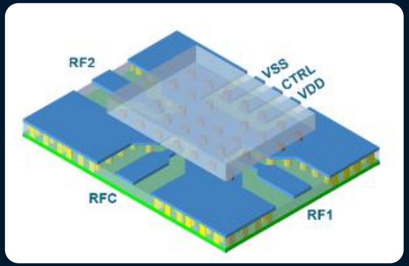


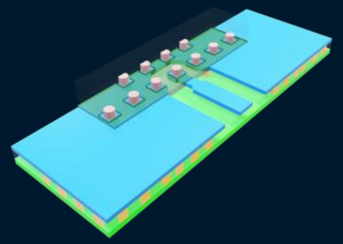




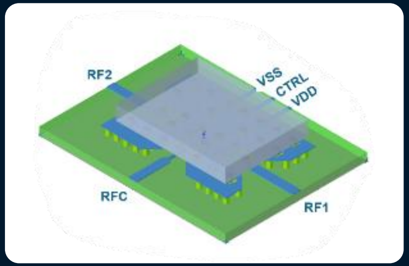
Transitions for CPW, Microstrip, and Stripline

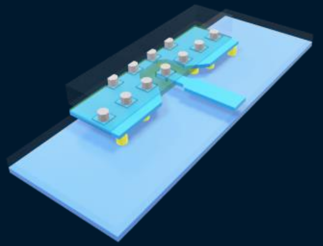
COPLANAR WAVEGUIDE



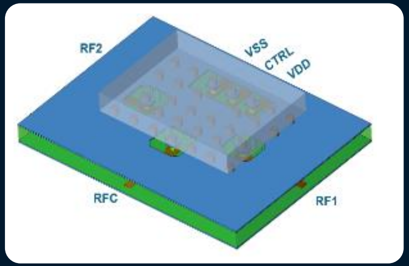


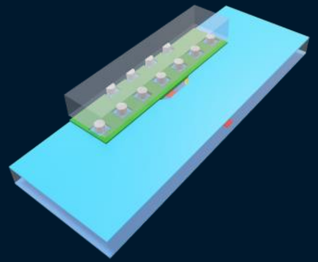
MICROSTRIP



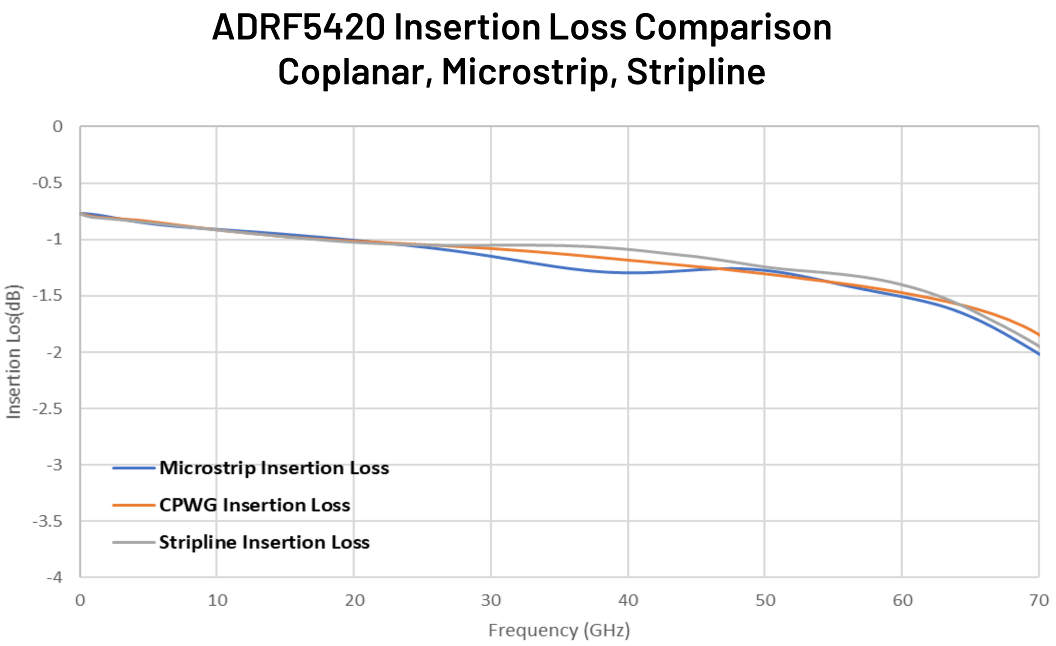


STRIPLINE





- Coplanar waveguide (CPW) is the first choice for many RF applications and certain designs require microstrip or stripline as well.
- Accurate EM plug models ensure the optimum performance for any RF transmission line of choice with proper signal and ground transitions.



EM Plug Use

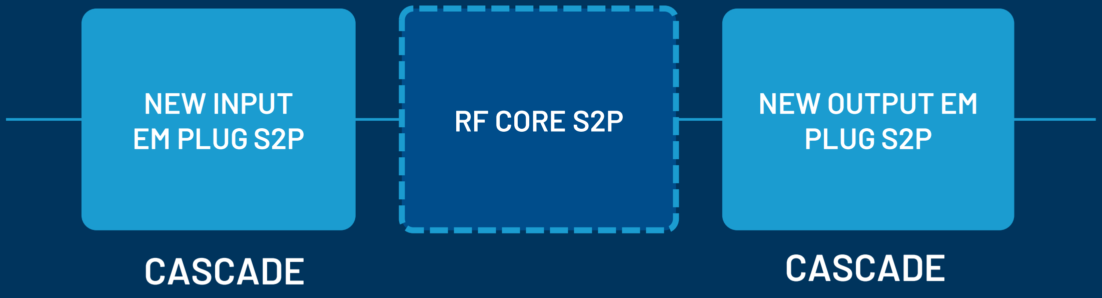
1 Obtain EM Plugs and RF core files from Analog Devices

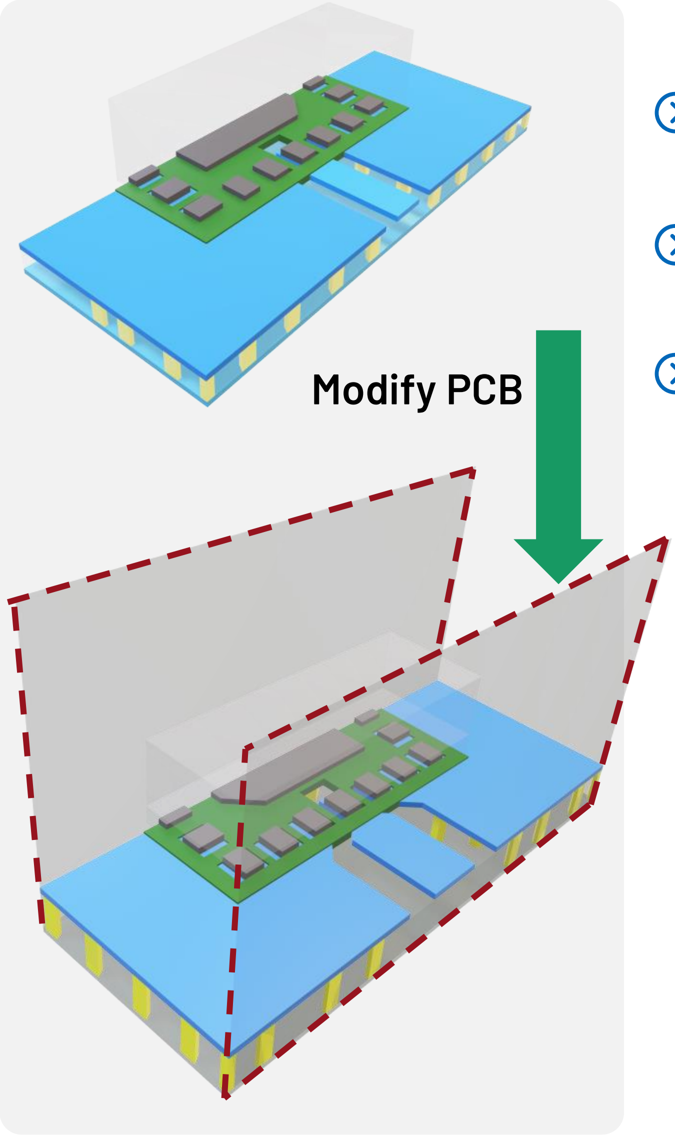
- EM plugs come where the PCB is configured as the ADI reference design

2 Modify EM plugs for the new substrate and transition

3 Run EM simulation of the input and output EM plugs export s2p

4 Combine with the RF Core





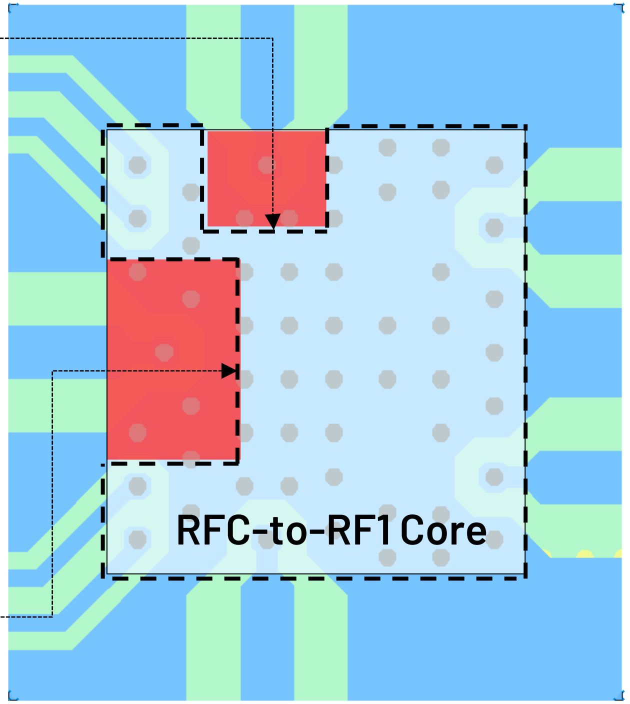
- RF substrate height and dielectric modified
- 50 Ω CPW dimensions changed
- Pad dimensions and landing pattern modified

PORTS PLACED AT THE PCB SIDE AND CHIP SIDE

RF Core Details

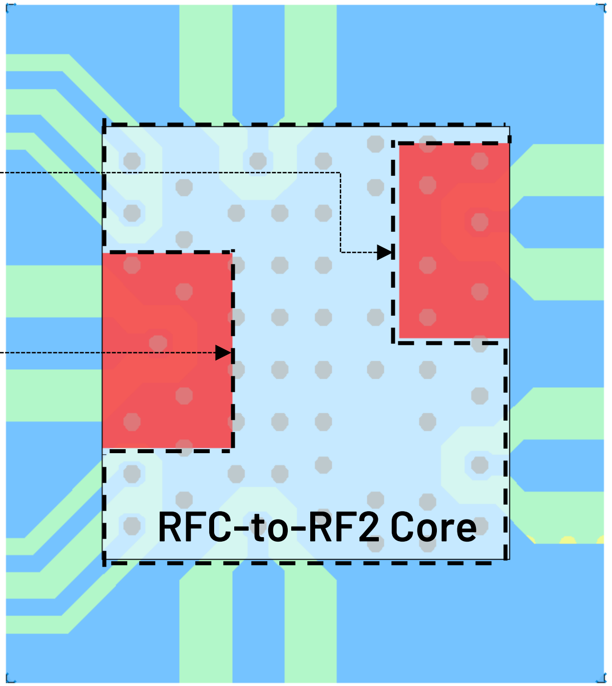
- There could be multiple RF core S-parameter files as the state of the chip may change:
  - RF arm of a switch, state of a digital step attenuator, biasing conditions of an amplifier, state of a tunable filter...
- For an SP4T example, RFC-to-RF1 and RFC-to-RF2 rf-cores will be provided as s2p touchstone files to be used with the EM plugs.

PORT2 (RF1)
REFERENCE PLANE



PORT1 (RFC)
REFERENCE PLANE

PORT2 (RF2)
REFERENCE PLANE



PORT1 (RFC)
REFERENCE PLANE

ANALOG DEVICES

Conclusion and What's Next

Analog Devices introduces a new unencrypted transition-based EM model approach, "EM Plugs," to the industry, enabling precise performance predictions across varying substrates and transitions.

DISTRIBUTABLE UNDER NDA

- Chip-to-substrate effects are captured only; no IP contained.

TOOL INDEPENDENCE

- EM plugs could be used on any CAD tool, unlike encrypted models.

LIGHTWEIGHT AND MODULAR DESIGN

- Allows rapid EM parameter sweeps and significantly reduces simulation times.

ACCURACY FOR HIGH FREQUENCIES

- Validated method up to 90 GHz using actual devices.

ADDRESSES COMPLEX DESIGNS

- System-in-package, multi-chip-modules...

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AHEAD OF WHAT'S POSSIBLE

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