WSG-9

Bringing Commercial Access to Space

Mohamed Abdalla

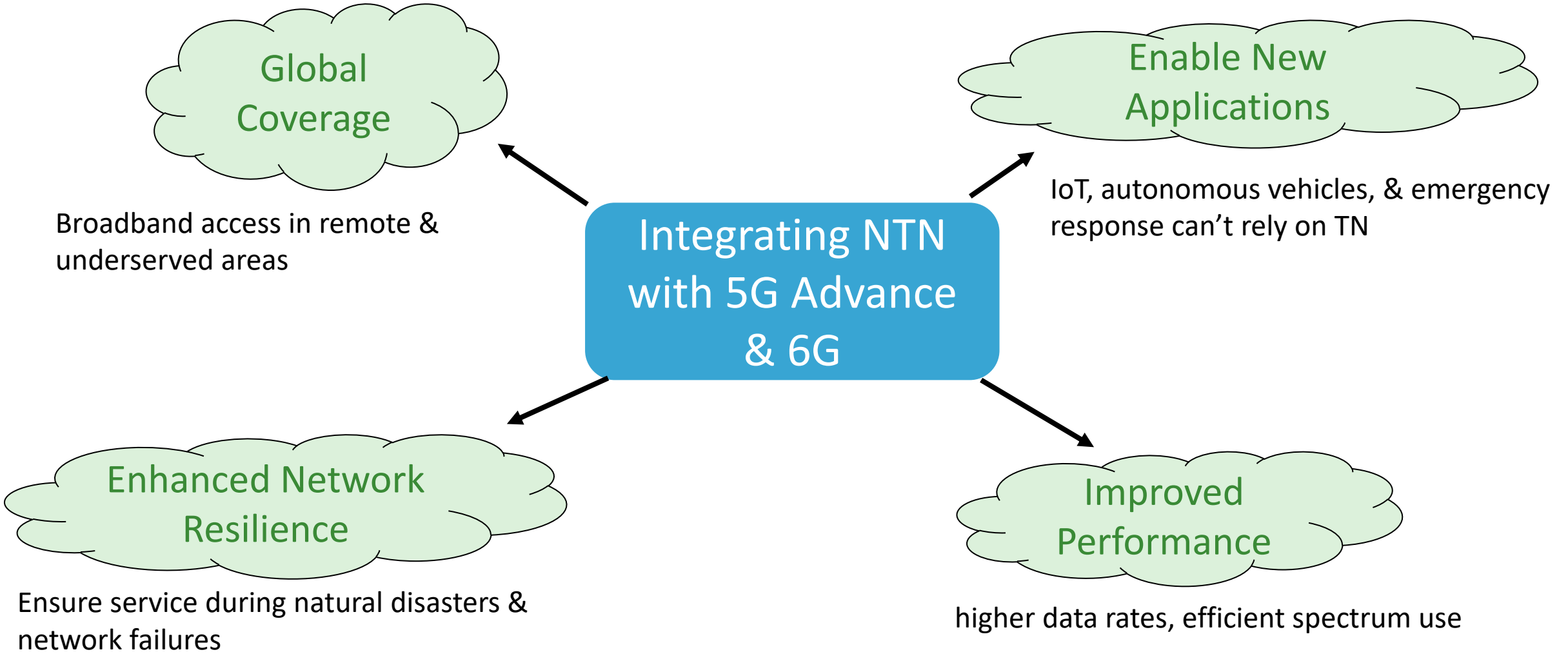
Analog Devices

ANALOG DEVICES

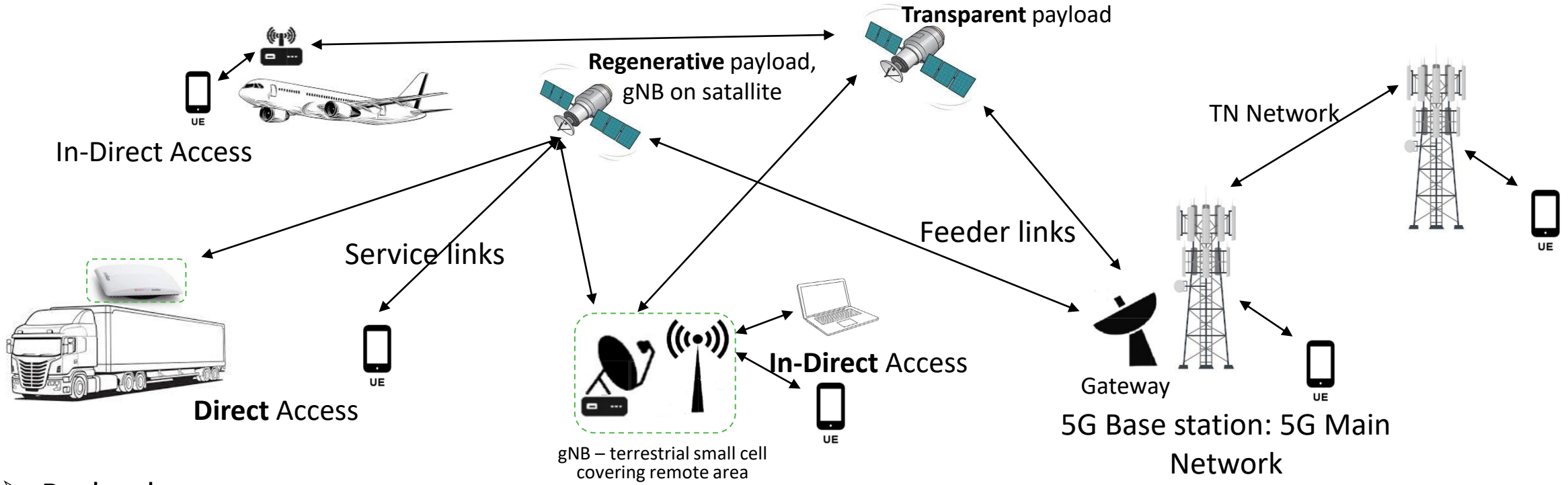
Presentation Outline

- Introduction:
  - Motivation for Integrating NTN with 5G
  - NTN Use cases & Challenges
- LEO SAT Technology Development
- Array Line-up Analysis: Impact of BFIC NF & P1dB
- Array Calibration
- Gen 1 Ku-Band Half Duplex BFIC & TDD Array Design
- Gen 2 BFIC Split Architecture & Ka-band FDD array with same Tx & Rx antenna aperture
- Conclusion

Motivation for Integrating NTN with 5G/6G Network



5G Non-Terrestrial Networks (NTN) Use Cases



- Payload:
  - Transparent payload: gNB on ground and satellite acts as repeater
  - Regenerative payload: packet-processing & gNB is placed on the satellite
- 5G NTN architectures can provide direct or indirect access to the main cellular network [1]

[1] F. Völk et al., "Field Trial of a 5G Non-Terrestrial Network Using OpenAirInterface," in IEEE Open Journal of Vehicular Technology, vol. 3, pp. 243-250, 2022

Using Low Earth Orbit (LEO) Satellites for NTN

Pros:

- Lower Latency ✓
- Lower free-space path loss ✓
- Smaller Beam footprint ✓
  - better frequency reuse
  - Smaller beam requires capability for accurate beam pointing (requires calibration) !!!

Cons (Challenges):

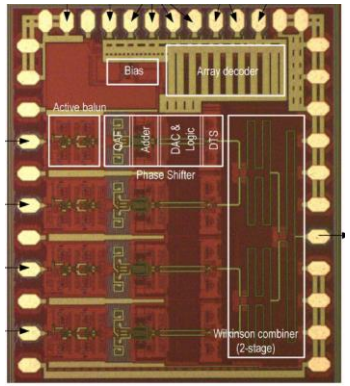
- Larger number of Satellites ✗
  - **Solution**: Lower cost Satellites
    - Small size/Weight
    - Low power consumption
    - Low NF Front-ends
- Constant Satellite movement ✗
  - **Solution**: Dual beam BFICs & Fast beam switching

- Solving the cons (Challenges) of LEO Sat will provide a path for commercializing NTN

LEO SAT Technology Development

2008 — Rebeiz – UCSD

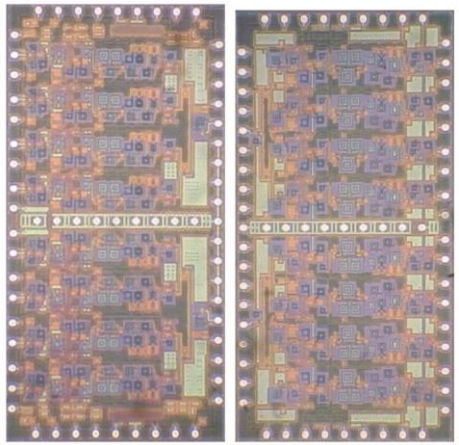
A Q-Band Four-Element Phased-Array Front-End Receiver



HEMT LNAs + 0.18µm
SiGe Rx: 4-Element BFIC

2010 — Warnick- Brigham Young & Washington State University

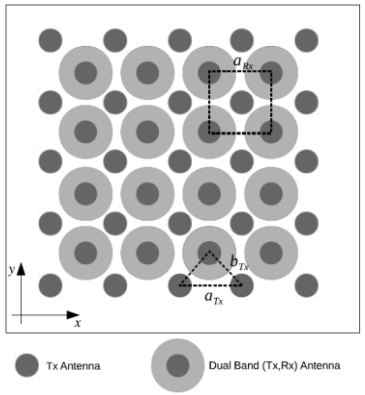
Integrated Eight Element Ku Band Transmit/Receive Beamformer Chipset



SiGe Rx & Tx
4-Element Dual Pol BFIC

2016 — Ziegler – University of Calabria, Qorvo & Airbus

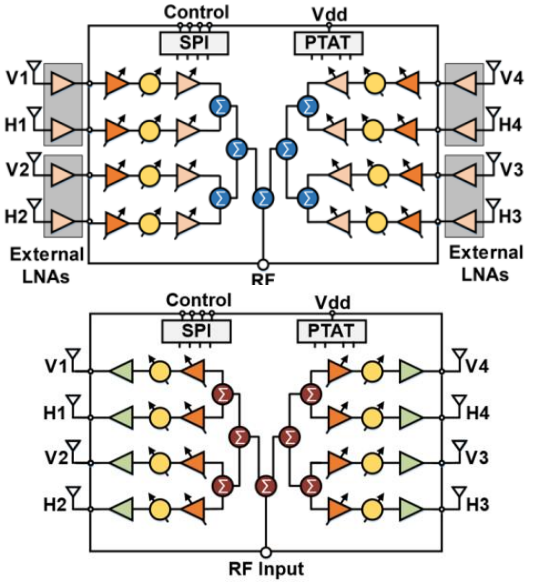
Radiating Elements for Shared Aperture Tx/Rx Phased Arrays



Not a comprehensive list!

2018 — Rebeiz - UCSD

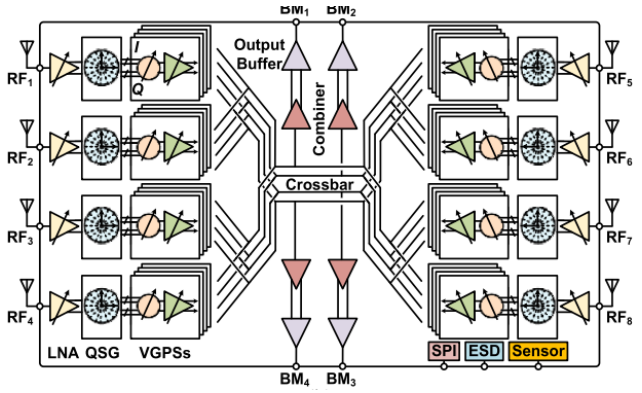
A Scalable Dual-Polarized 256-Element Ku-Band Phased-Array SATCOM Receiver & Transmitter



GaAs LNA + SiGe Rx & Tx
8-Elements BFIC

2023 — Zhiwei Xu - Zhejiang University & UC Davis

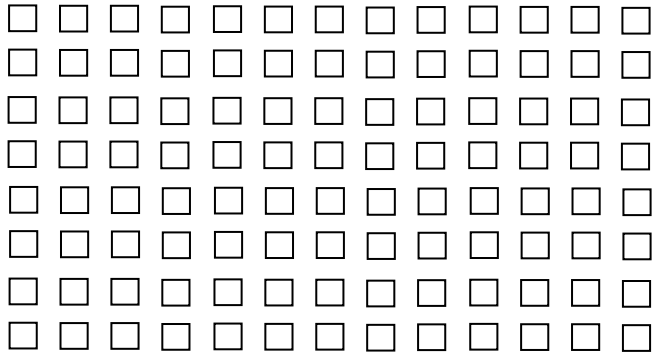
A Compact Ka-Band Eight-Element Four-Beam Receiver



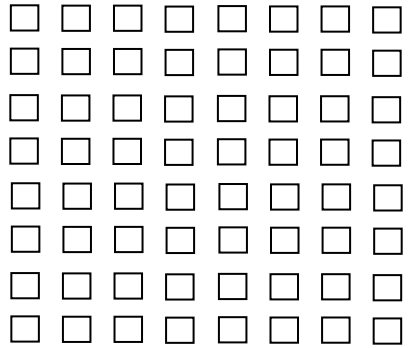
65nm Bulk CMOS
8-Elements BFIC

Rx Array Line-up Analysis: Impact of Reducing BFIC NF

Gen1 Array
104 BFICs: 8x13



Gen2 Array
64 BFICs: 8x8



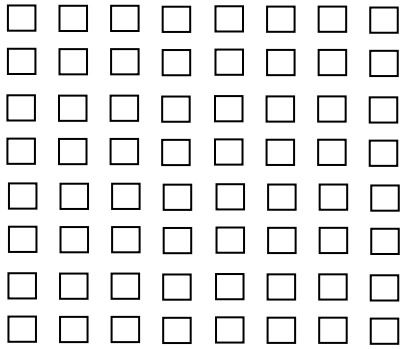
- If Gen2 BFICs have lower NF by 0.5dB compared to GEN1 BFIC
- To achieve the same target G/T of 6.9dB/K
  - Gen1: Array size: N=416 Elem (104 BFICs x 4 CHs/BFIC)
  - Gen2: Array size: N=256 Elem (64 BFICs x 4 CHs/BFIC)
- Less # BFICs for same G/T → Reduced BOM/cost, PCB area & Power consumption/heat sink cost → thinner flat panel

	Gen1			Gen2	
# BFs	104			64	
Array Gain	31.161	dBi		29.052	dBi
Antenna Noise Temp.	20	°K		20	°K
Feed NF	0.5	dB		0.5	dB
Feed Temp (T_A)	290	°K		290	°K
G/T =	**6.9**	**dB/K**	**G/T =**	**6.9**	**dB/K**

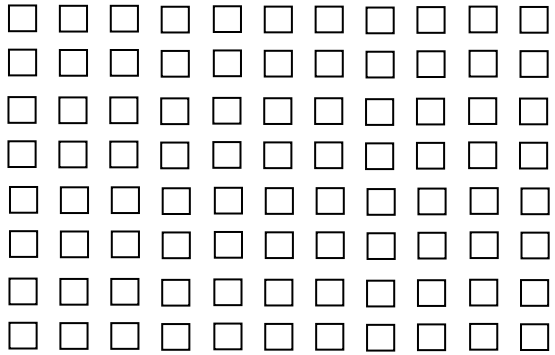
38% Power Consumption Saving!

Tx Array Line-up Analysis: Impact of BFIC P1dB

Gen1 Array
64 BFICs : 8x8



Gen2 Array
80 BFICs : 8x10



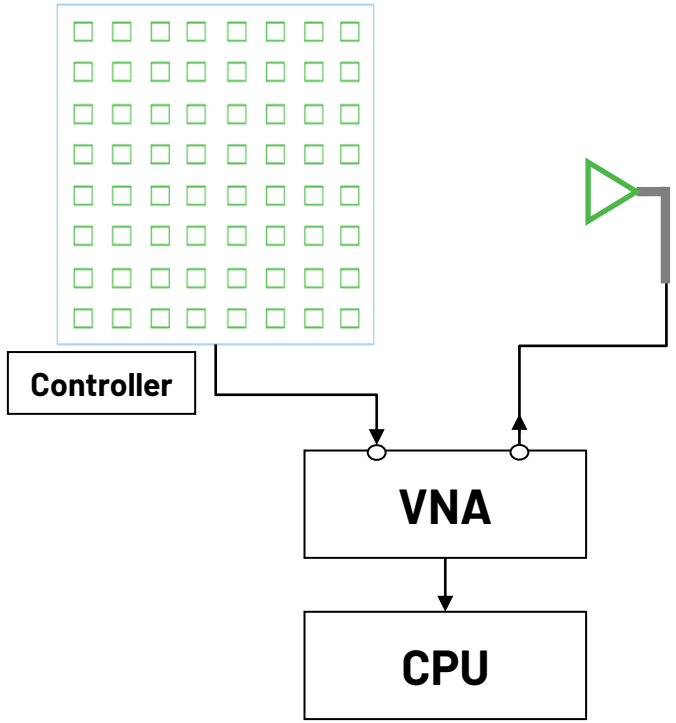
- If Gen2 BFICs have lower P1dB by 2dB compared to GEN1 & assuming the same efficiency
- To achieve the same target EIRP of 64.6dBm
  - Gen1: Array size: N=256 Elem (64 BFICs x 4 CHs/BFIC)
  - Gen2: Array size: N=320 Elem (80 BFICs x 4 CHs/BFIC)
- Sometime Less P1dB per element is more Power efficient→ Good news for CMOS!

	Gen1		Gen2	
# BFICs	64		80	
Pout/Ch	12	dBm	10	dBm
Ant. Directivity	4.97	dBi	4.97	dBi
Feed Loss	0.5	dB	0.5	dB
Efficiency	15	%	15	%
Pdiss/Element	106	mW	67	mW
Array Pdiss	6.8	W	5.3	W
EIRP	**64.6**	**dBm**	**EIRP**	**64.6** **dBm**

22% Power Consumption Saving!

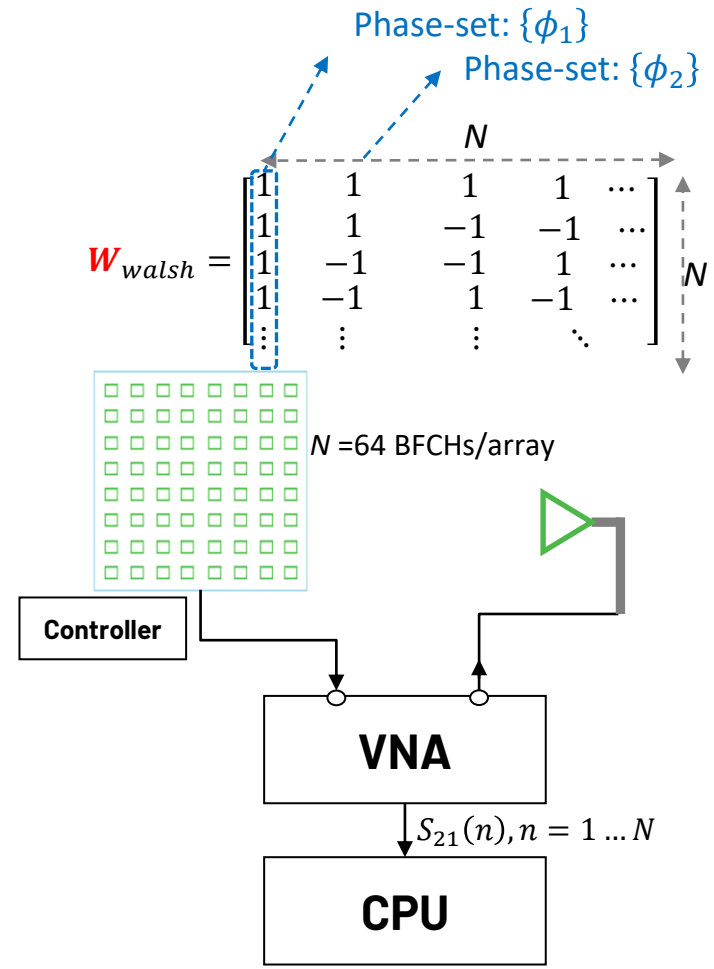
Array Calibration

- Need for array calibration arises due to BFIC channels gain and phase mismatches due to:
  - Fabrication/process variations
  - Unequal RF trace losses
  - Temperature gradient
- To guarantee proper beam steering & nulling → array calibration is necessary
- Array calibration is typically done in production using external Horn antenna, VNA & an external controller (for BFCH gain/phase control)



Walsh Code Based Array Calibration

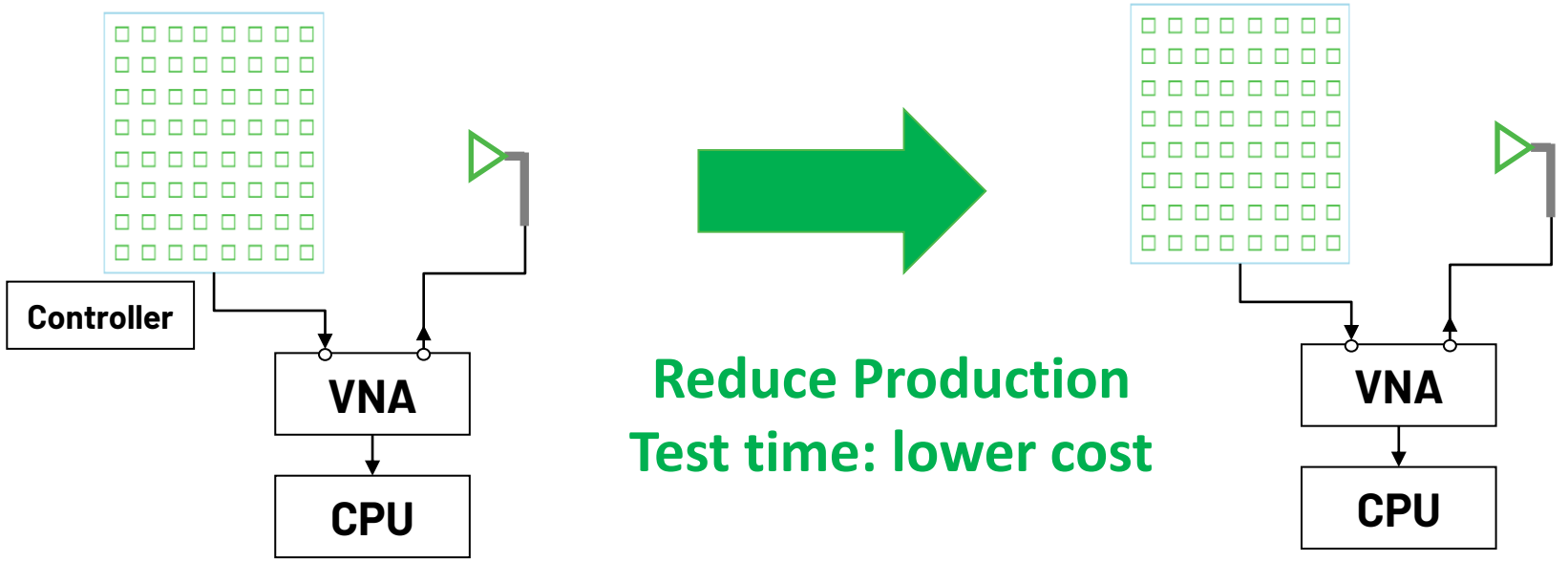
- **General description**: Apply phase-shifts to BFCHs
  - The phase-shifts are either 0° or 180° (Orthogonal bi-polar Walsh code)
  - For *N* (=64) BFCHs, we use *N*(=64) Walsh-code generator
  - An $N \times N$ Walsh matrix is shown on the right
- **Detailed Procedure**:
  1. Set BFCHs phase-shifters to the phase set $\{\phi_1\}$
  2. Measure array S_{21} (magnitude and phase)
  3. Repeat for different phase-sets $\{\phi_2\}, \{\phi_3\}, \ldots, \{\phi_N\}$
  4. Process the *N* values of S_{21} to estimate the gain & phase mismatches of the N BFCHs & calibrate the array



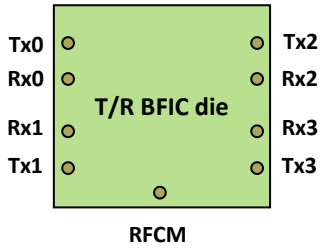
Lengthy process, done during array production testing

On-Chip Built-in Walsh Calibration

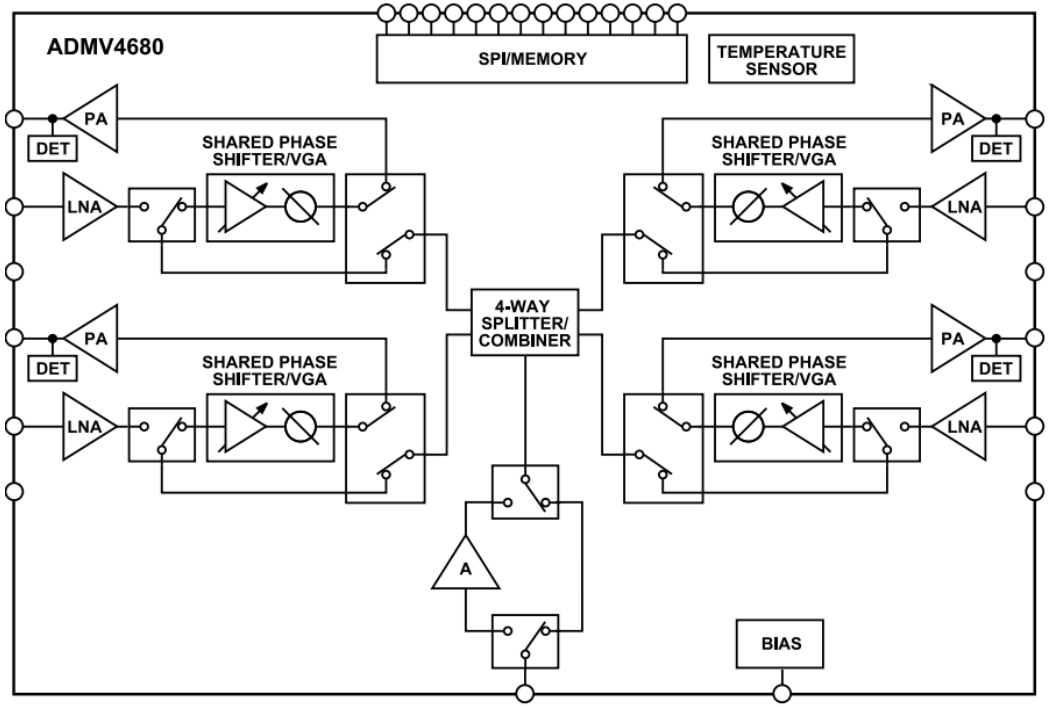
- Walsh-code sequence generators can be integrated inside CMOS BFIC
- Each BFIC is programmed to know its location in the array to apply the proper Walsh sequence
- Hardware assisted calibration can speed up calibration time for the array by more than 100x compared to using an external controller

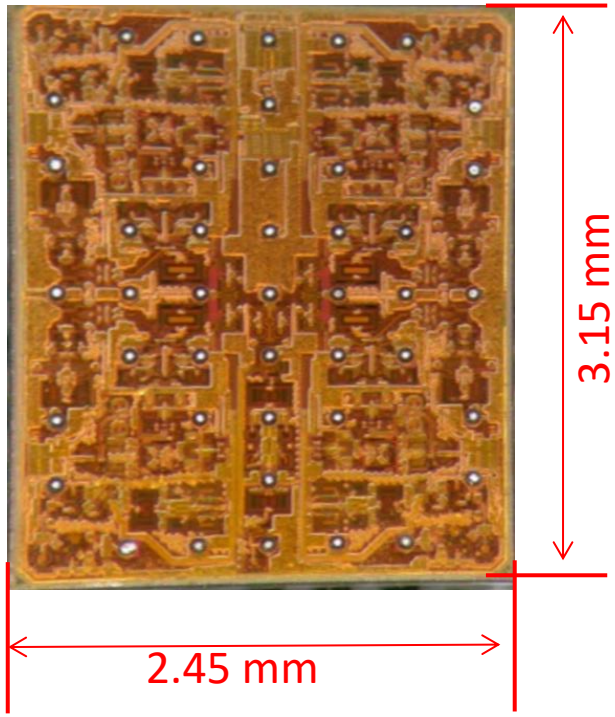


GEN1 Fully Integrated Ku-Band Half Duplex BFIC



GEN1: Bulk CMOS T/R BFIC

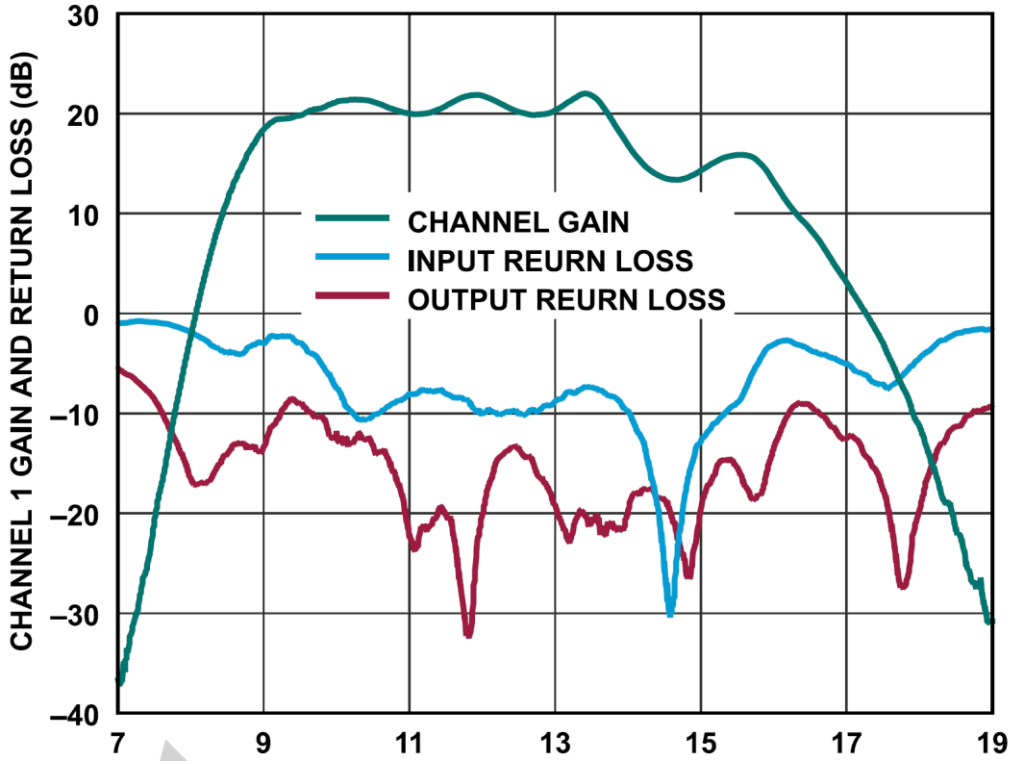


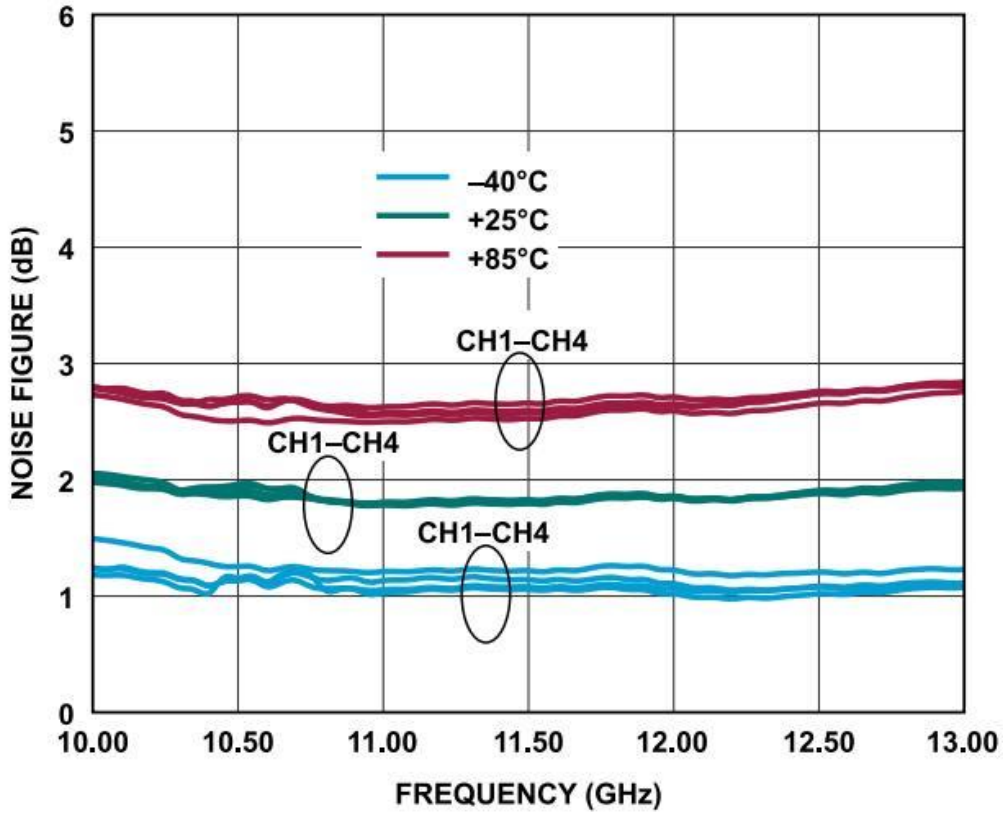


- Chip consist of 4 channels with no switch Infront of the LNA to reduce NF
- LNA/PA feed the same antenna from different ports to the achieve required isolation
- The VGA & VM are re-used in each channel by the Tx & Rx to save Si area/cost
- To reduce packaging cost a bare die flip chip BGA is used

Objective was to minimize BFIC cost!

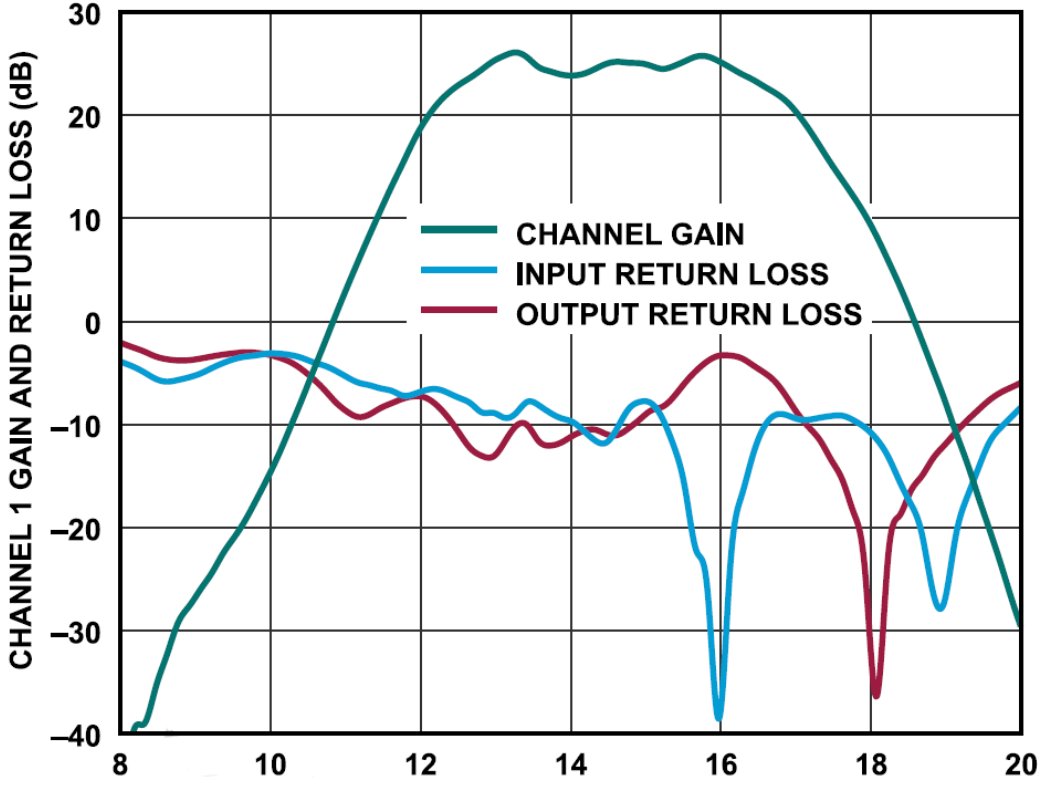
Rx Performance for GEN1 Ku-band TDD BFIC

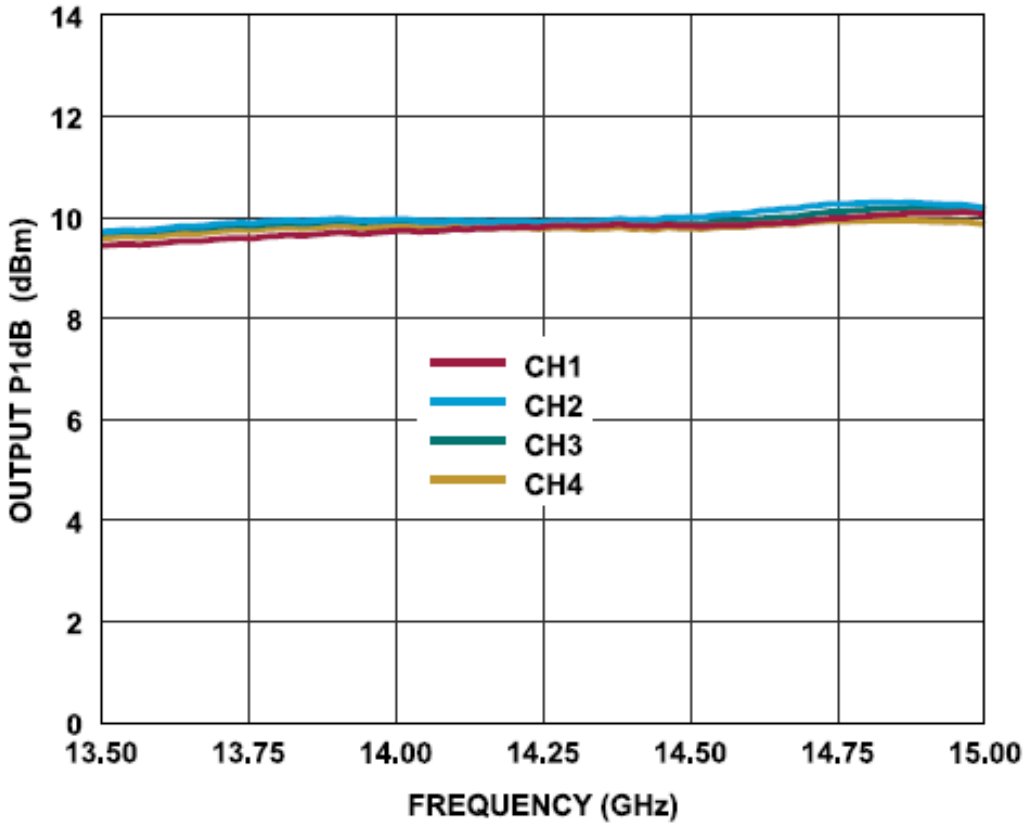




- Gain ripples attributed to limited isolation of the flip chip BGAs
- NF achieved by Bulk CMOS technology is ~1.8dB @Pdiss of 78mW/CH

Tx Performance for GEN1 Ku-band TDD BFIC

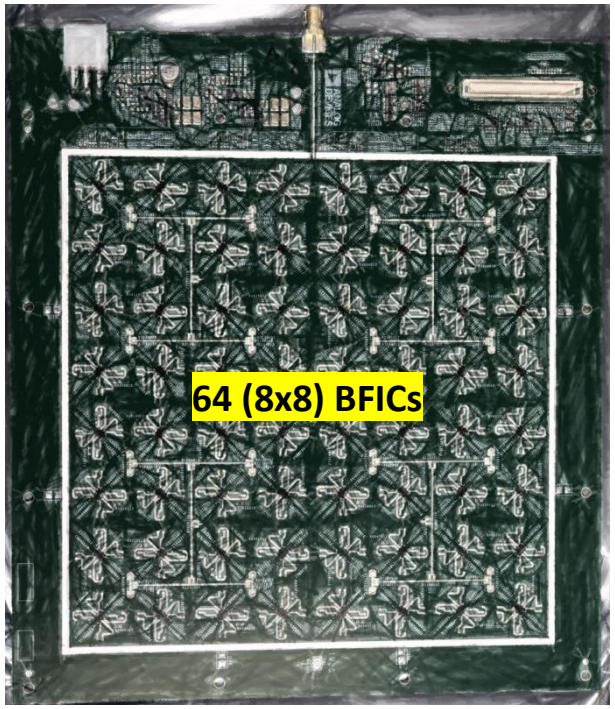




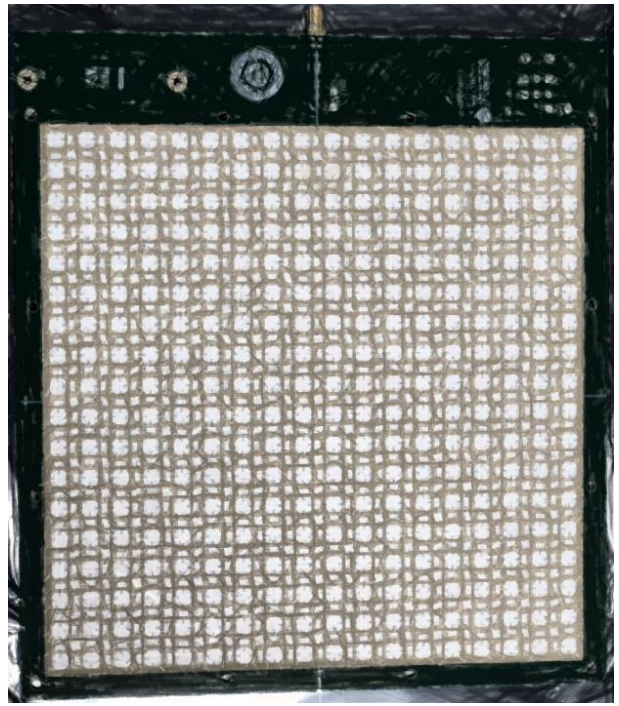
- Tx achieves a 10dBm OP1dB on bulk CMOS
- Tx Pdiss is 108mW/CH at 10dBm output power

GEN 1 Ku-Band TDD Array

Component Side

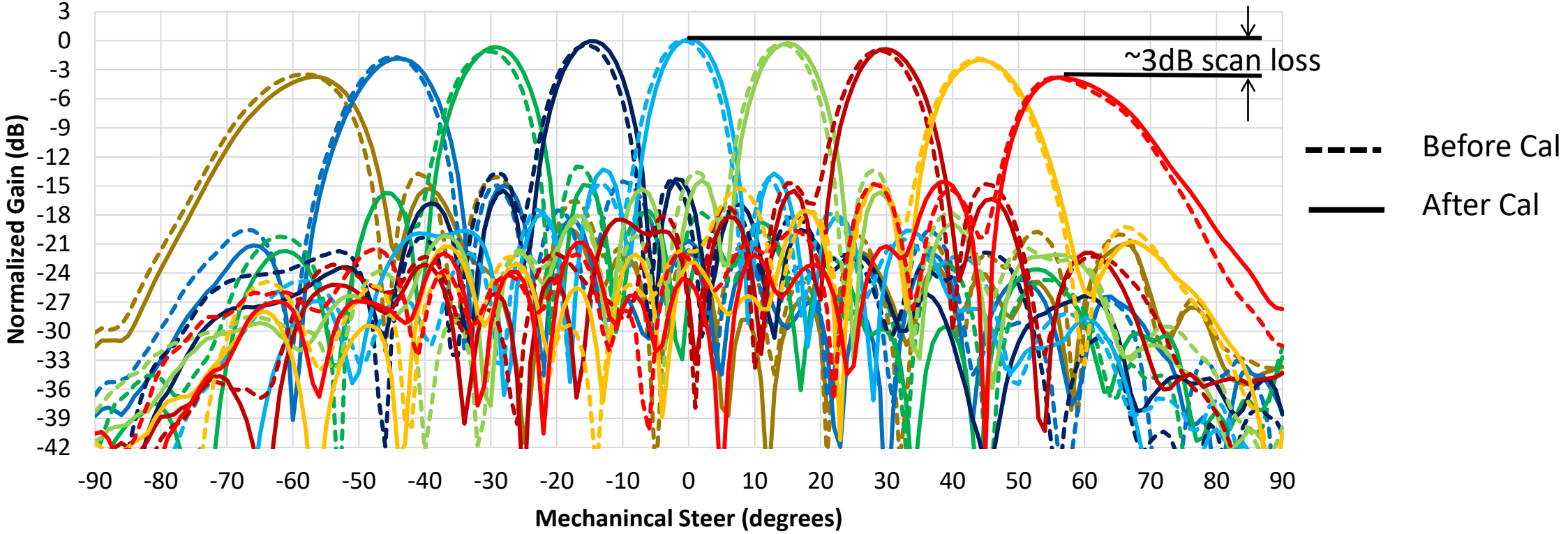


Antenna Side



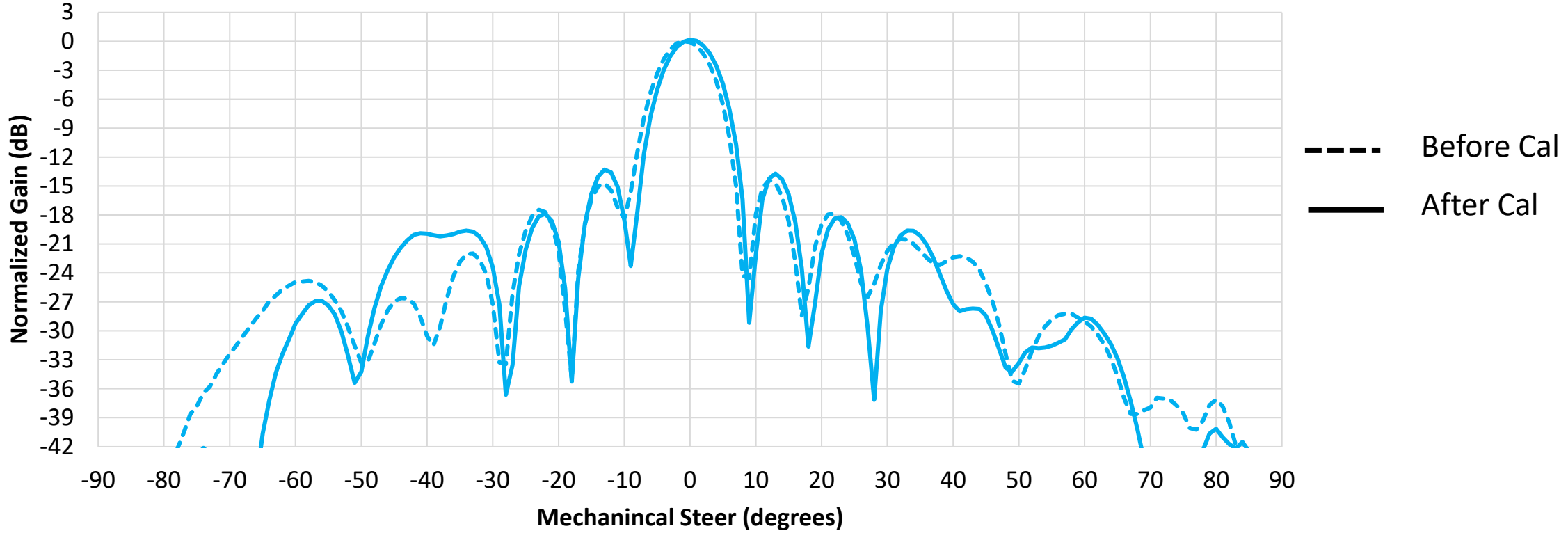
- Each BFIC channel feeds a dual band Tx/Rx antenna element
- Patented circularly polarized antenna element doesn't require an external polarizer
- Design achieves <3dB axial ratio for both the Tx & Rx bands under ± 60° scan

Gen 1 Ku-band: CP Rx Pattern across azimuth scan angles before and after calibration



- Design achieves ~3dB scan loss across ± 60°

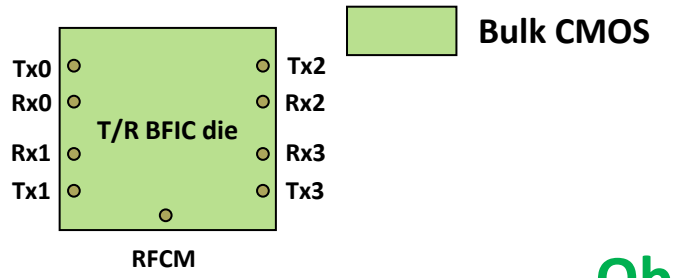
Gen 1 Ku-band: CP Rx Pattern across azimuth scan angles before and after calibration



- Design achieves ~3dB scan loss across ± 60°
- Array Calibration improves beam pointing error, null location/depth and side lobe balance

GEN2 BFIC Architecture/Technology Selection

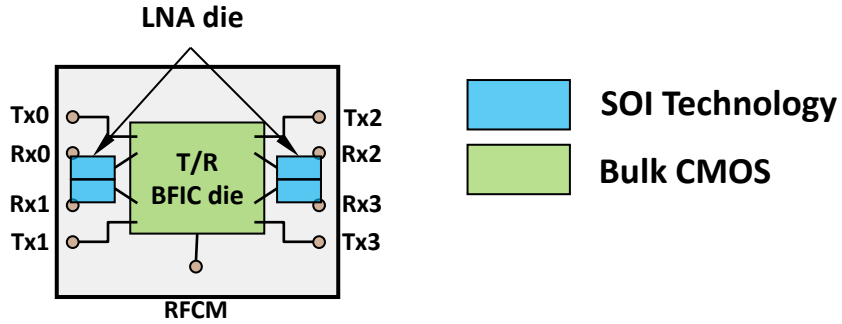
GEN 1:



GEN1: T/R BFIC

Objective is minimizing overall system cost!

GEN 2:

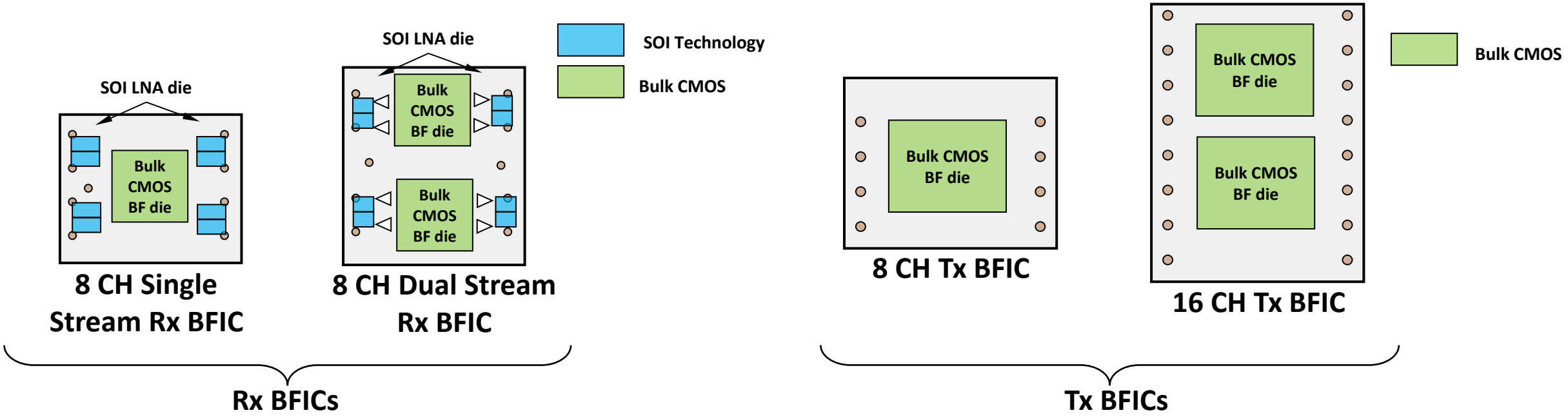


GEN2: T/R BFIC

- Fully integrated BFIC on low-cost bulk CMOS technology
- Flip chip bare die BGA
- Technology & Packaging choices dictated by desire to minimize BFIC cost

- SOI Technology with low NF was selected for LNA to achieve competitive G/T
- BFIC including VGA/VM kept on low-cost bulk CMOS technology
- Split architecture allowed using filters between LNA and BFIC to reject the Tx band leakage
- Flip chip laminate-based BGA was used to assemble the 3 dies

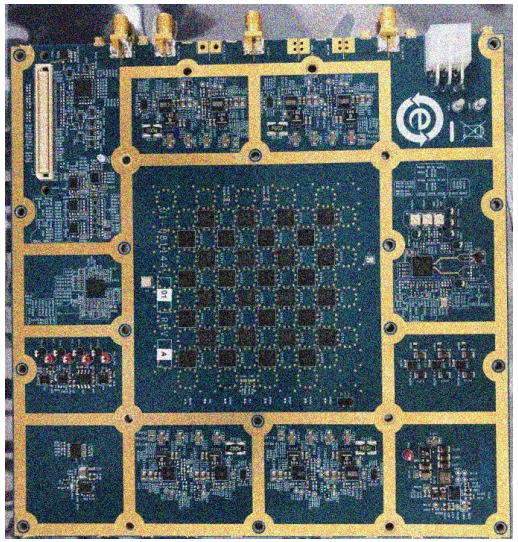
Gen 2 FDD Rx & Tx BFICs



- Same split technology approach was used to build 8 CH FDD Rx ku/ka BFICs
  - Enables increasing capacity by adding a splitter in the laminate to design a Dual stream Rx required for MC NTN networks
- Due to the low P1dB requirement the Tx ku/ka BFIC were designed on bulk CMOS

Gen 2: Ka FDD Tx & Rx Array using Same Ant. Aperture

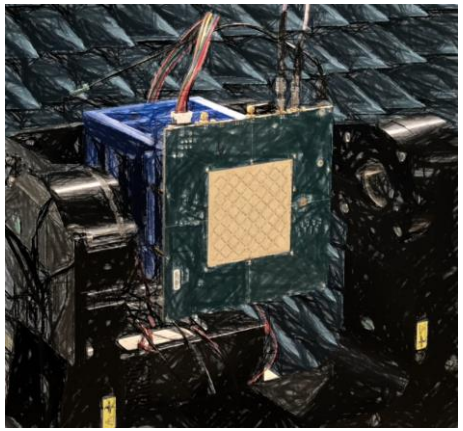
Component Side

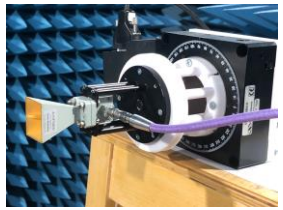


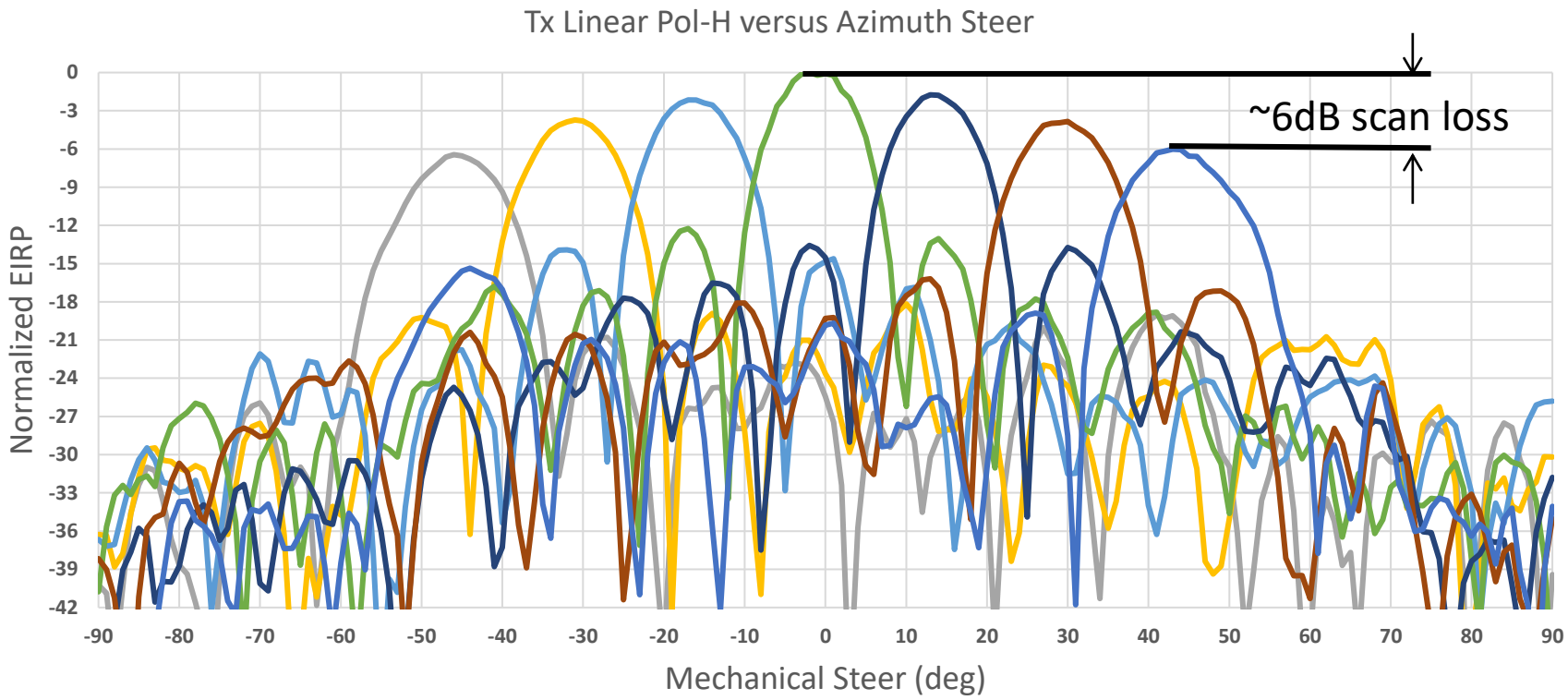
Antenna Side

- 16 Rx & Tx BFICs are interleaved to design an FDD array using the same Tx/Rx antenna aperture
- Array also include frequency up/down conversion & power solution
- PCB filters are also included to improve Tx/Rx isolation for FDD operation

Gen 2 Ka-band: TX Linear Pol Patterns Measurements







- Scan loss was limited by DRCs due PI & SI requirements not by the element design
- Working on improving scan range/loss beyond ±45^{o} in 2nd spin of the array design

Conclusion

- Lowering Rx NF is key to commercializing NTN leading to:
  - Smaller array size, BOM, & lower cost
  - Less power consumption & less expensive heat sink solutions
- Splitting the LNA and the Rx BFIC into different dies provides more flexibility for technology selection & utilizing Tx reject filtering
- Tx P1dB & Pdiss needs to be optimized based on array size, higher P1dB might not always be better!
- On-chip digital calibration techniques can reduce array test times to help cut array production cost