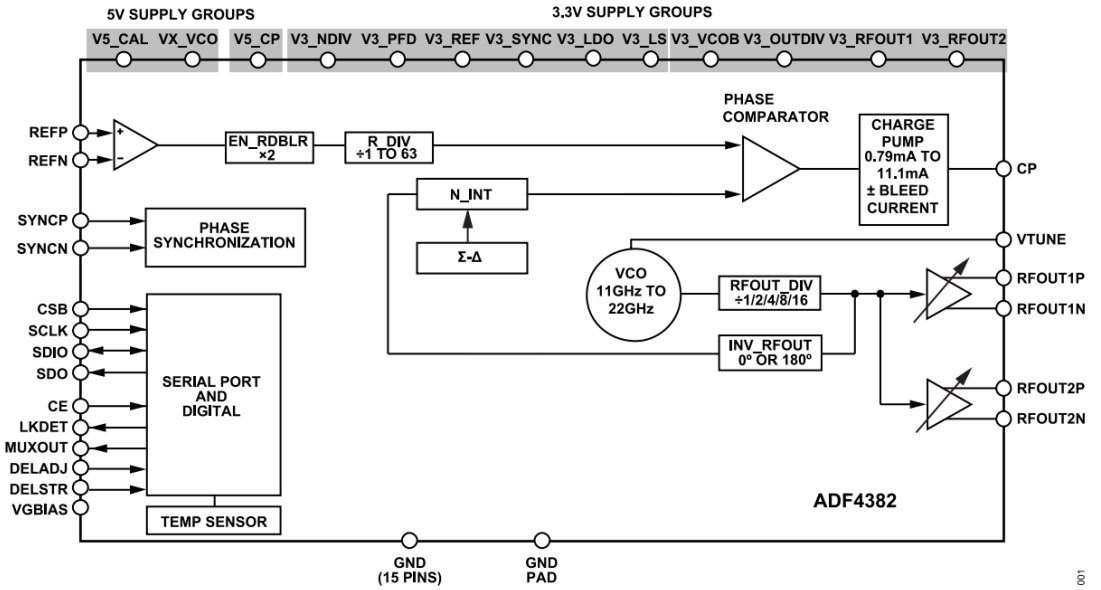
ADF4382 FAST CALIBRATION FEATURE

Kieran Barrett and Jude Osemene
Analog Devices

ADF4382 Overview

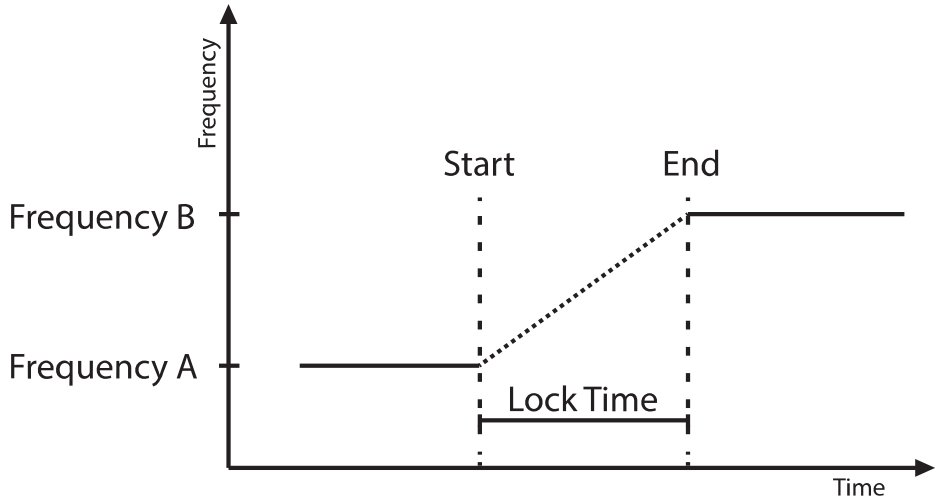
- Integrated fractional PLL frequency synthesizer
- Excellent temperature stability of 0.06 ps/˚C
- **Fast calibration** feature for fast lock times

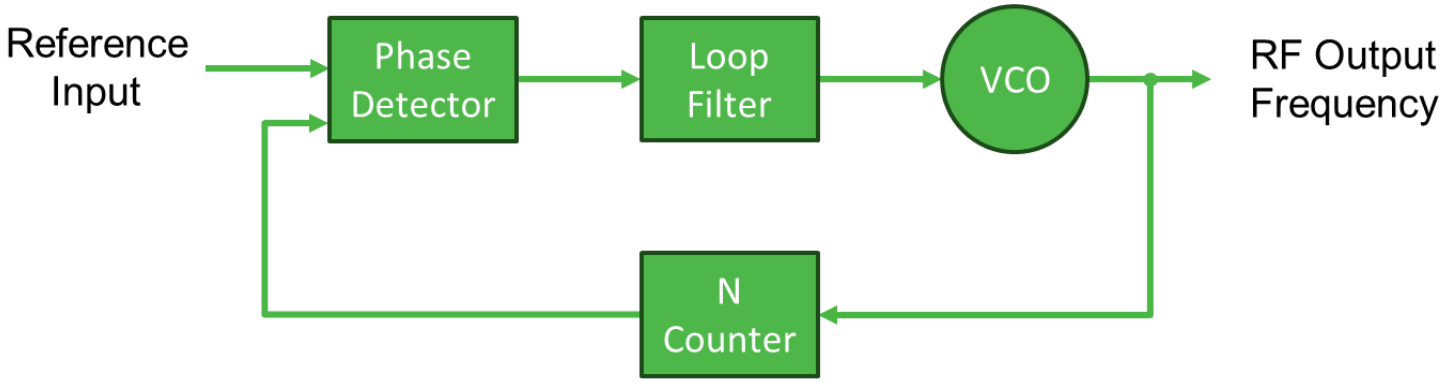
- Variants Octave Range:
  - ADF4382 : 11GHz to 22GHz
  - ADF4382A : 11.5GHz to 21GHz
  - ADF4383 : 10GHz to 20GHz



PLL Basics: Lock Time

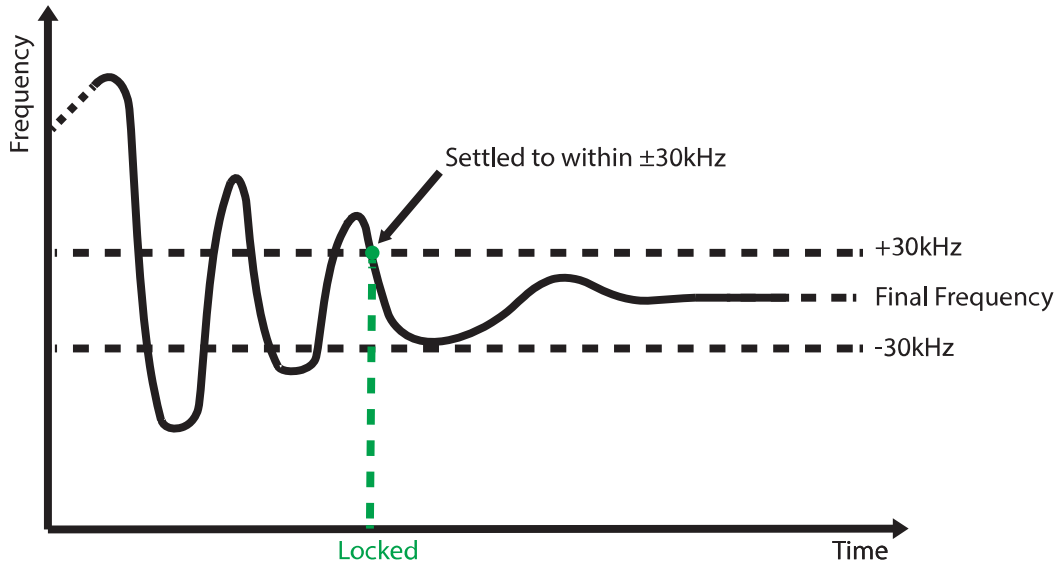
- Lock time is the time taken to lock to the frequency and phase of the reference when switching between two frequencies
- The start point is the point at which the frequency begins to change
  - This is typically after a register write to the device
- End point is determined by the lock time criteria





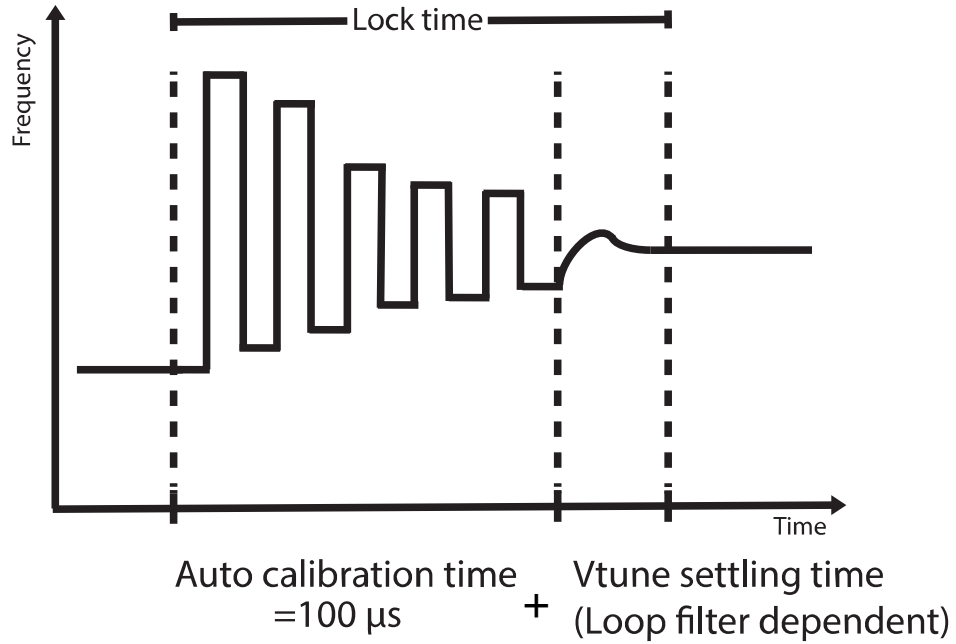
Lock Time Criteria

- The point at which the device is determined to be locked varies, depending on user application
- This threshold may be a frequency, phase, or tuning voltage settling window
- The threshold value used may be 1ppm, 10ppm or an absolute frequency or phase window
- 30kHz settling window example:



Lock Time Components

- Two main components of lock time:
- **VCO Auto Calibration:**
  - Multi-band VCO architecture requires calibration routine to digitally select suitable core and band for selected frequency (100µs)
- **Loop Filter Settling Time:**
  - V_{TUNE} settling time through the loop filter
  - Depends on loop filter bandwidth used

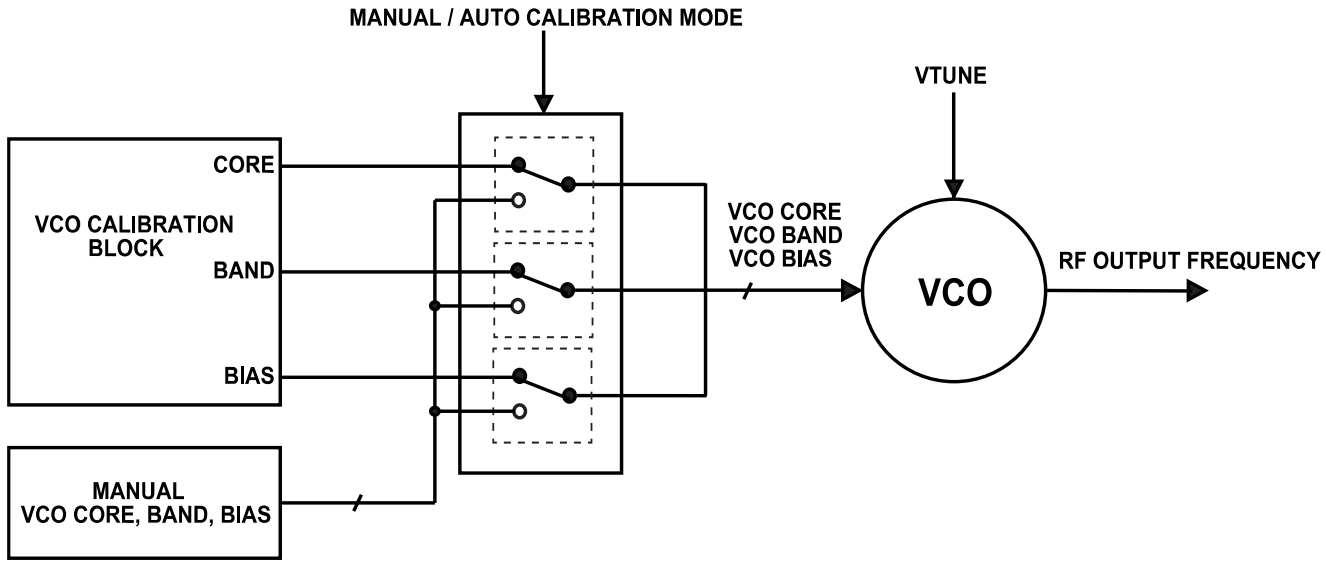


Existing Methods: Manual Calibration

- First perform an autocalibration for each frequency after initialization
- At each frequency, the corresponding core, band, and bias value is read back from the device and stored externally
- Stored core, band, and bias for each frequency can be manually written for each frequency for shorter lock time

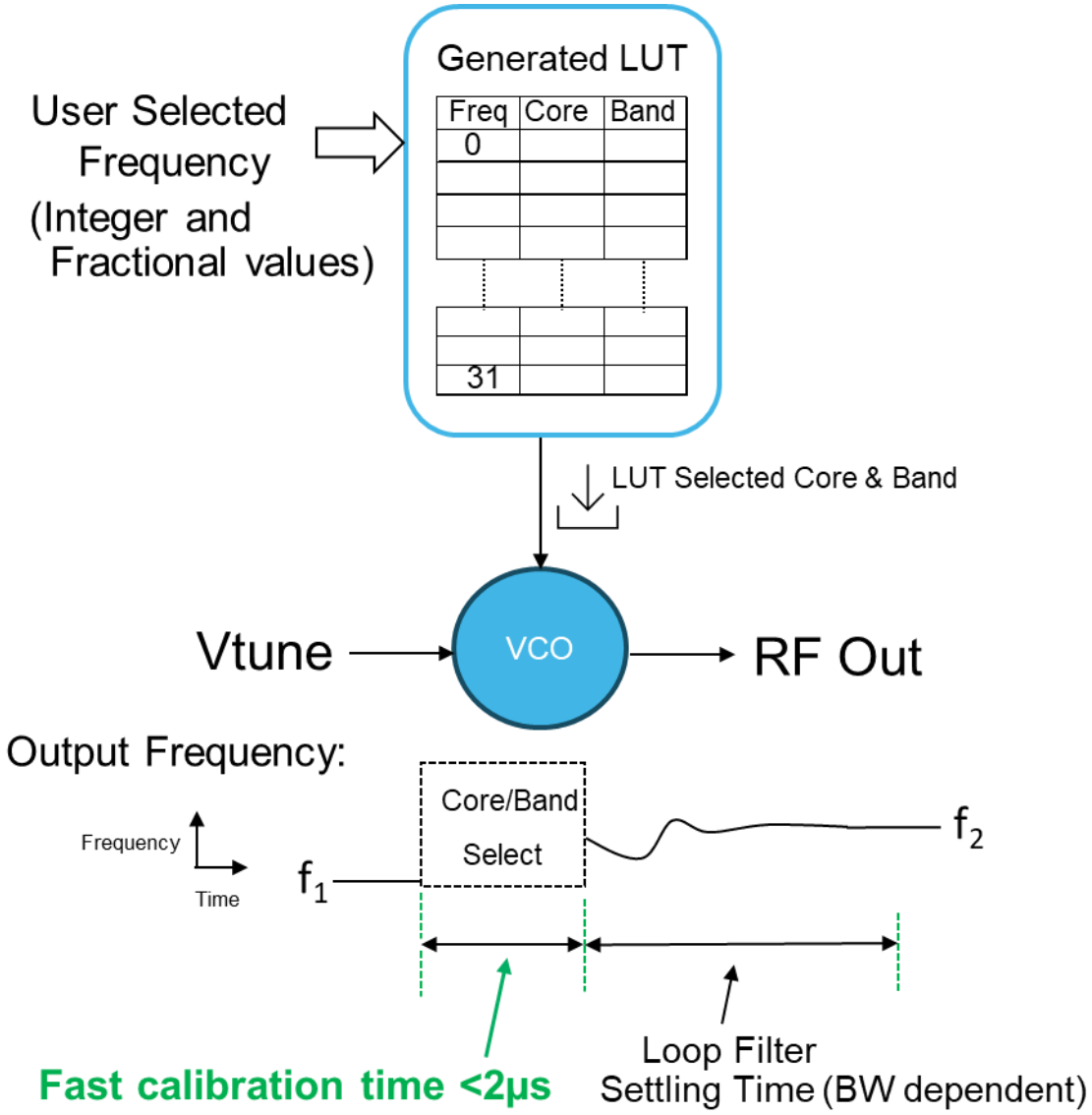
Disadvantages:

- Complexity of storing external values
- Number of register writes



Fast Calibration Overview

- Look-up table (LUT) contains core, band values
- Interpolation at output frequencies during fast calibration
- Fast Calibration reducing overall lock time to <10µs (Bandwidth 30kHz)

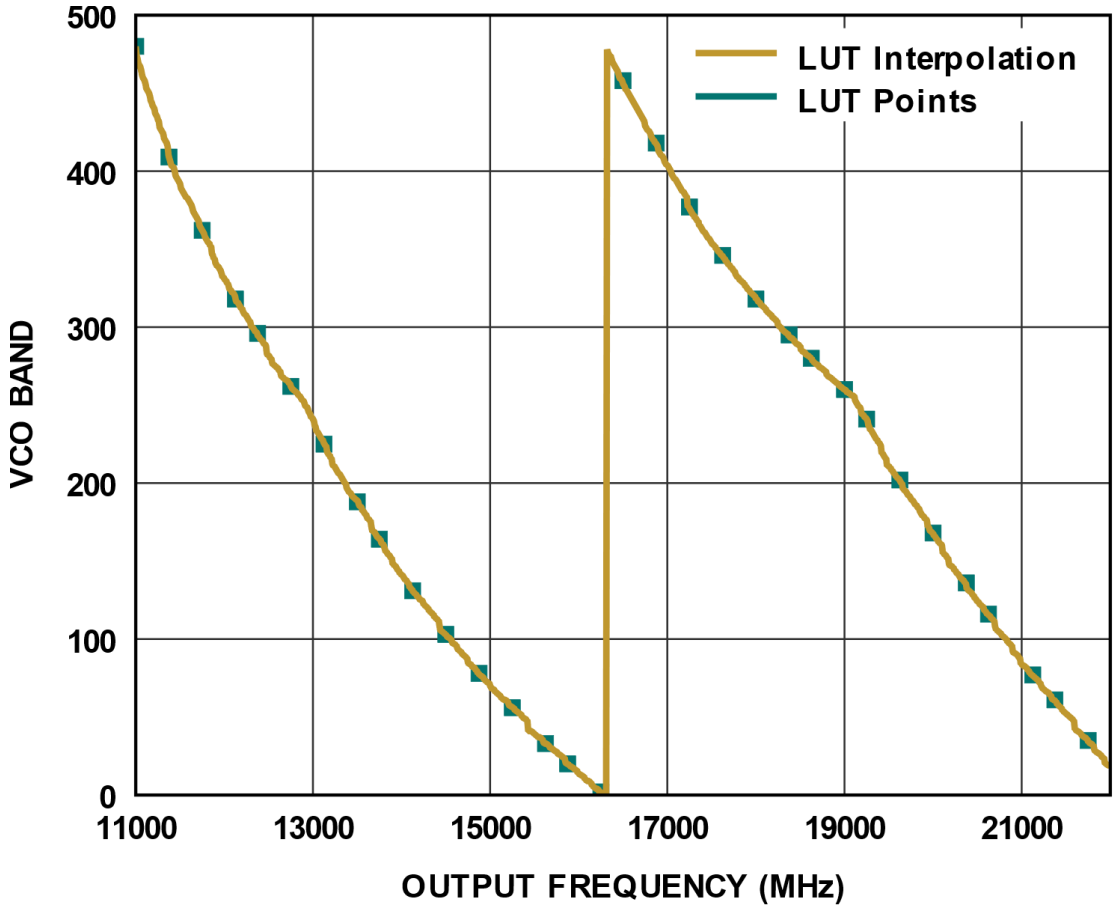


Fast Calibration Outline Procedure

1. Initialize device with default initialization
2. Enable Fast Calibration Routine
3. Auto calibration is performed across 32 points across octave range
4. Look-up table stores 32 core, band and bias values with N counter values
5. After LUT has been built, the fast calibration routine interpolates most suitable VCO values
6. Fast Calibration must be reinitialized after **+/- 20°C** temperature change

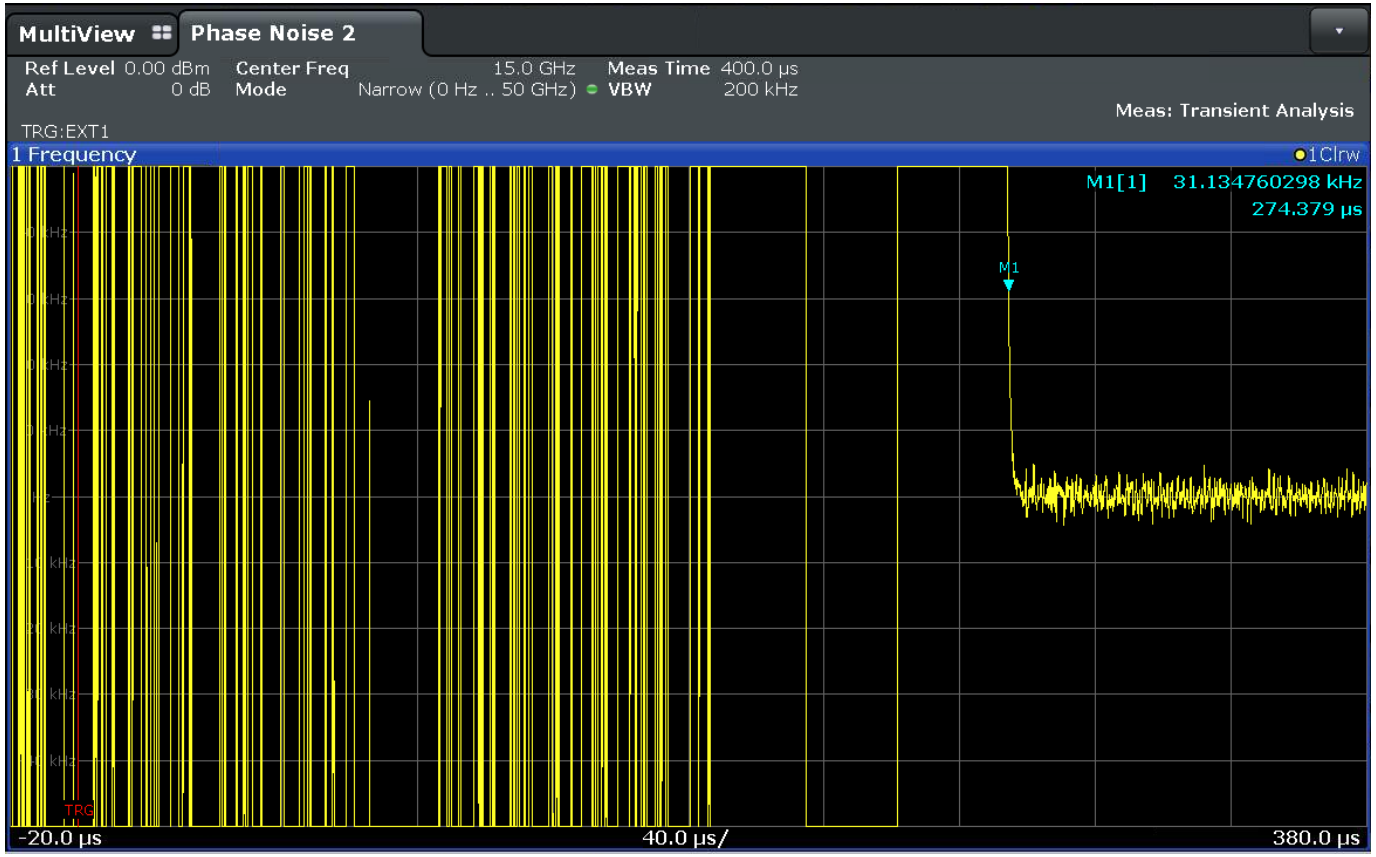
VCO Interpolation

- Auto calibration stores VCO values for 32 points in on-chip memory
- Result shows octave range of ADF4382 (11GHz to 22 GHz)



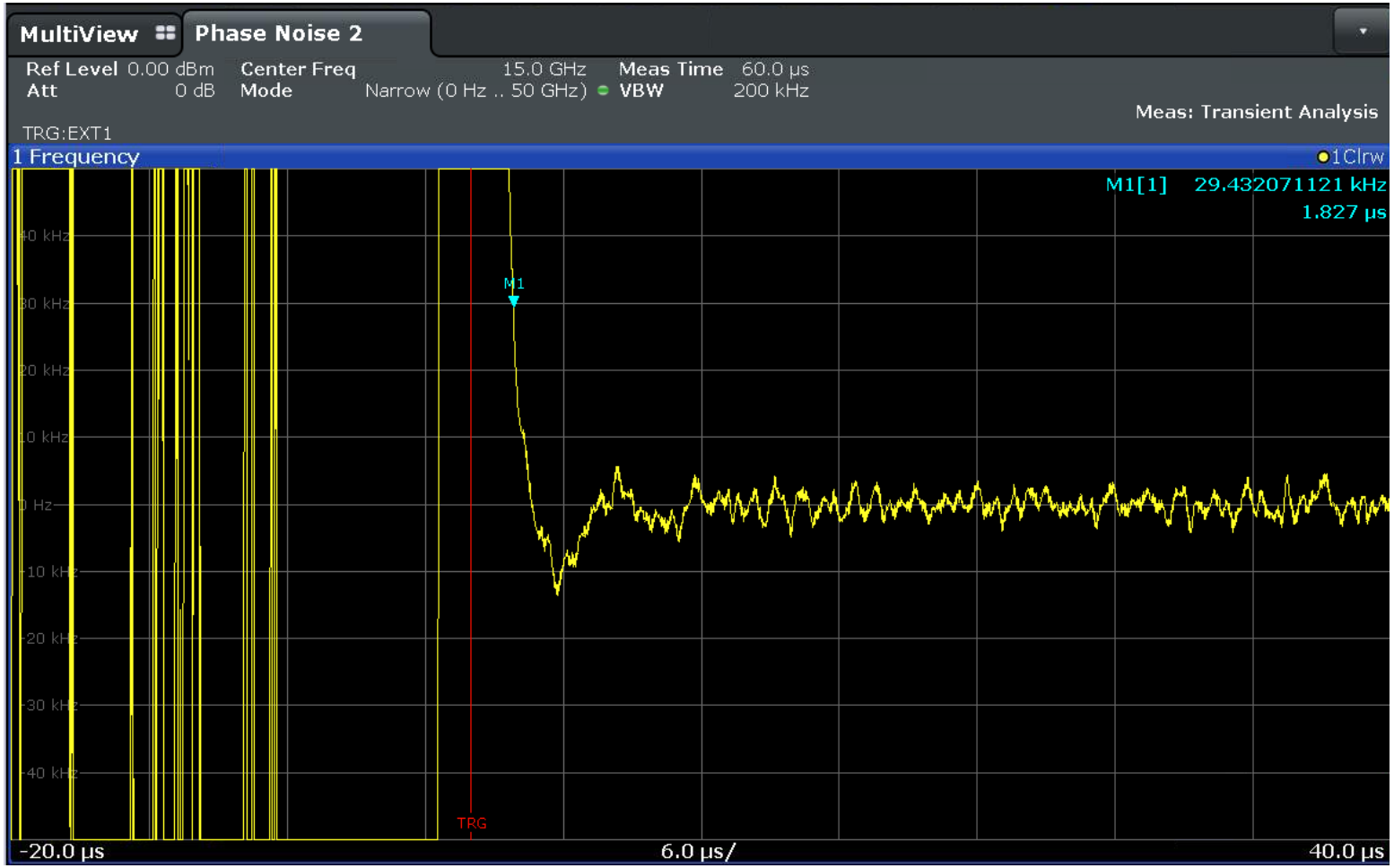
Results – Auto Calibration

- 12GHz to 15GHz : 274.4 µs



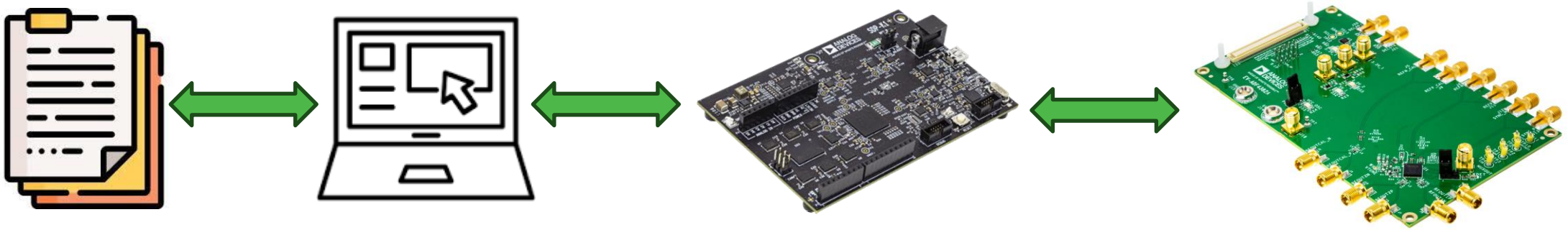
Results – Fast Calibration

- 12GHz to 15GHz : 1.8 µs



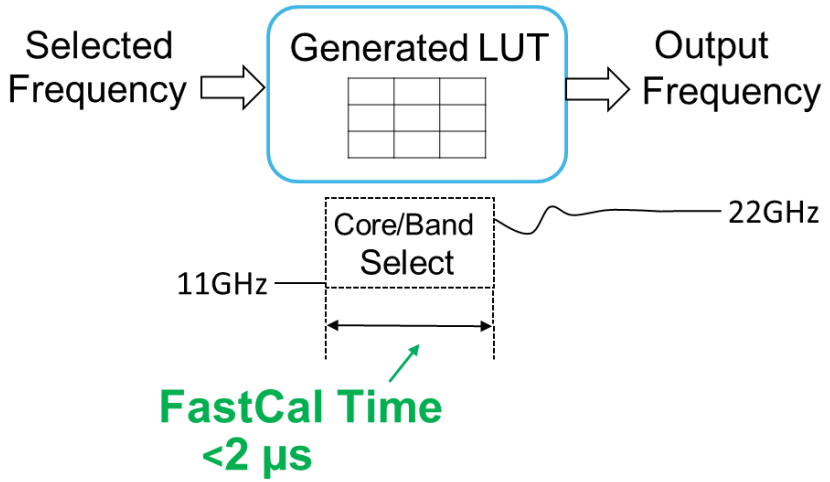
Supporting Collateral

- Upcoming release of detailed fast calibration Application Note for detailed explanations and theory
- Software driver provided which includes supporting Fast Calibration functions
- ADI evaluation boards can be readily used to evaluate fast calibration



Key Takeaways

- Fast Calibration uses 32 point look-up table built after device initialization
- Interpolation routine provides core, band, & bias value for frequency selected
- Fast Calibration significantly reduces PLL lock time
  - Calibration time reduced to <2µs
  - Lock time reduced to <10µs (+/-30kHz)
- Lock and Leave range of +/-20°C
- Available on all variants: ADF4382/83/82A



Thank You

- **Any Questions?**
- **Visit Analog Devices Booth #1243**