ZIF based SDR Transceiver as a new solution for Test, Measurement and Radar applications

Padraig Mc Daid

Over a decade of Transceiver Technology Leadership

WIRELESS

- Comms Infrastructure
- Fixed Wireless Access
- General-Purpose Radio
- Distributed Antenna Systems
- Repeater

INSTRUMENTATION

- Portable Field Instruments
- Software-Defined Radios
- Wireless Test and Measurement Emulators
- RF Communication Testers

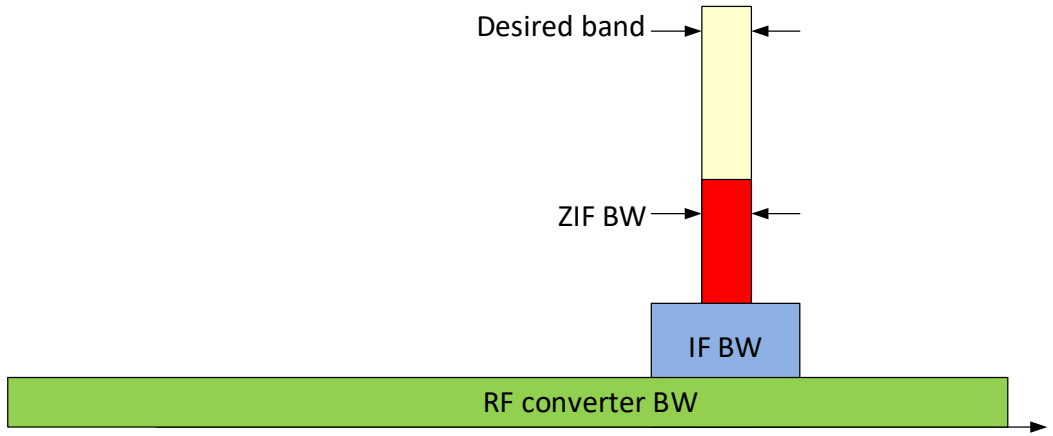
AEROSPACE & DEFENSE

- Portable and Secure Radio Communications
- Electronic Warfare
- Military Communications
- Phased Array Radar
- Drone Detection

INDUSTRIAL AUTOMATION

- Portable and fixed
- Industrial Testers
- UHF RFID Readers
- Energy Smart Metering

Why Zero-IF (ZIF) Transceiver and Direct RF based solutions?



Analog Devices Supports both Zero-IF and High Speed Converer approaches to ensure support of multi-market application requirements.

Zero-IF (ZIF) Transceivers

- ‘Any band’ functionality
- Capture/synthesize bandwidths of up to 600MHz+
- Lowest power consumption within these operational bands
- No “image bands”—simplifies out of band filtering
- “QEC Calibration” to realize high performance over broadband signals

High Speed (Direct RF) converters

- ‘Every band’ functionality
- Capture/synthesize bandwidths of > 1GHz
- “digitally assisted analog” provides enhanced dynamic range performance
- Provides flexible system solution

Three new Product Releases available now on ADI website

ADRV9032R

ADRV9022

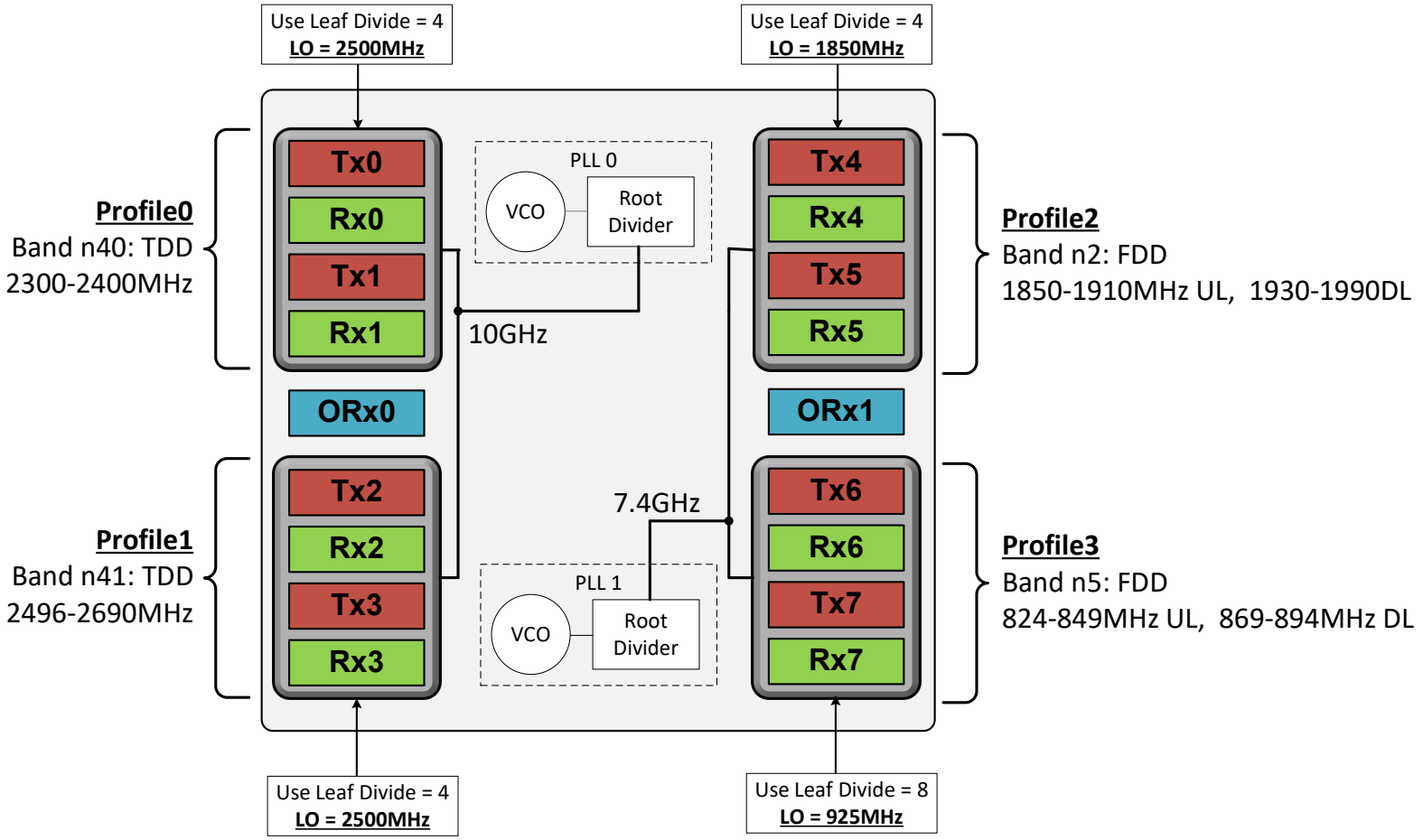
ADRV9042

Part Number	ADRV9032BBPZ-2T1	ADRV9022BBPZ-4T1	ADRV9042BBPZ-8T1
Configuration	2T2R2ORX	4T4R2ORX	8T8R2ORX
RF Range	350MHz to 7.225GHz	10MHz to 6.1GHz	500 MHz to 7.455 GHz
Bandwidth Support	200 MHz	200 MHz	400 MHz
Tx Large Signal BW	200 MHz	200 MHz	660 MHz, LO > 1200 MHz
Tx Synthesis BW	450 MHz	450 MHz	800 MHz, LO > 1200 MHz
ORx BW	450 MHz	450 MHz	800 MHz, LO > 1200 MHz
DFE Support?	N/A	DPD/CFR	DPD/CFR/CDUC/CDDC
DPD Support BW	N/A	200 MHz	400 MHz
Interface (Number of Lanes)	16 Gbps JESD204B/C (8 lanes)	24.33 Gbps JESD204B/C (4 lanes)	14.74 Gbps JESD204B / 24.33 Gbps JESD204C (8 lanes)
Package Size	19 x 18.5 mm BGA	14 x 14 mm BGA	27 x 20 mm BGA
Power Consumption (example Use Case)	4.82W (200MHz TDD)	6.89W (200MHz TDD)	10.44W (100MHz, TDD)

*All products also support Multichip synchronization (MCS) and External LO input

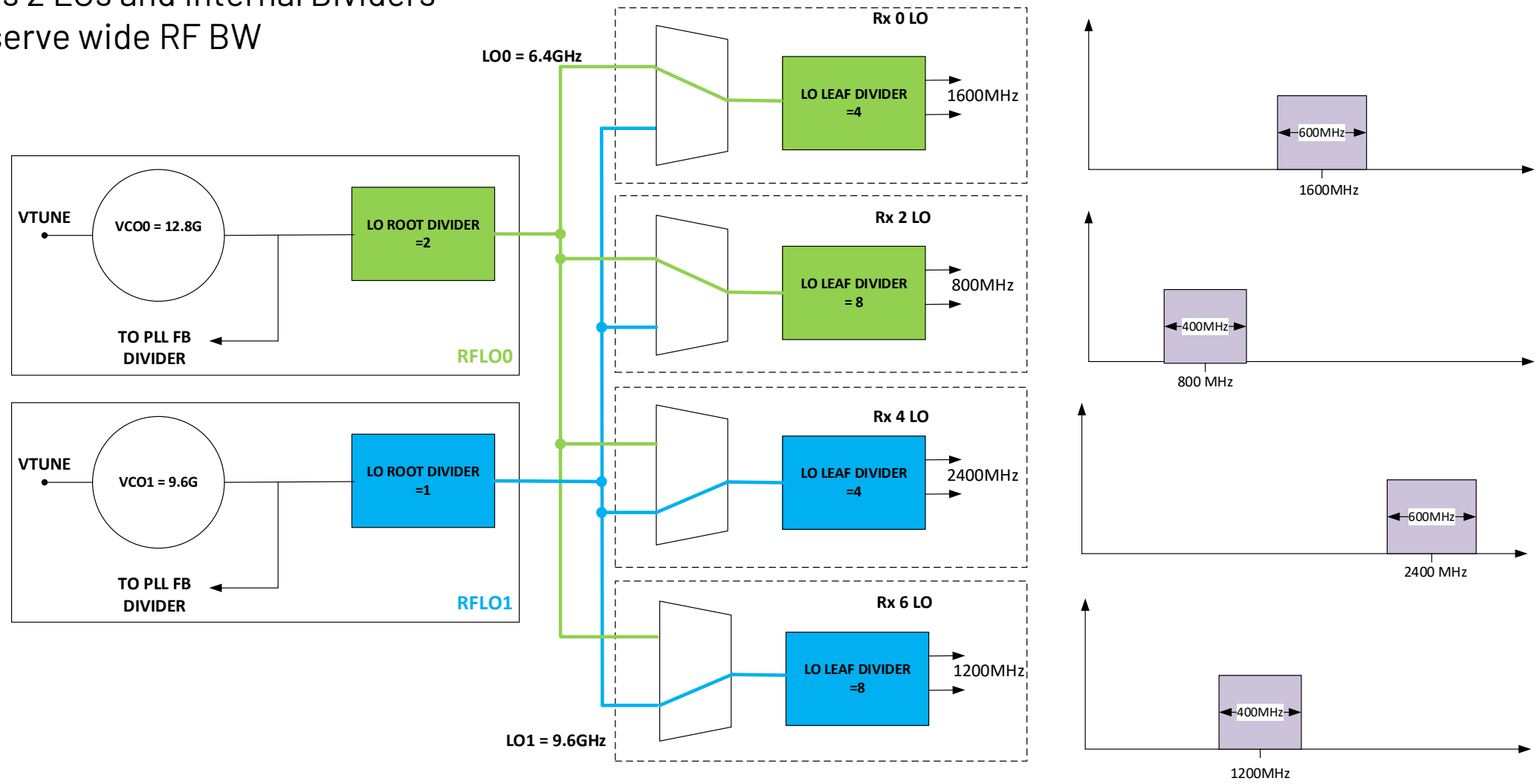
LO Placement Solution for use case (example using ADRV9042)

- ADRV9042 has 2 LOs - can set to 4 LO locations, and leaf divide each by factor of 2/4/6/8. This provides a great deal of flexibility for multi-band support.
- Example shows how ADRV9042 can enable a 4x2T2R use case supporting 4 bands (n2, n5, n40, n41)
- Based on Tx-Orx mapping state, Orx channel NCO setting will change to ensure observation of desired Tx band



See ADI Demo-station: Muti-Channel Spectrum Sensing LO Setup

Utilizes 2 LOs and Internal Dividers
to Observe wide RF BW



Multichip Synchronization (MCS) Operational Details

MCS boots up a single chip to a repeatable phase offset

Within a single chip, all Tx and Rx channels boot up to a repeatable phase offset from boot to boot.

Every Tx / Rx will have the same phase after MCS. So Tx0 on TRx1 will have the same phase as Tx0 on TRx1, TRx2 etc. Same for Rx's.

MCS aligns multiple transceivers in a system.

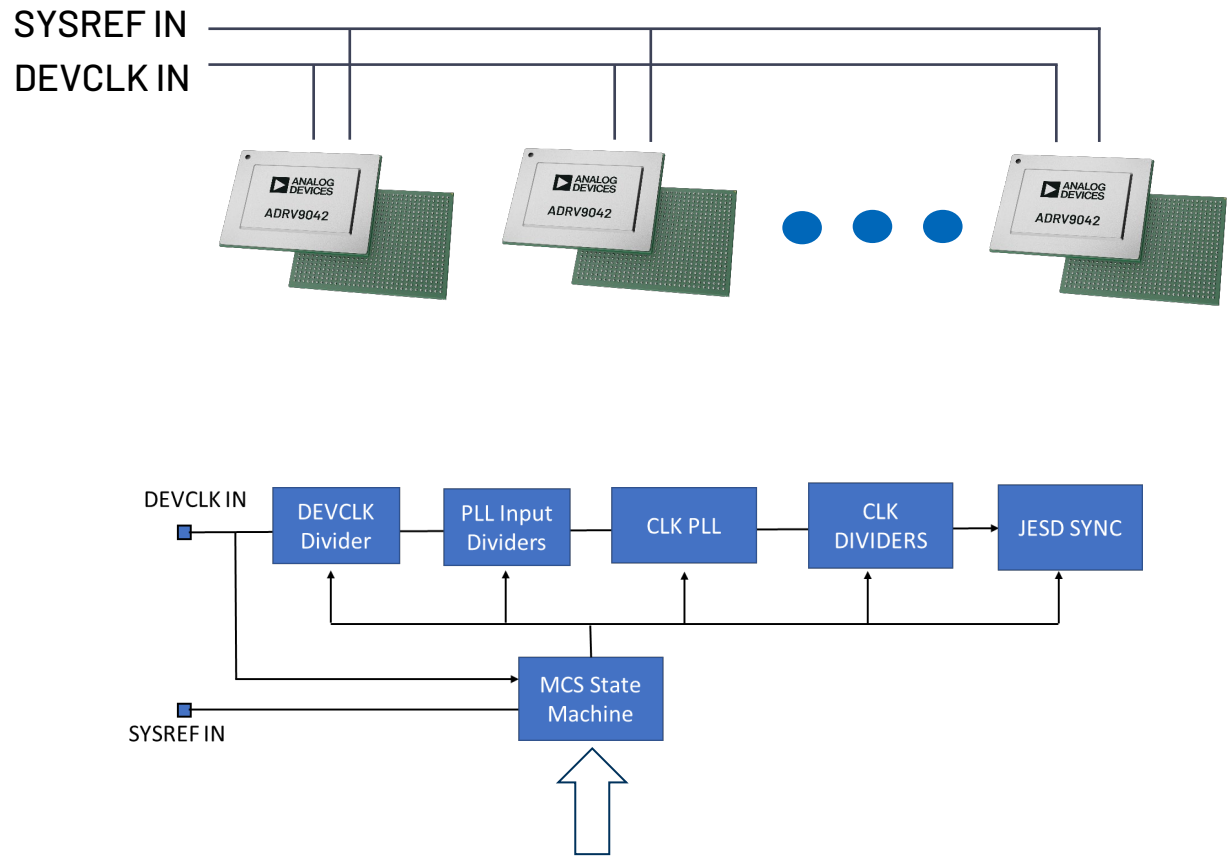
The on-chip MCS enables a deterministic latency, that is repeatable from boot to boot, for the full data path through the TRx.

MCS sequence performed in multiple stages

Each one initiated with a SYSREF rising edge

MCS is across full LO Tuning Range

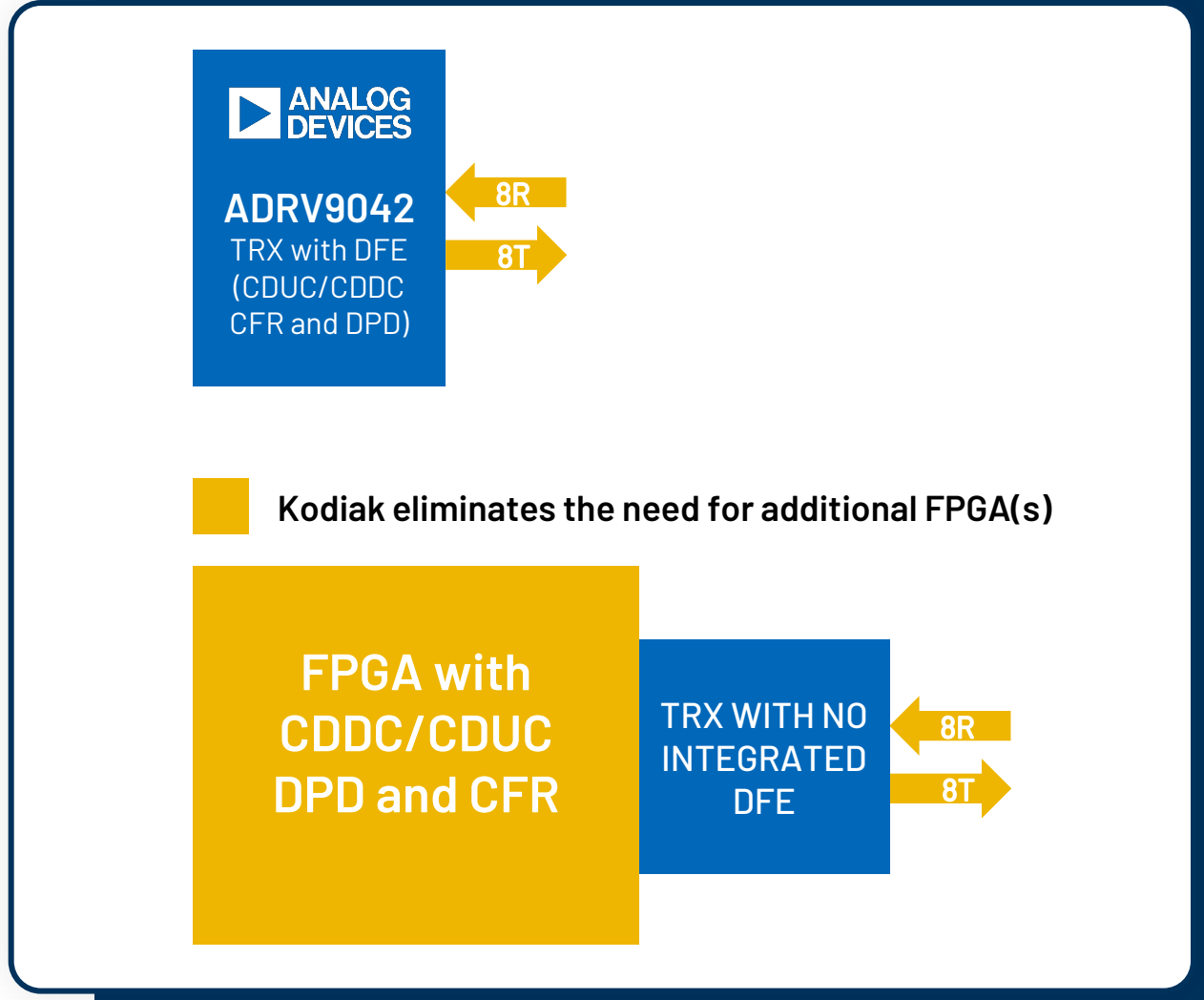
Palma, Maui, and Kodiak products



The (MCS) state machine resynchronizes the system reference signal (SYSREF) to the local device clock (DEVCLK) domain

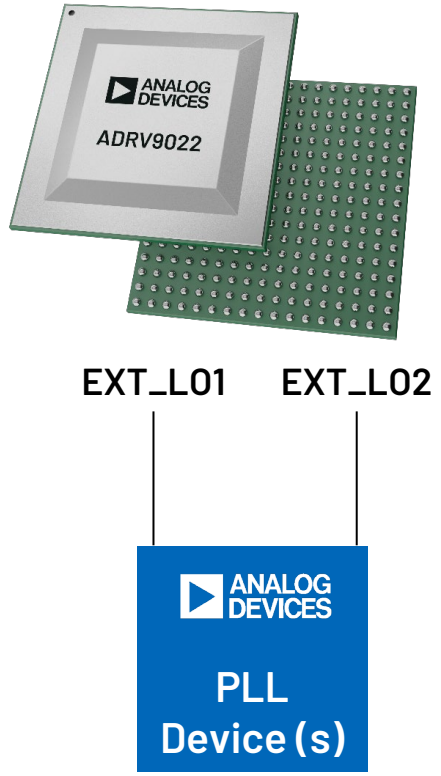
DPD Integration, Offloading Need from FPGA

- **DPD is valuable for signal source instruments, allows generation of power-efficient OTA signals**
- **ADRV9042 and ADRV9022 products remove the need for additional FPGA(s) or FPGA logic for these digital features**
  - ADRV9042 integrates CDUC/CDDC, CFR, and DPD (full DFE)
  - ADRV9022 integrates CFR and DPD



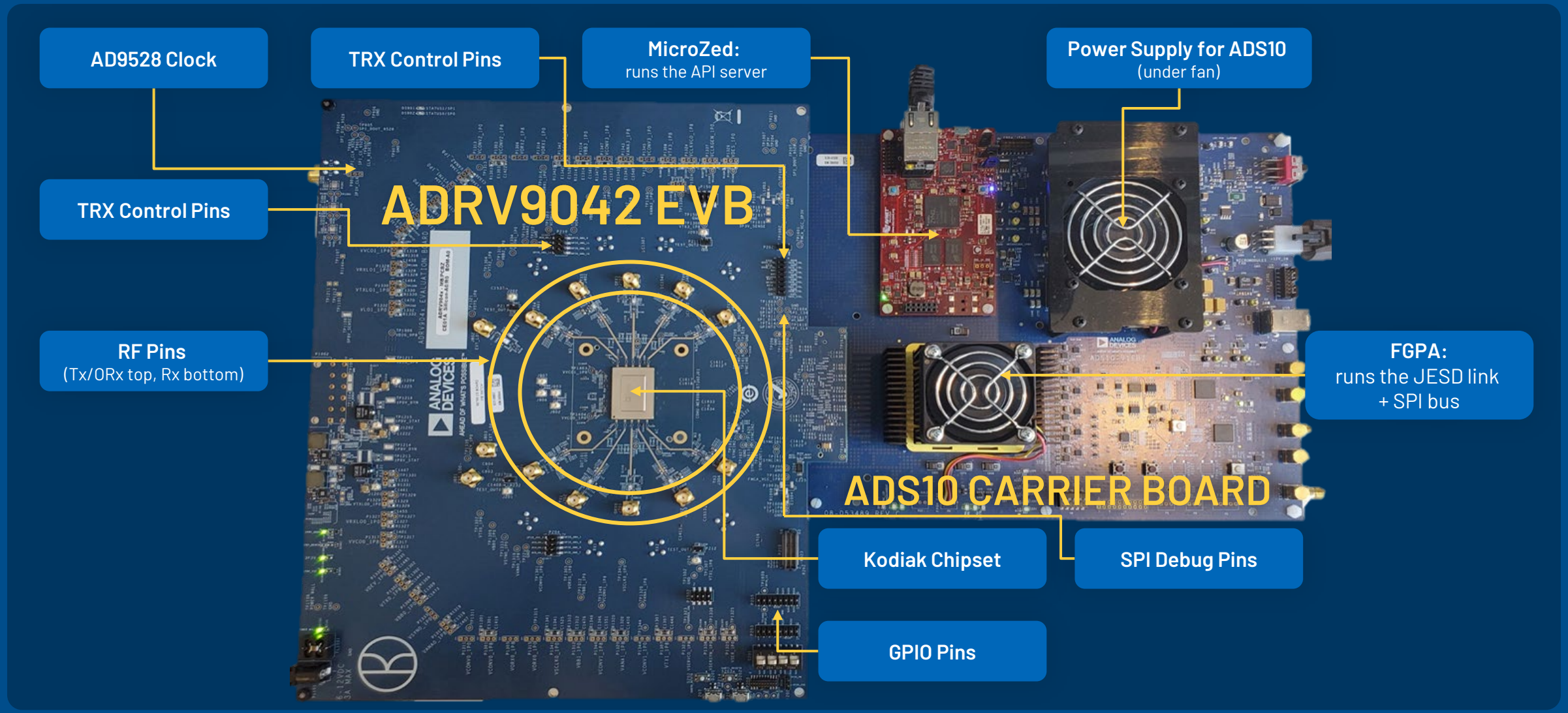
External LO Support on all devices

- **External LO is valuable for those applications demanding more stringent performance levels**
- **ARV9032R, ADRV9022, and ADRV9042 products all support external LO**
  - ExtLO frequency can be changed with device reset / power down
- **This approach can deliver improved phase noise performance**
  - LO phase noise level defined/set by external PLL chip



Each TRX provides two external LO inputs, allowing an external synthesizer to be used with the device

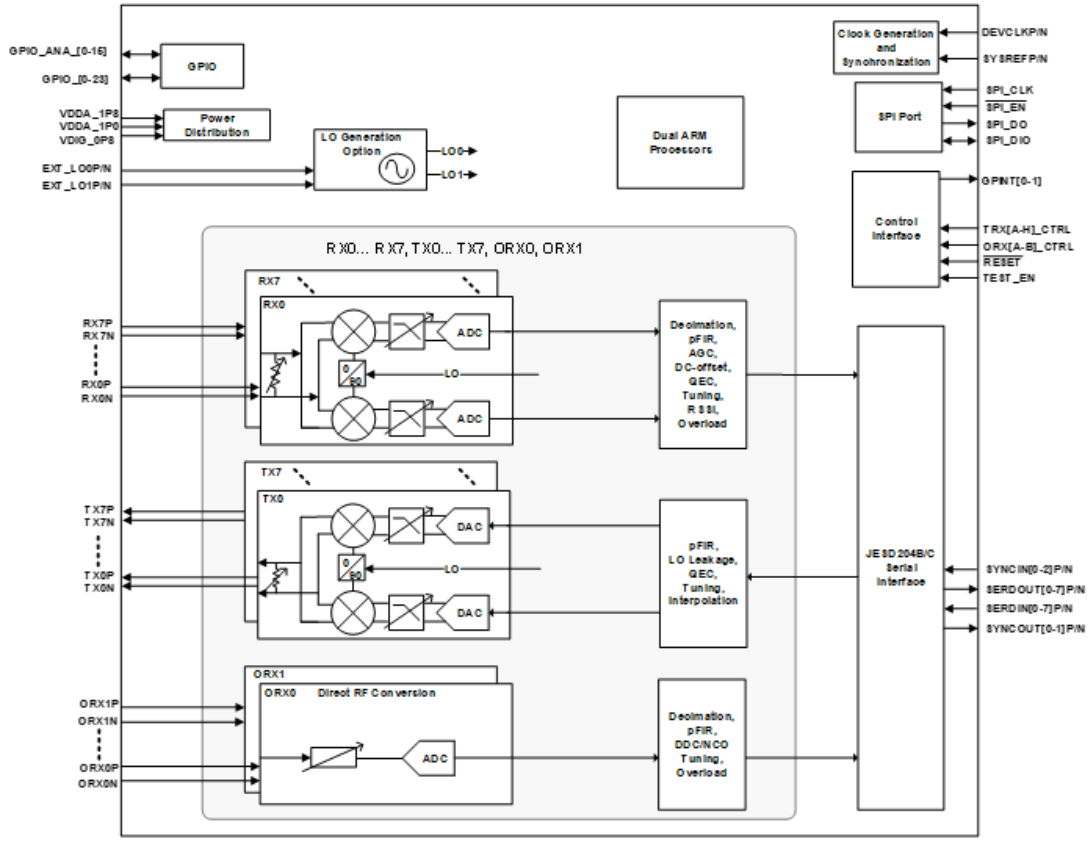
Evaluation Platforms available for all products



New Product ‘Paris’ overview

- Up to 8 Tx and 8 Rx Channels
- Up to 600MHz RF BW and beyond
- RF range supporting up to ~7.4GHz
- ~1W per channel power performance
- <0.5% Rx EVM Performance
- Multi-chip phase synchronization
- Wide Band Frequency Hopping
- Boot support
- 19 x 19mm package

Evaluation Board & samples available – contact Analog Devices local representative



Recap of the new Product Releases available now on ADI website

ADRV9032R

ADRV9022

ADRV9042

Part Number	ADRV9032BBPZ-2T1	ADRV9022BBPZ-4T1	ADRV9042BBPZ-8T1
Configuration	2T2R2ORX	4T4R2ORX	8T8R2ORX
RF Range	350MHz to 7.225GHz	10MHz to 6.1GHz	500 MHz to 7.455 GHz
Bandwidth Support	200 MHz	200 MHz	400 MHz
Tx Large Signal BW	200 MHz	200 MHz	660 MHz, LO > 1200 MHz
Tx Synthesis BW	450 MHz	450 MHz	800 MHz, LO > 1200 MHz
ORx BW	450 MHz	450 MHz	800 MHz, LO > 1200 MHz
DFE Support?	N/A	DPD/CFR	DPD/CFR/CDUC/CDDC
DPD Support BW	N/A	200 MHz	400 MHz
Interface (Number of Lanes)	16 Gbps JESD204B/C (8 lanes)	24.33 Gbps JESD204B/C (4 lanes)	14.74 Gbps JESD204B / 24.33 Gbps JESD204C (8 lanes)
Package Size	19 x 18.5 mm BGA	14 x 14 mm BGA	27 x 20 mm BGA
Power Consumption (example Use Case)	4.82W (200MHz TDD)	6.89W (200MHz TDD)	10.44W (100MHz, TDD)

*All products also support Multichip synchronization (MCS) and External LO input

AHEAD OF WHAT'S POSSIBLE

analog.com