ANALOG DEVICES

IWTu7: Designing a High-Fidelity Signal Chain from 0.1 to 55 GHz: Architectures, Components, and Integration Strategies

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analog.com

Goal and Agenda

Goals:

- Understand why wideband RF architectures are evolving, not just how
- Map data-converter capability directly to RF front end
- Make informed tradeoffs for wideband, high-dynamic range systems
- Understanding core technology that makes up wideband signal chains

Topics:

- Technology trends
- 0.1-55 GHz Architecture overview
- Amplifier/SIP packaging
- Up/Down conversion RFIC Integration
- Filtering Technology overview
- Data Converter Deep Dive

RF System Constraints

Diverse missions, shared RF Challenges

Extreme SWAP-C Pressure

- Smaller platforms
- Higher quantities
- Same Capability at reduced cost

Hardware Reuse Across Bands and Missions

- Common Hardware Platforms
- Software Defined
- Reduced sustainment costs

Edge Compute & Real Time Adaptation

- Processing at the edge
- Reduced Latency
- AI/ML-enabled optimization

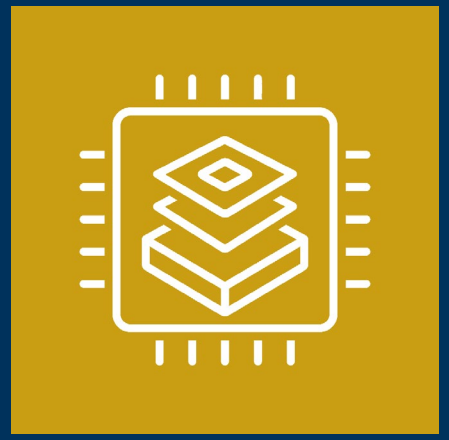
Spectrum Congestion and Interference

- Dynamic spectrum access
- Co-site interference, blockers, jamming

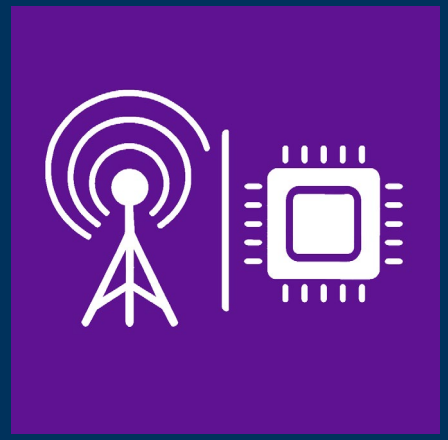
Key Technology Trends shaping the Future

Wideband & Multi-Function Architectures

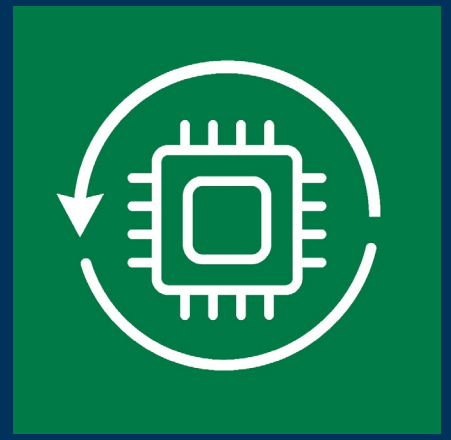
Advanced Packaging & Thermal Management



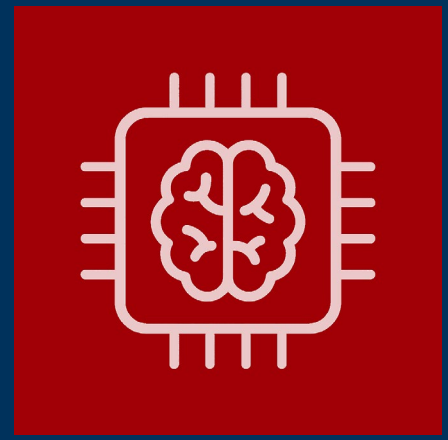
Advancing Data Converter Capability



Data Flow and Information Management



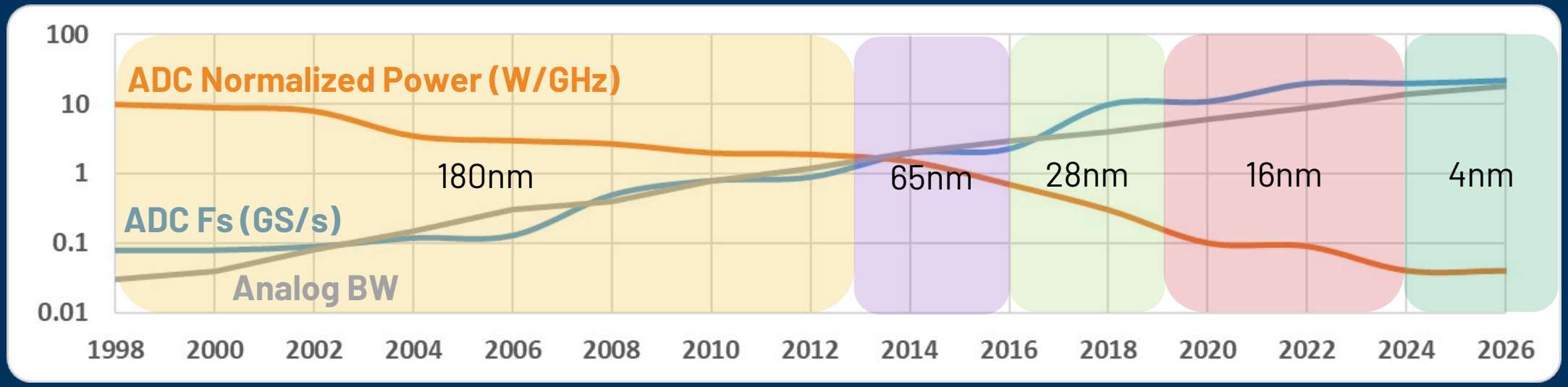
Cognitive & Adaptive AI/ML Operational Functions



All powered by cutting edge ADI antenna-to-processing innovations

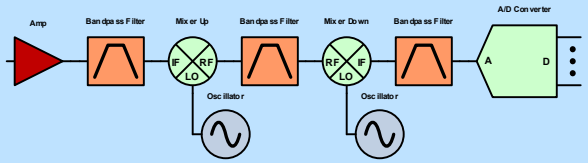
Customer domain expertise driven solutions

High-Speed Converter Progression : Dictates RF architecture

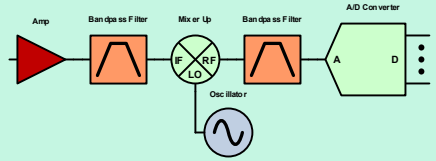


0.1-18 GHz

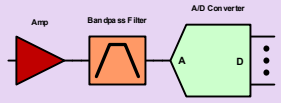
Dual+ conversion Super-Het



Single Conversion "High-IF"

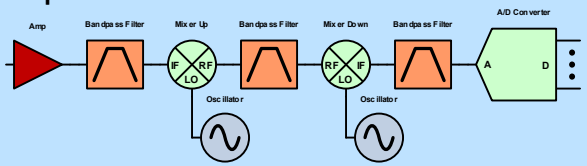


Direct Sample

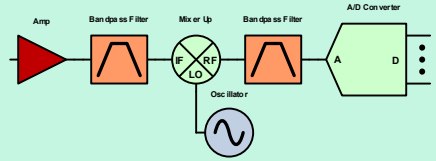


0.1-50+ GHz

Dual conversion Super-Het



Single Conversion "High-IF"



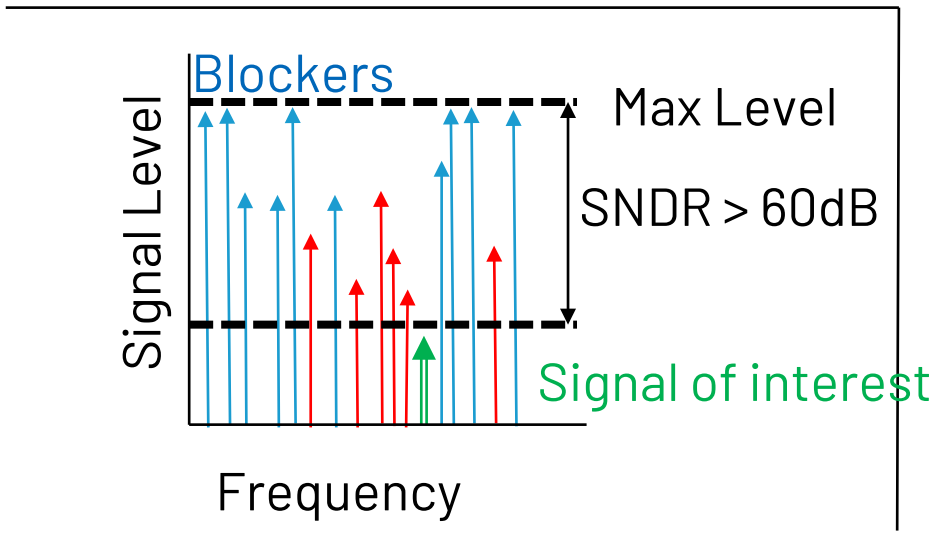
0.1-55 GHz Architecture

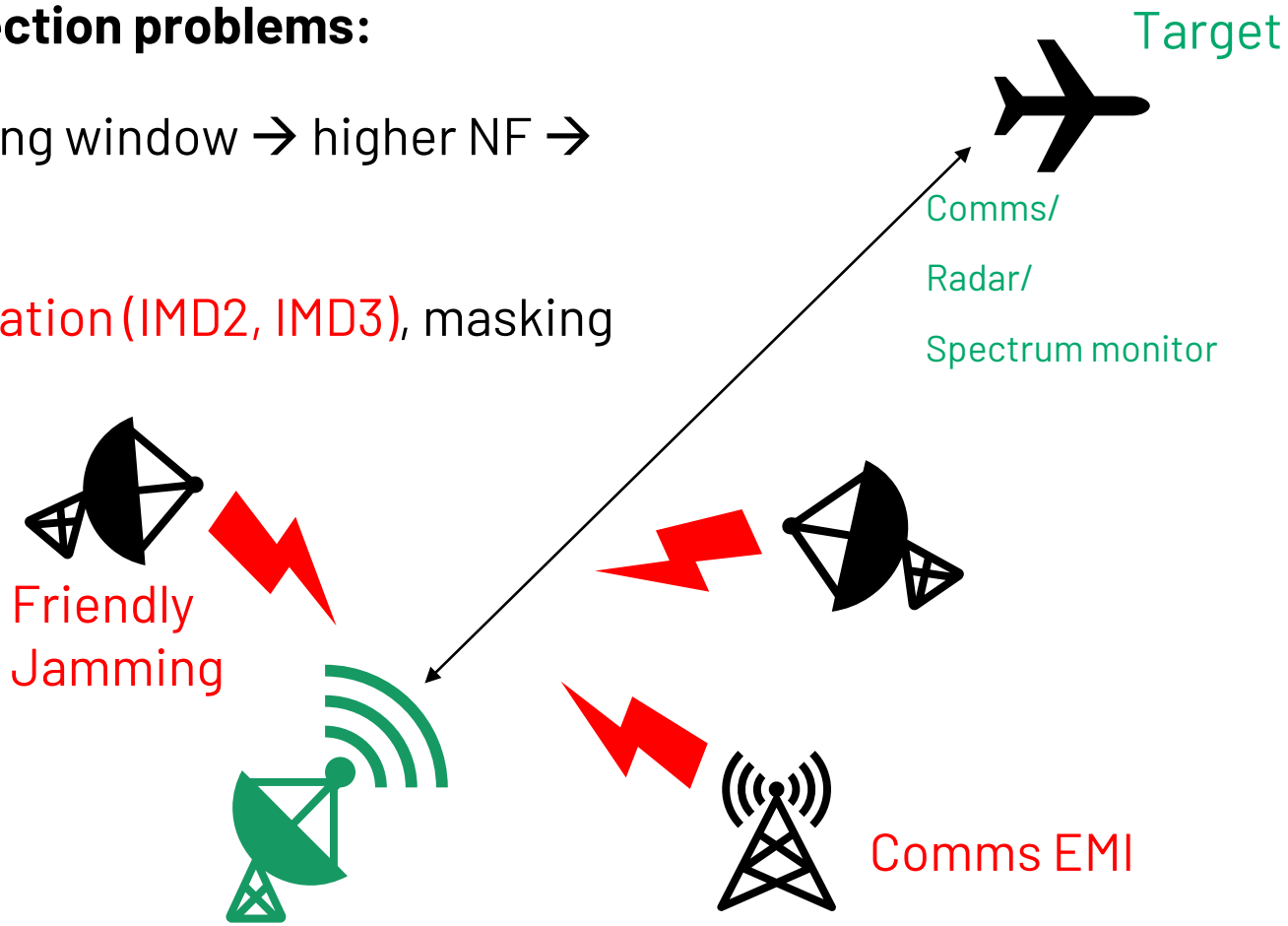
Challenge: Operating in Contested Environments

- Wideband RF systems are Signal-to-Noise-and-Distortion (SNDR) limited because **blockers create detection problems:**

  Blockers force higher SNDR operating window → higher NF → worse system noise floor

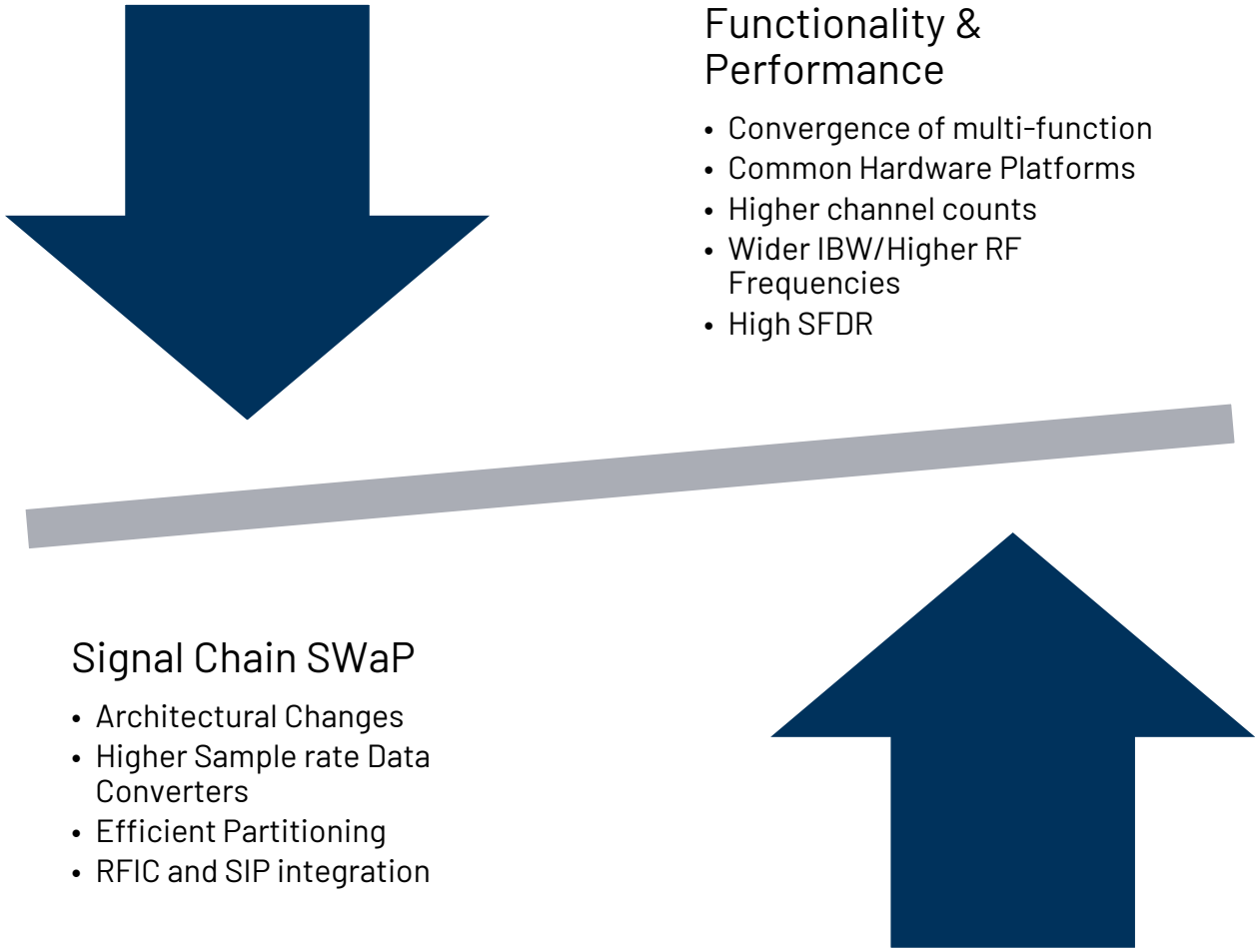
  Multiple blockers create intermodulation (IMD2, IMD3), masking Signal of Interest





Challenge: Reducing Size, Weight, and Power (SWaP)

Increasing functionality while decreasing SWaP Envelope



Functionality & Performance

- Convergence of multi-function
- Common Hardware Platforms
- Higher channel counts
- Wider IBW/Higher RF Frequencies
- High SFDR

Signal Chain SWaP

- Architectural Changes
- Higher Sample rate Data Converters
- Efficient Partitioning
- RFIC and SIP integration

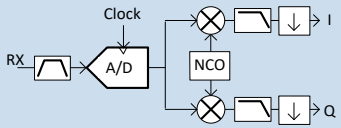
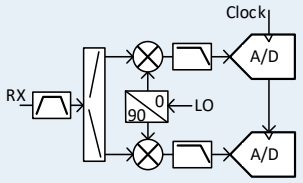
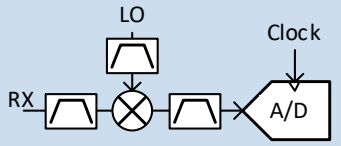
Low Frequency to 55 GHz signal chain Target Specifications

Parameter	Target
Frequency Coverage	0.1-55 GHz
Instantaneous Bandwidth	4 GHz
SFDR/SNDR	>60 dB
Noise Figure	<10 dB
Operating Power range	-120 to +20 dBm
Input no damage	+30dBm
Size	>50% reduction vs discrete solutions

To achieve this requires:

- Optimal architecture selection
- Gain ranging
- Careful frequency planning
- Filtering
- Optimized partitioning

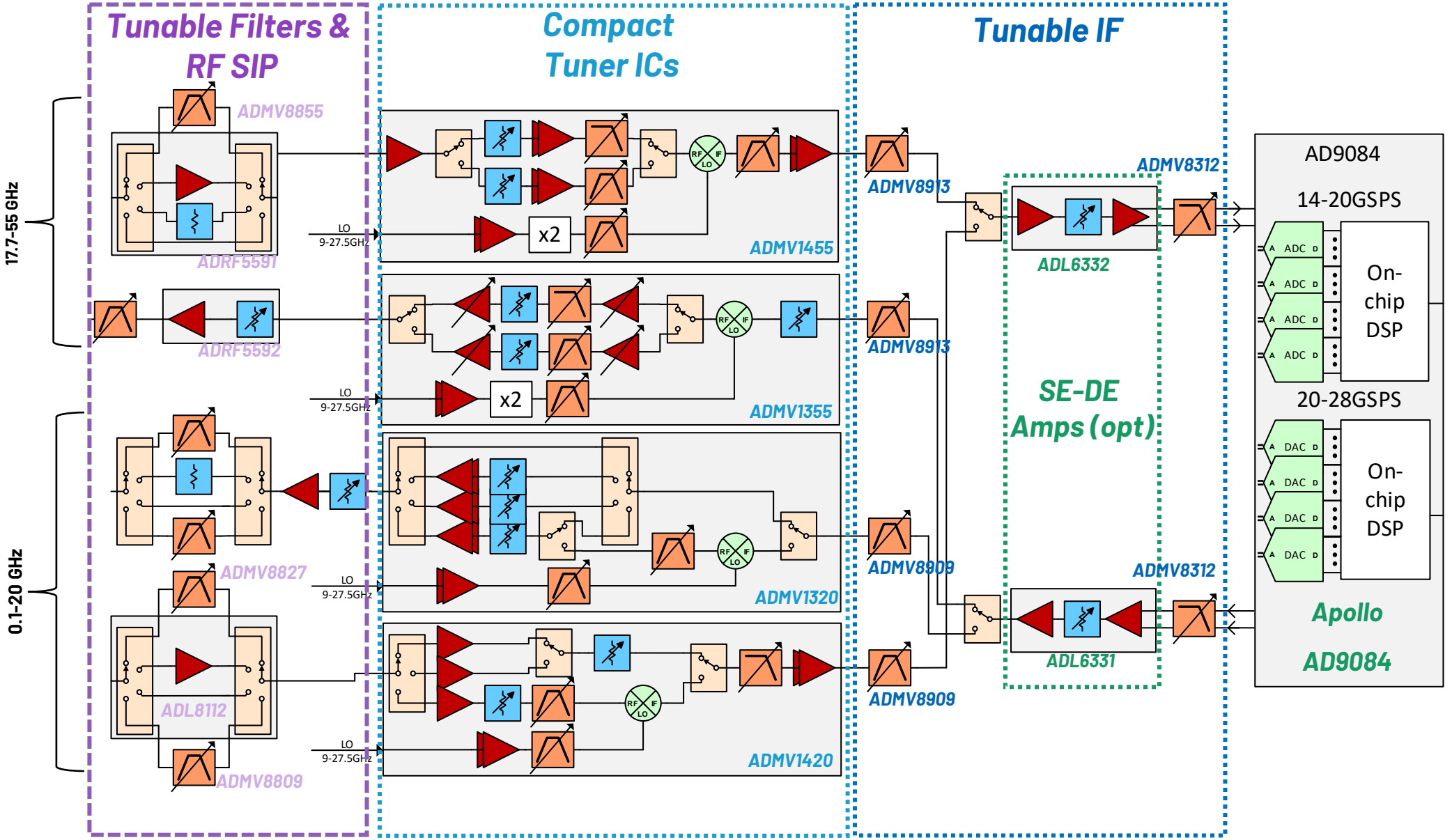
Architecture approaches to covering 0.1-55 GHz

	Architecture	Today's technology	Benefits	Challenges…	Technology Required for **55 GHz coverage**
	Direct Sample	~30 GHz	• Collapse RF chain	• Spur performance • Filtering Q at high frequency	• Extremely high ADC/DAC sample rates >110GHz • Extremely stable clock
	Zero-IF	~7 GHz	• Power efficient	• I/Q imbalance • Quadrature LO generation	• Wide-band I/Q Calibration • Quadrature LO gen up to 55GHz
	Super-Het w/ High-IF	>55 GHz	• Frequency coverage	• SWaP • LO Distribution • Frequency Planning	• Moderate ADC/DAC sample rates >20GSPS • High-IF operation

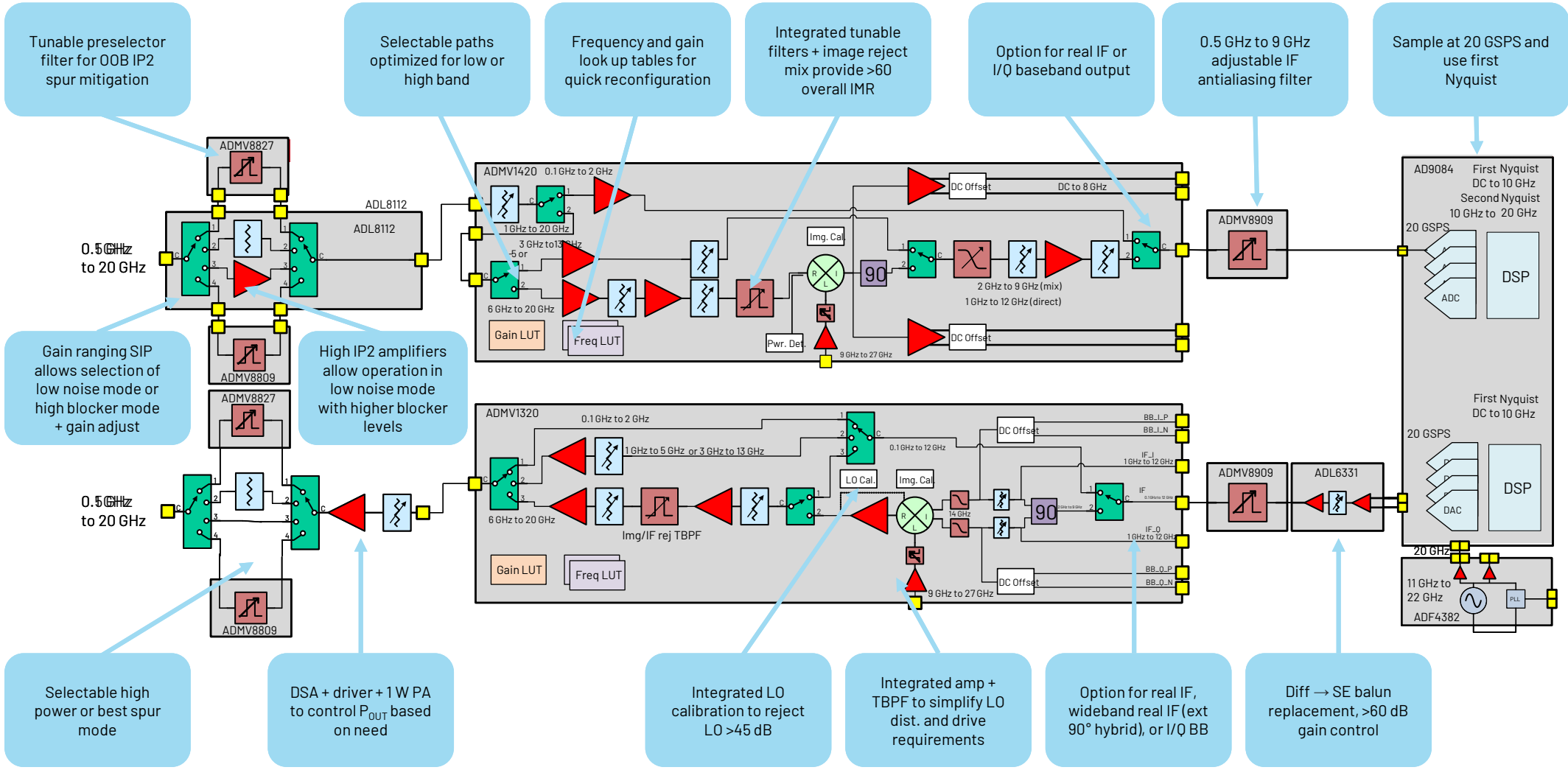
Hybrid: Use a combination of **Direct Sample** + **Super-het** to cover full frequency range

0.1-55 GHz Wideband Signal Chain Solution

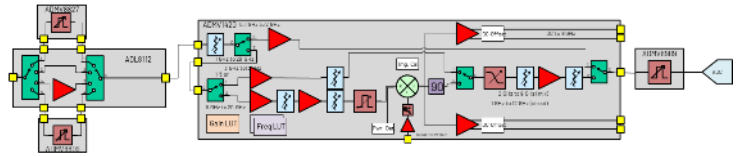
- Direct Sample + Frequency extension
- High-IF architecture for optimal frequency planning
- Partitioning for flexibility and optimal performance
- Reduced size through RFIC and System-in-package (SIP)



0.1 GHz to 20 GHz Receiver/Transmitter System Highlight

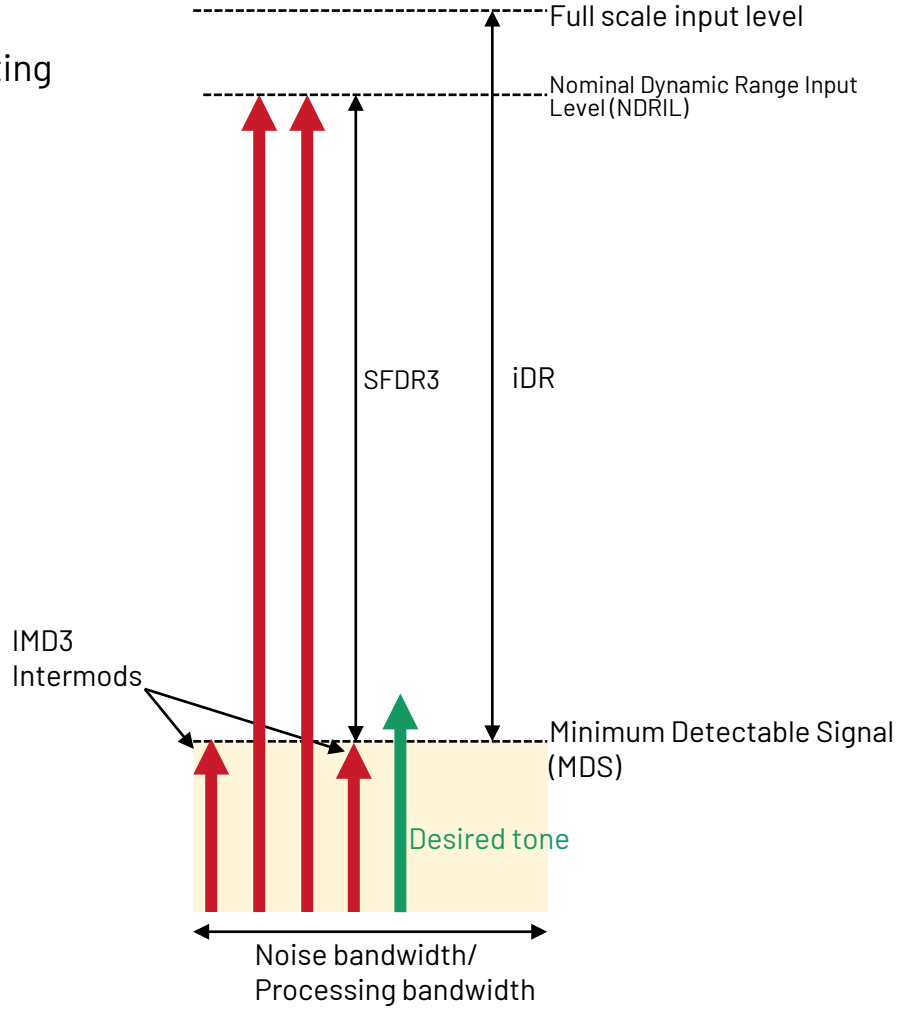


SFDR, SNDR, Spurs, Dynamic Range (Receiver)



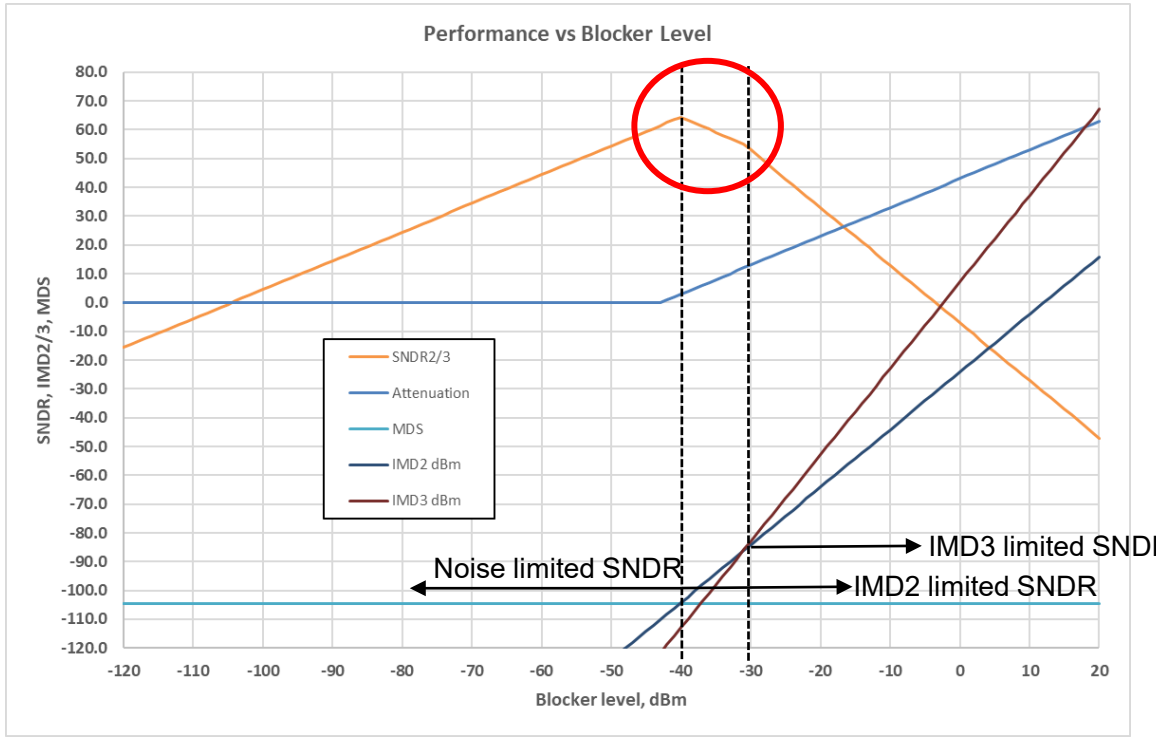
Concerns for managing interference:

- **Full scale input Level (dBm):** Maximum input level to signal chain before compressing/saturating
- **Minimum Detectable Signal (MDS):** Minimum Input level to signal chain, set by effective *noise bandwidth and noise figure*
  - ***Effective Noise Bandwidth*** *- set by DSP path and waveform type, typ values from 1MHz-1000MHz*
- **iDR (dB):** Instantaneous dynamic range. Input Full scale – Minimum Detectable Signal
- **SFDR3 (dB)**: Maximum Signal to noise and distortion ratio (SNDR) possible for a signal chain, function of *noise figure, IP3, and processing bandwidth*
- **SFDR (dB):** All other signal related spurs.
  - ADC harmonics, interleaving spurs
  - RF harmonics/intermods
  - Anti-alias rejection
  - Mixer MxN spurs, Image spurs (for super het)
  - IF rejection (for super het)
  - Sideband spurs (PLL/clock)
- **Nominal Dynamic Range Input Level:** Input level for maximum SNDR (MDS + SFDR)
- **SNDR (dB):** Signal to noise and distortion ratio, changes based on input signal level

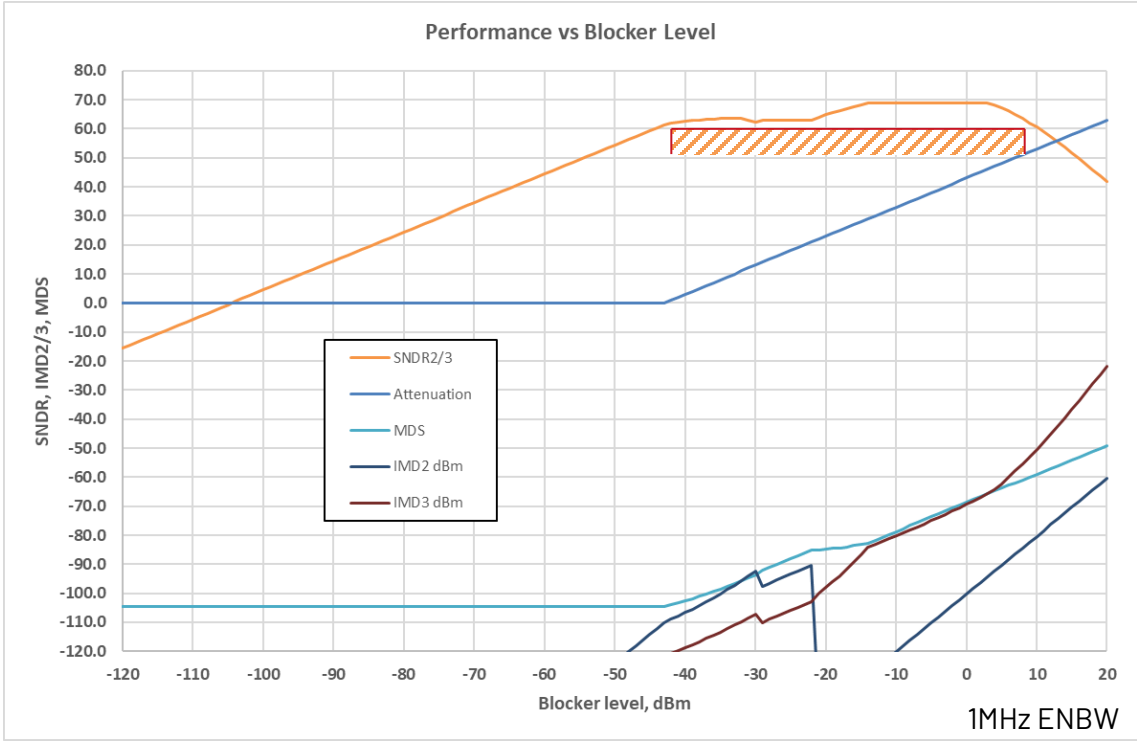


Goal: Maximize ability to **detect weak signals** while being desensitized by a large signal

Example: 0.1-20 GHz Signal Chain SNDR Performance

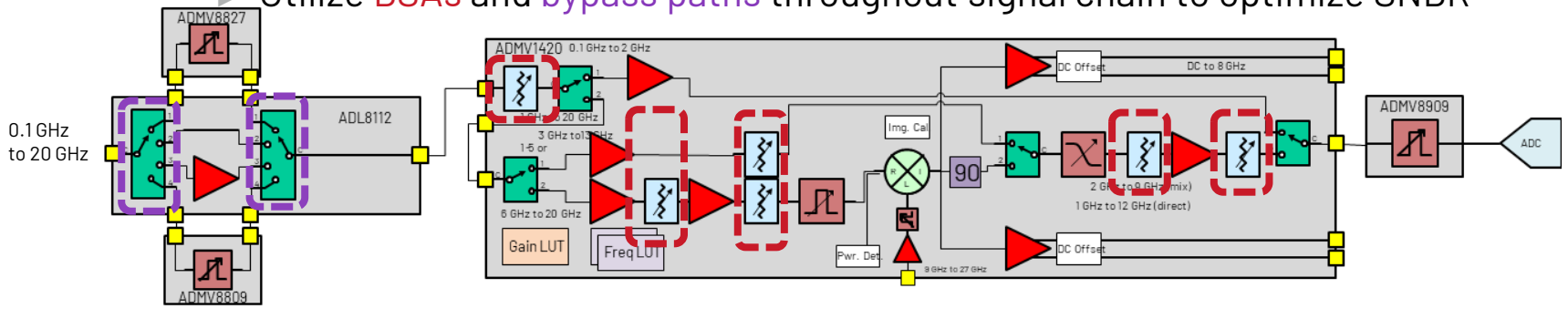


AGC



1MHz ENBW

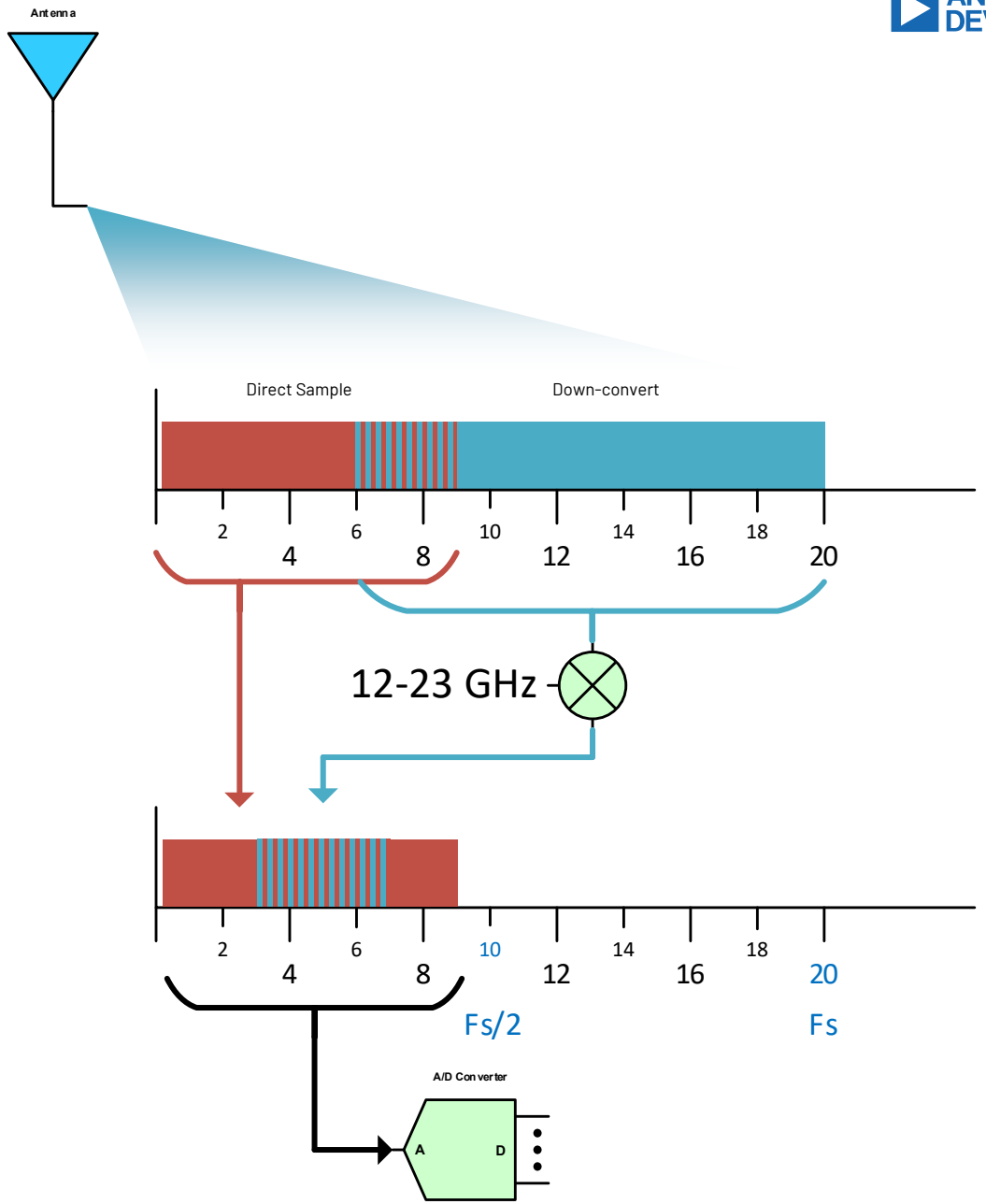
- Utilize DSAs and bypass paths throughout signal chain to optimize SNDR



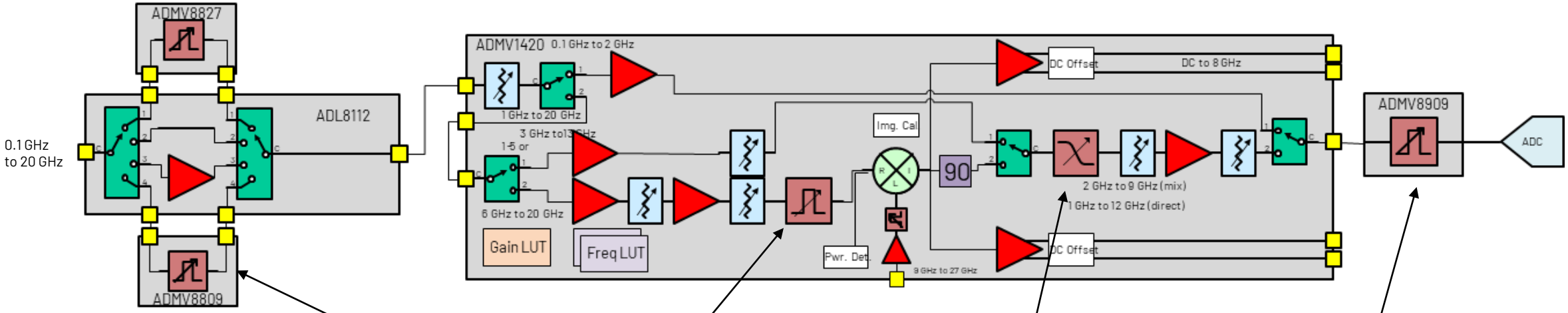
https://www.analog.com/en/analog-dialogue/articles/sfdr-considerations-in-multi-octave-wideband-digital-receivers.html

Frequency Plan, 0.1-20 GHz band

- AD9084 Fs = 20GSPS
  - Nyquist at 10GHz
- Direct sample up to ~9 GHz
- Down-convert higher frequencies to 1st Nyquist
- Select IF in the middle of the Nyquist
  - 3-7 GHz range
- IF placement will depend on practical filtering
- LO range falls out of IF and RF range
  - LO = IF + RF



Purpose of filtering within signal chain



- Sub-octave preselection
- Image rejection
- IF rejection

- Image rejection
- IF rejection
- MxN rejection

- Sub-octave IF preselection
- LO rejection
- Anti-alias

- Harmonic/noise rejection
- Anti-alias

Typically, the rejection requirements are tied to SFDR targets. If targeting 60+dB SFDR → need 60+dB of rejection for all above spurious mechanisms.

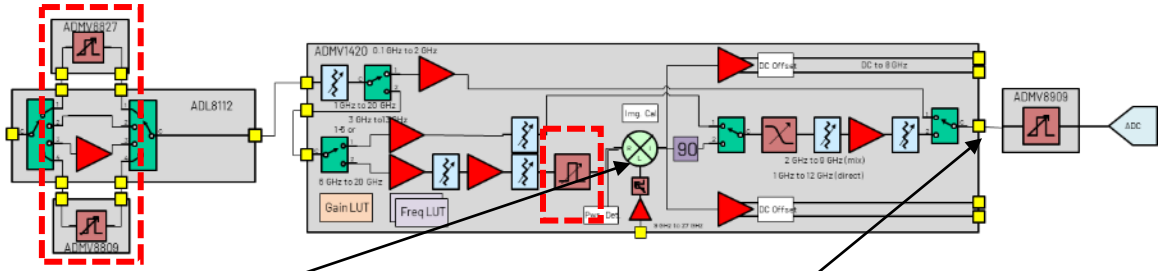
Image and IF rejection

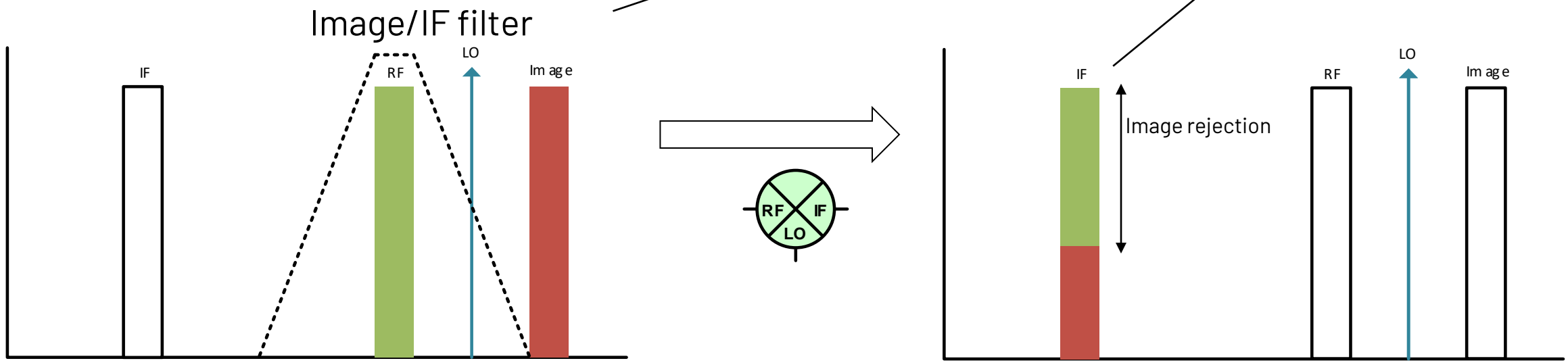
Image: Spectrum that will mix with LO to create interferer in IF

- Can be improved with filtering in front of mixer, or using "Image Reject Mixer"

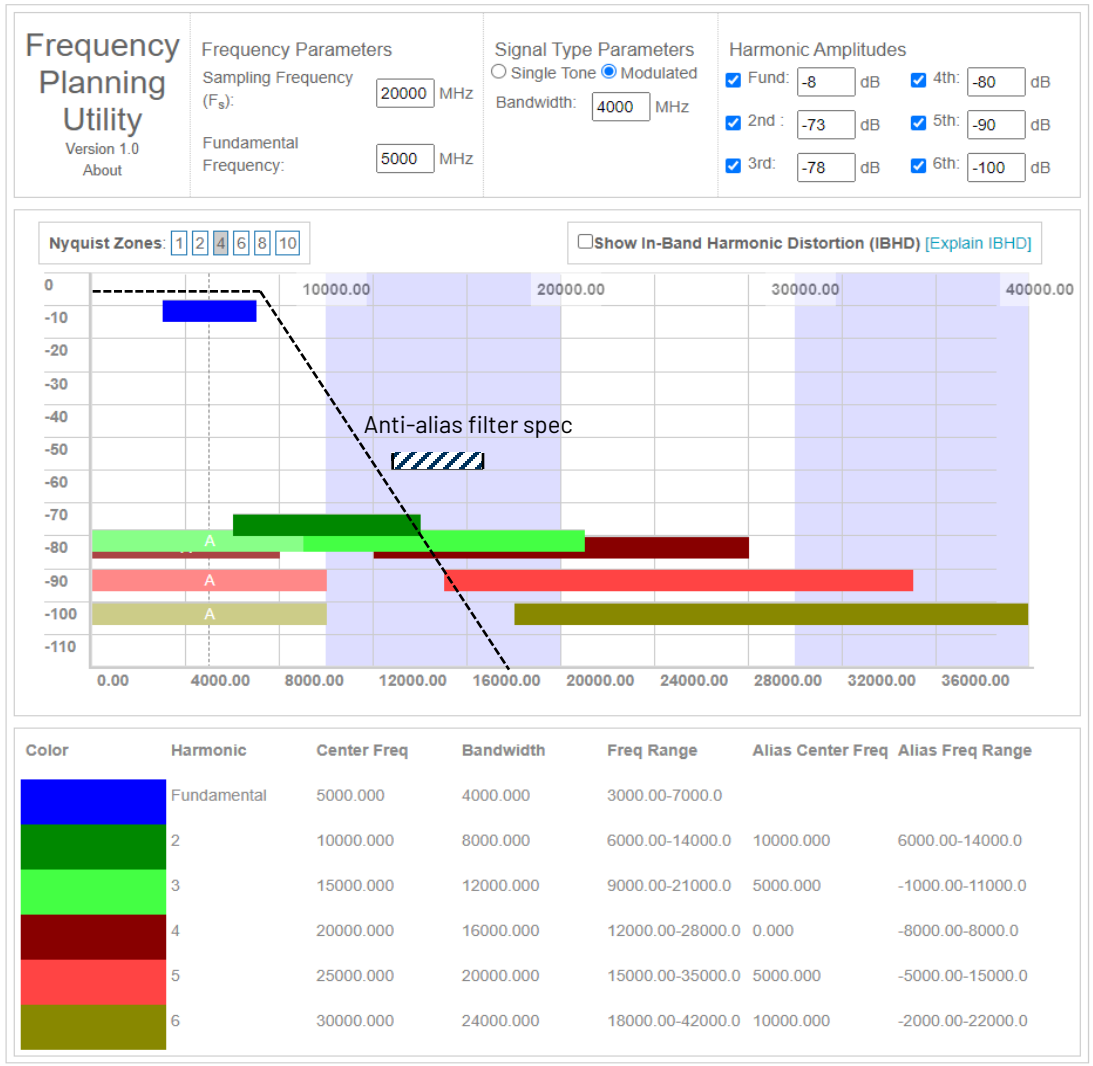
IF: leakage at IF frequency across the mixer

- Can be improved with filtering or better isolation in the mixer



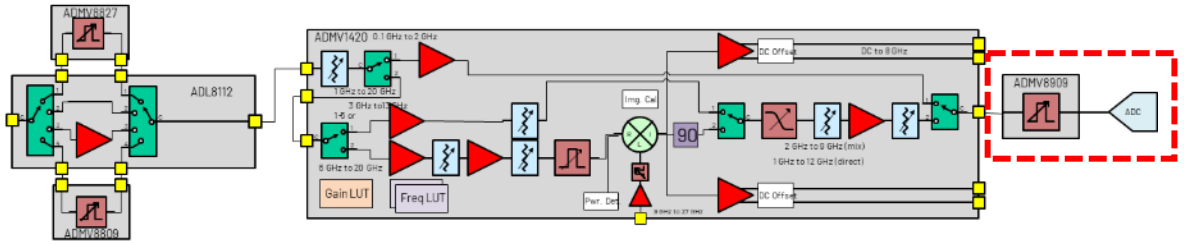


ADC Spur planning

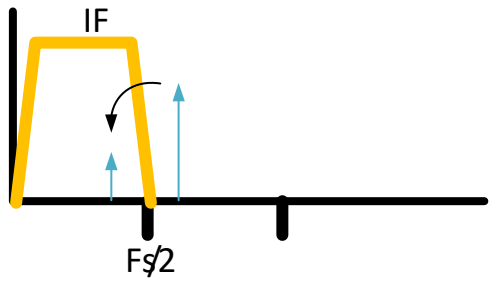


Color	Harmonic	Center Freq	Bandwidth	Freq Range	Alias Center Freq	Alias Freq Range
	Fundamental	5000.000	4000.000	3000.00-7000.0		
	2	10000.000	8000.000	6000.00-14000.0	10000.000	6000.00-14000.0
	3	15000.000	12000.000	9000.00-21000.0	5000.000	-1000.00-11000.0
	4	20000.000	16000.000	12000.00-28000.0	0.000	-8000.00-8000.0
	5	25000.000	20000.000	15000.00-35000.0	5000.000	-5000.00-15000.0
	6	30000.000	24000.000	18000.00-42000.0	10000.000	-2000.00-22000.0

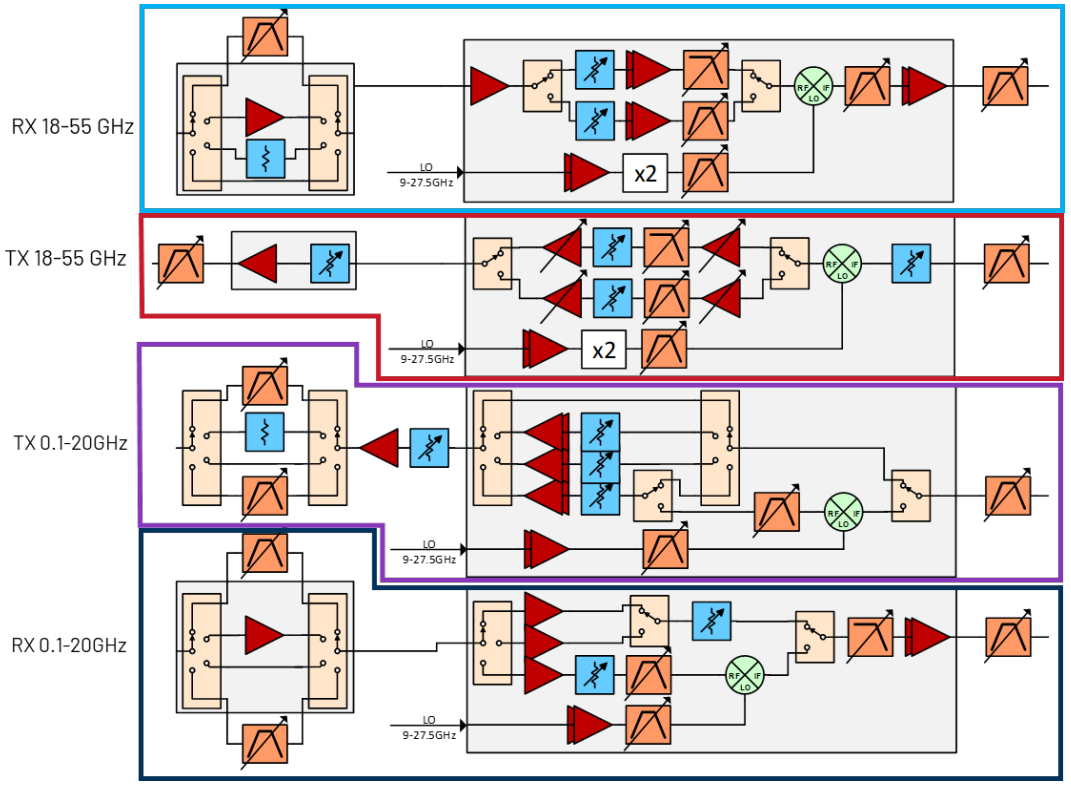
http://www.analog.com/en/design-center/interactive-design-tools/frequency-folding-tool.html



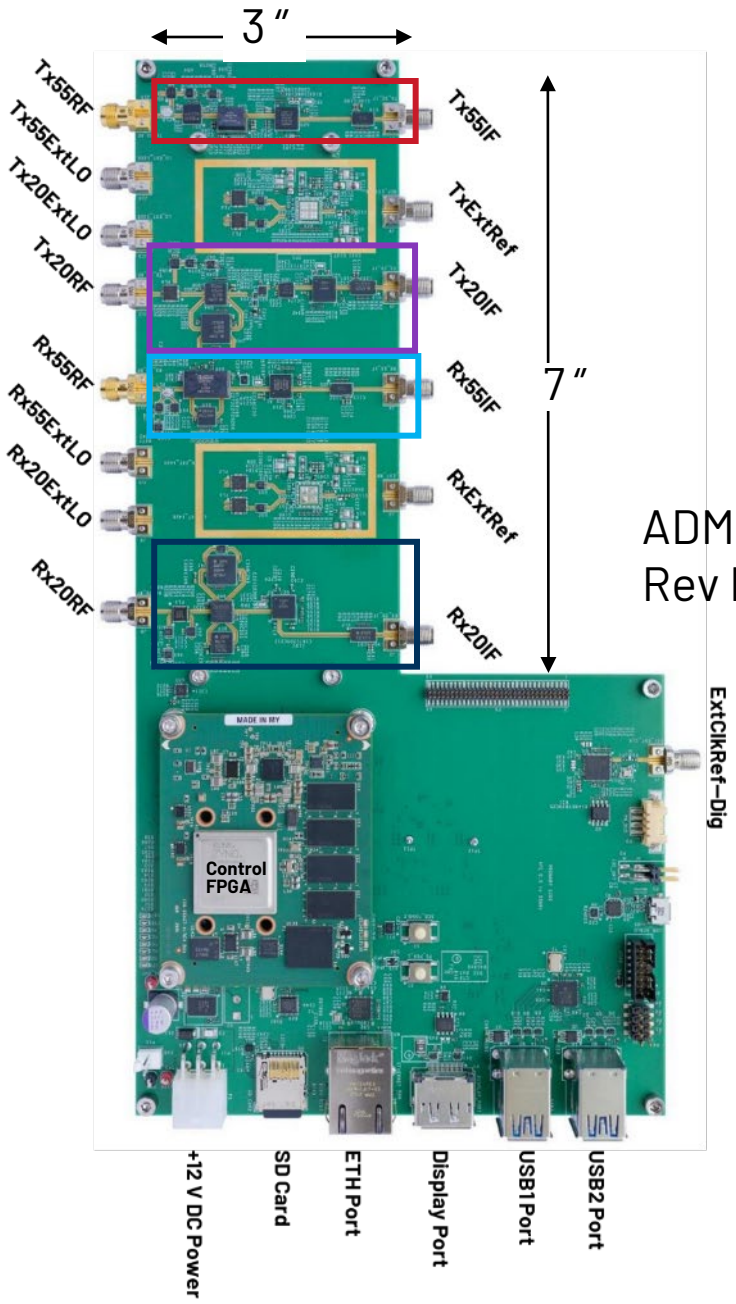
- IF placement at ~3-7 GHz
- Anti-Alias requirement:
  - 60dB rejection in 2nd Nyquist where interferer would fold in band
- Tunable IF filter allows for IF and Sample Rate adjustment



Signal Chain Evaluation Board (ADMV6010-EK1)



- 4 signal chains (0.1-20 GHz RX/TX and 18-55 GHz RX/TX)
- Access to both baseband I/Q (concept stage) and IF I/Os
  - Edge launch for IF and vertical launch for I/Q
- Power tree and digital drivers
- SystemVue model and full customer user guide
- Integrated AMD Kria™ K26 FPGA SOM for control/config
- Python control scripts for user control

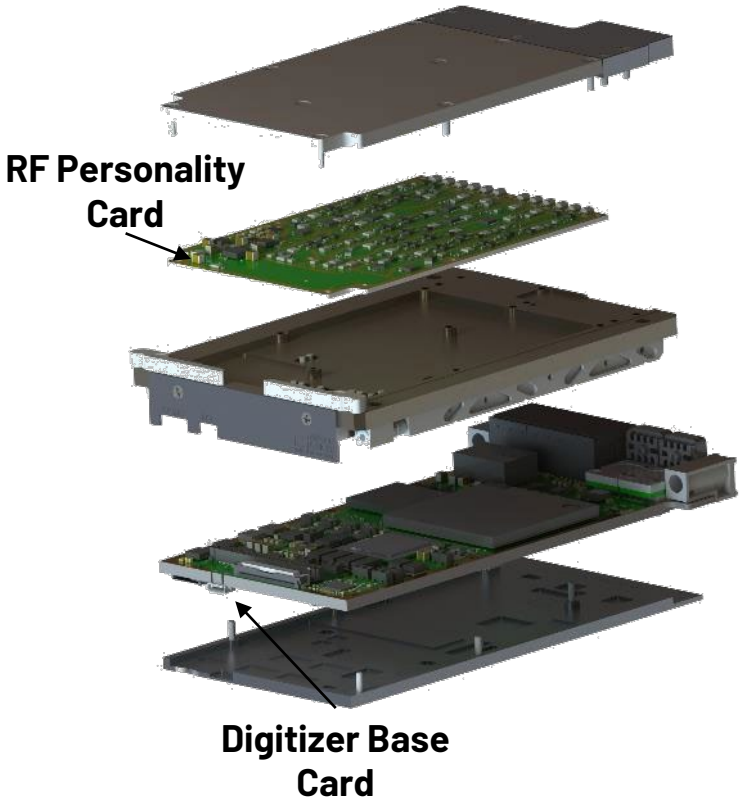


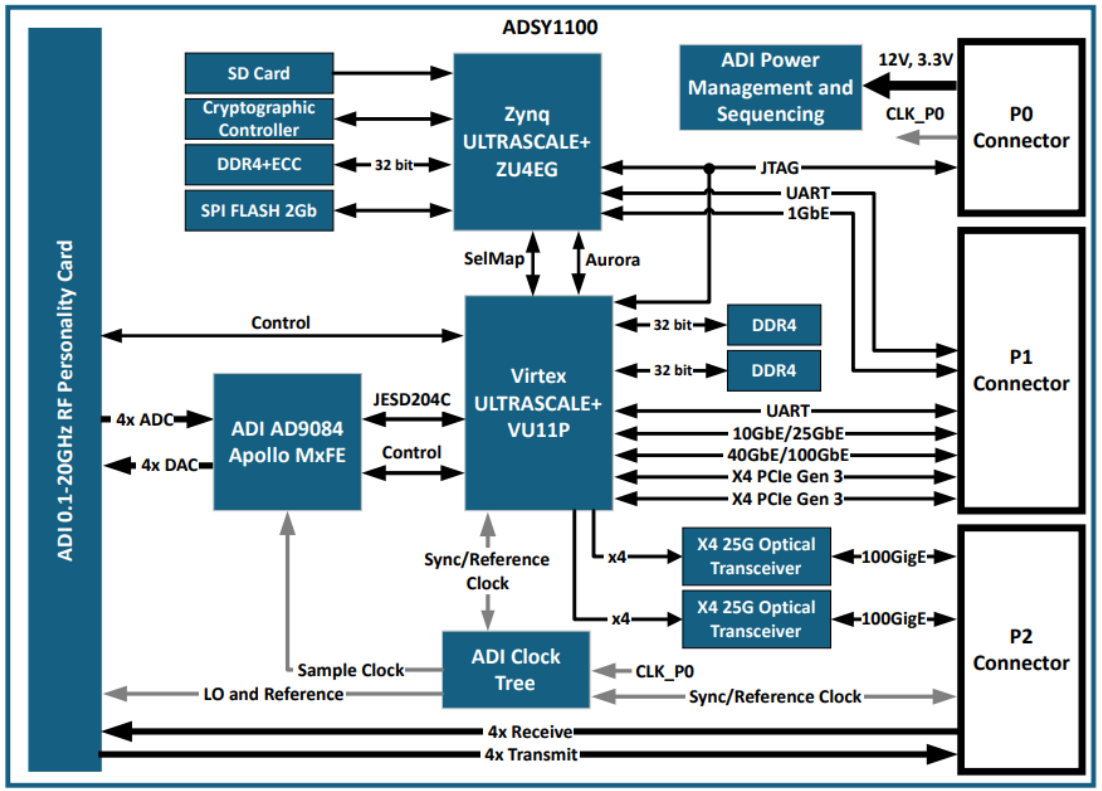
ADMV6010-EK1
Rev B Board

ADSY1100: 4T/4R, 0.1-20GHz, 1" Pitch 3UVPX SOM

Key Digitizer Base Card Features

- 4x 20GSPS ADCs
- 4x 28GSPS DACs
- Hardened DSP FFT Sniffer
- Fast-Frequency Hopping
- AD9084 Low-Latency Loopback





ADSY1100-1C3A (RF Personality card shown)

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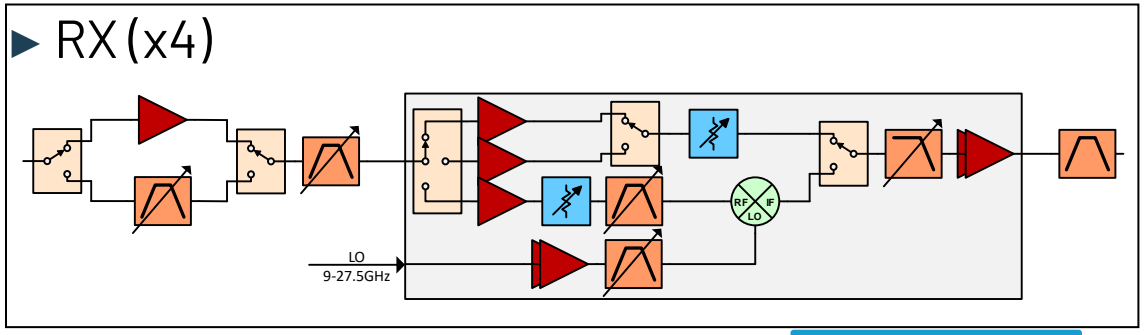
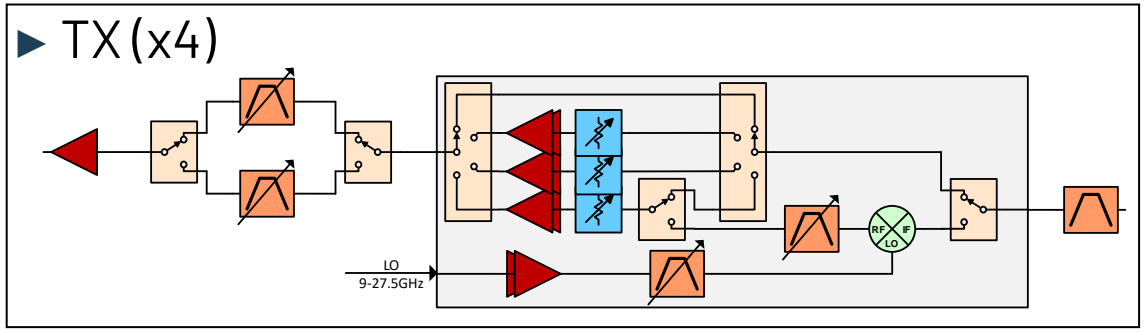




RX0-RX4

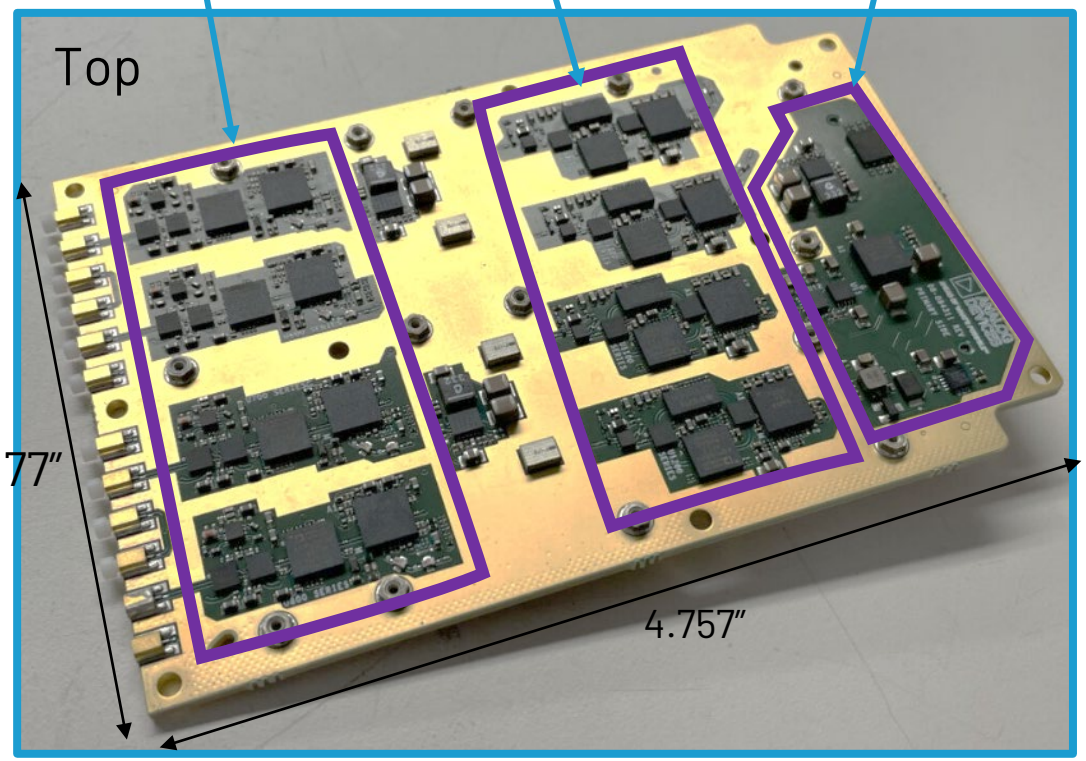
TX0-TX4

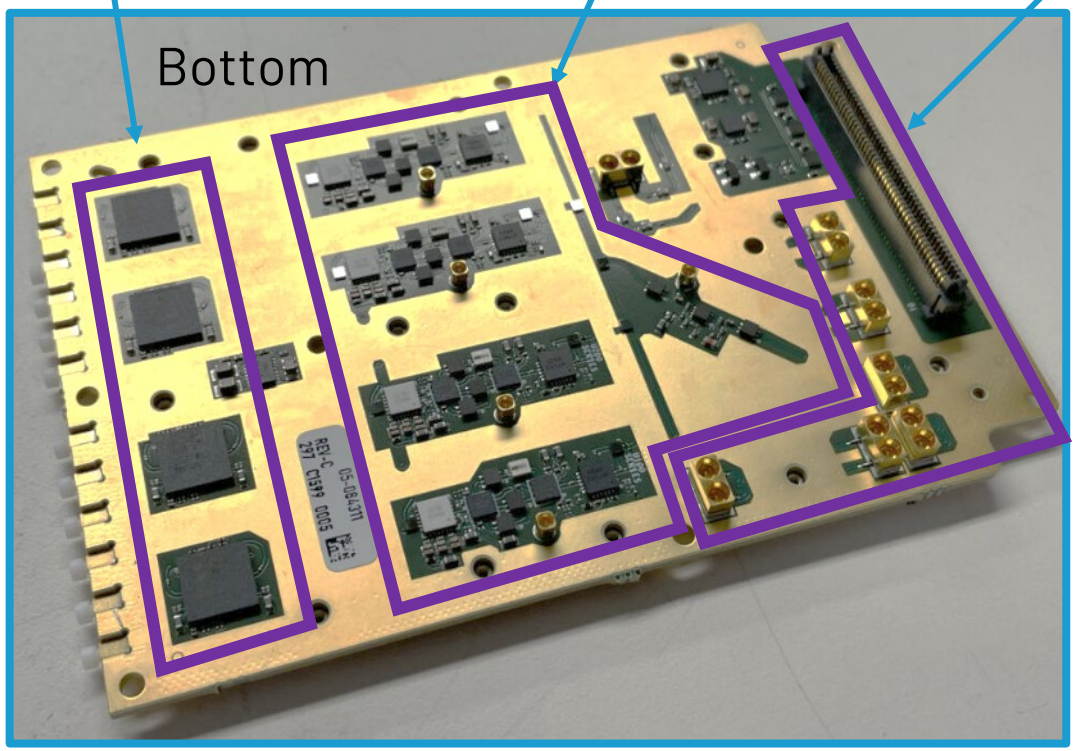
EEPROM + DC Power Tree

RX Tunable BPFs

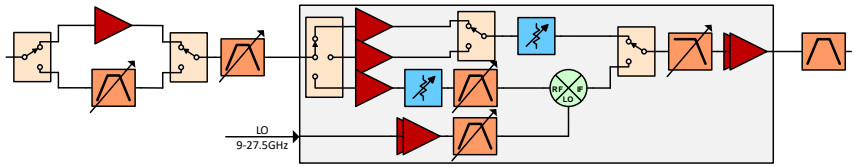
4X Selectable LOs

Mezzanine / RF to ADSY1100

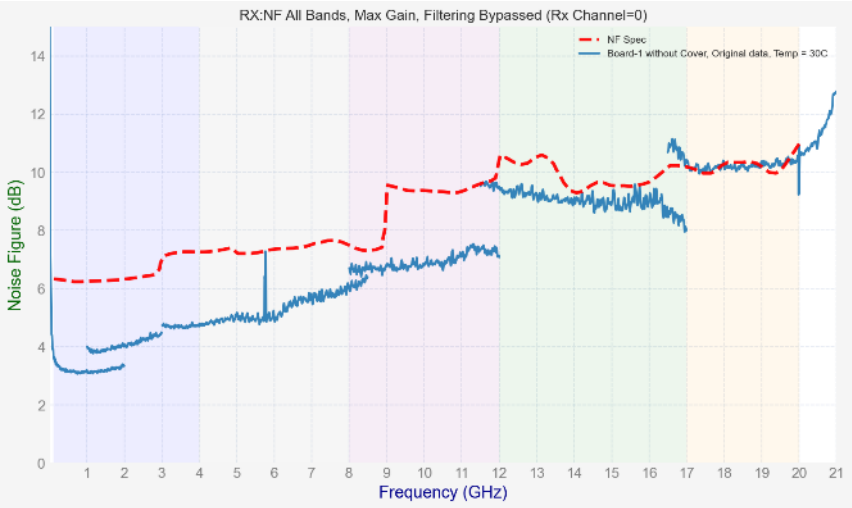




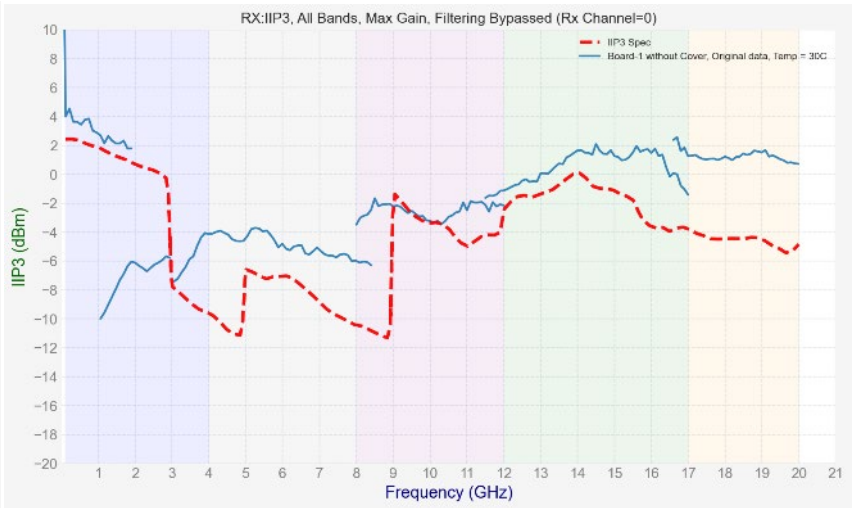
Rx Measured Performance (First pass)



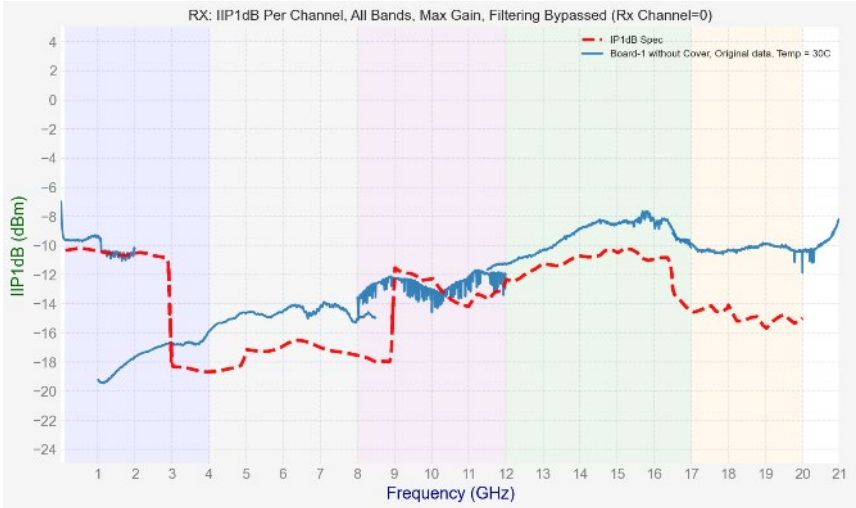
Rx NF



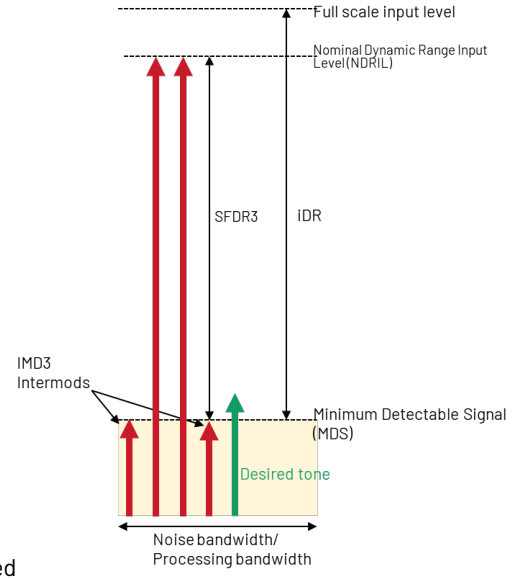
Rx IIP3



Rx IP1dB



	NF	IP3	SFDR3*	NDRIL*
2 GHz	4 dB	2 dBm	68 dB	-32 dBm
10 GHz	7 dB	-2 dBm	63 dB	-34 dBm
18 GHz	10 dB	1 dBm	63 dB	-31 dBm



SFDR3 = 2/3(IIP3-MDS); MDS = -174+NF+10*LOG(BW), 10 MHz noise bandwidth used
NDRIL = MDS+SFDR3

Gain Ranging SIPs and Amplifiers

Problem statement – Gain Ranging

Wideband mmWave systems need compact, efficient, high-dynamic range amplifiers, attenuators, and switches for gain ranging. Choosing the right semiconductor process (GaN, GaAs, SOI) and integrating it with advanced packaging solutions is critical to achieve the right performance/power tradeoff.

Challenges:

- Achieving high dynamic range across 0.1-55 GHz
- Reducing footprint and parasitics through integrated SiP solutions
- Enable fast, stable gain control for AGC and multi-mode operation

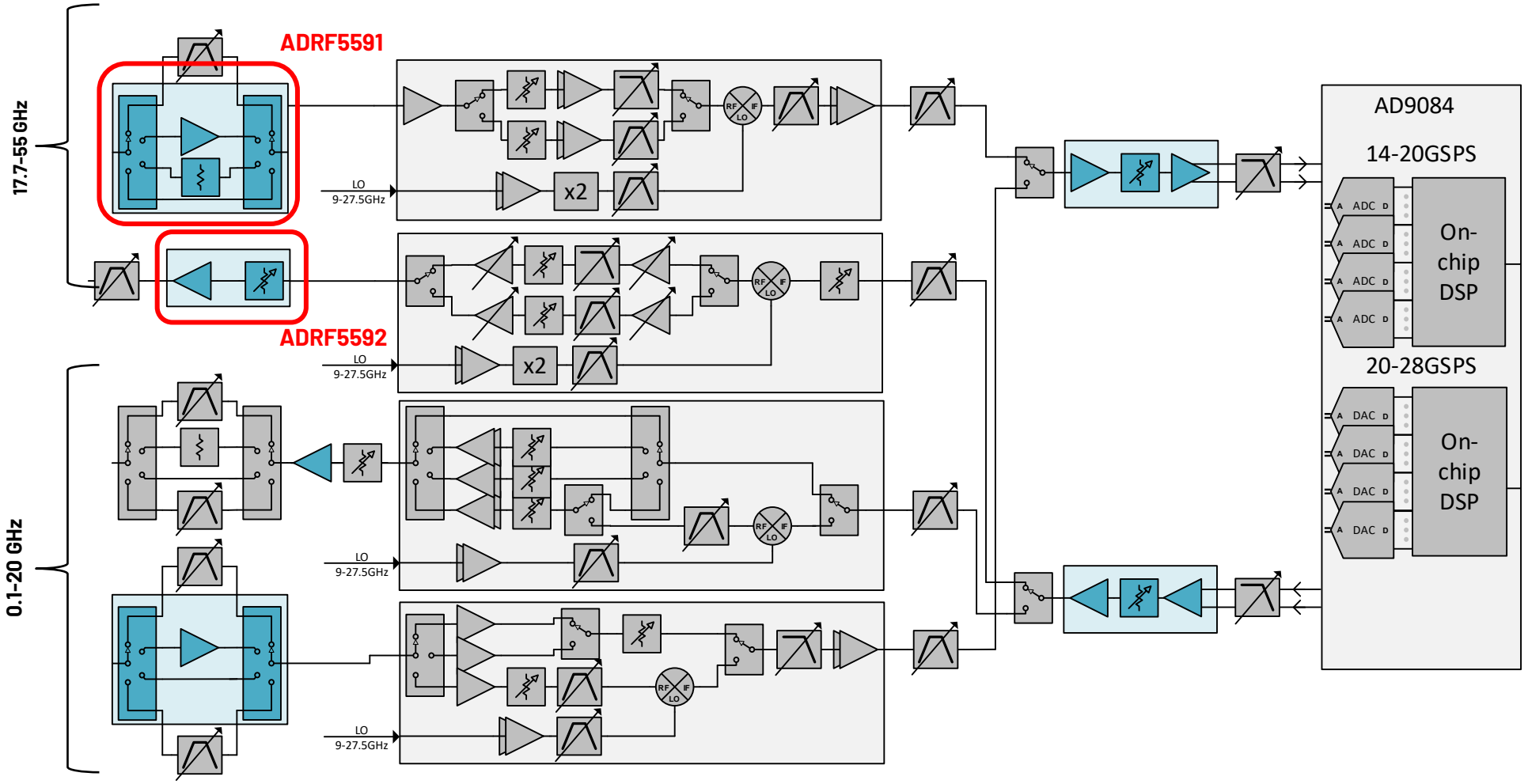
RF Front-End Solution for Apollo MxFE

Target Applications:

- Electronic Warfare
- Phased Array Antenna
- Satcom
- Multi-band Radar
- Instrumentation

RF Front-End Designs for high-speed data converters:

- 20&55GHz Tx/Rx Chains
  - Coarse Gain Ranging with Wide Dynamic Range
  - Filtering
    - Harmonic / IP2 Rejection
    - Blocker Rejection



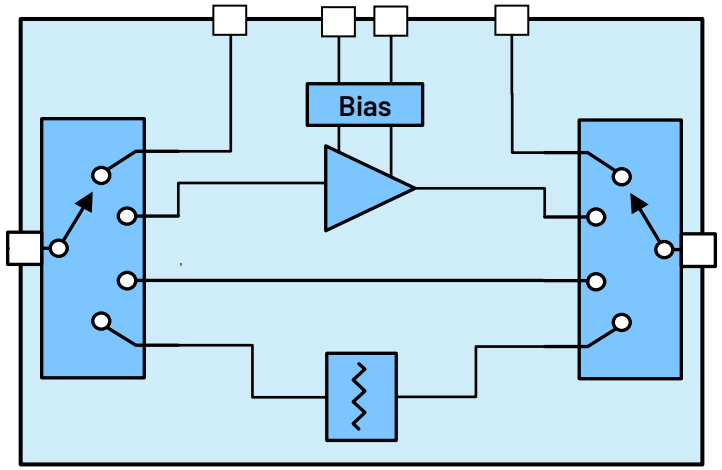
18 GHz to 55 GHz Flexible Rx/Tx Front Ends

ADRF5591

18 GHz to 55 GHz Rx Gain Ranging SiP

KEY FEATURES

- Integrated amplifier, through, attenuator paths
- External path for filter option
- No external components needed
- SOI switch, GaAs amplifier
- Optional bias controller
- 400 mW power dissipation in gain mode
- 13 mm × 7.5 mm size

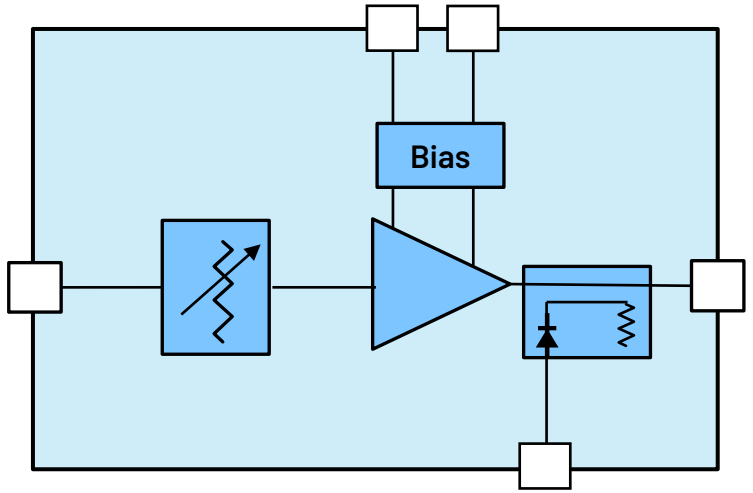


ADRF5592

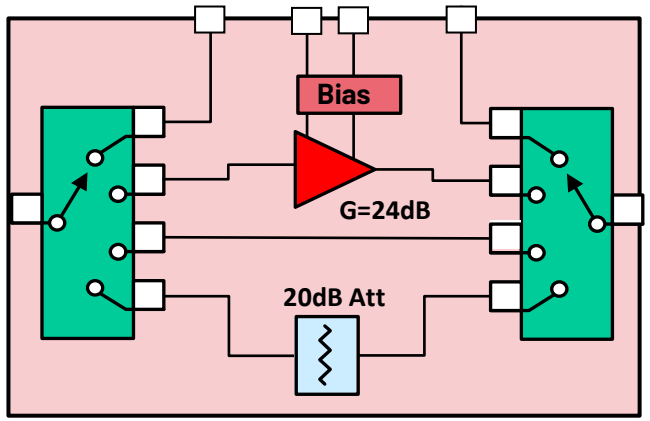
18 GHz to 55 GHz Tx Gain Ranging SiP

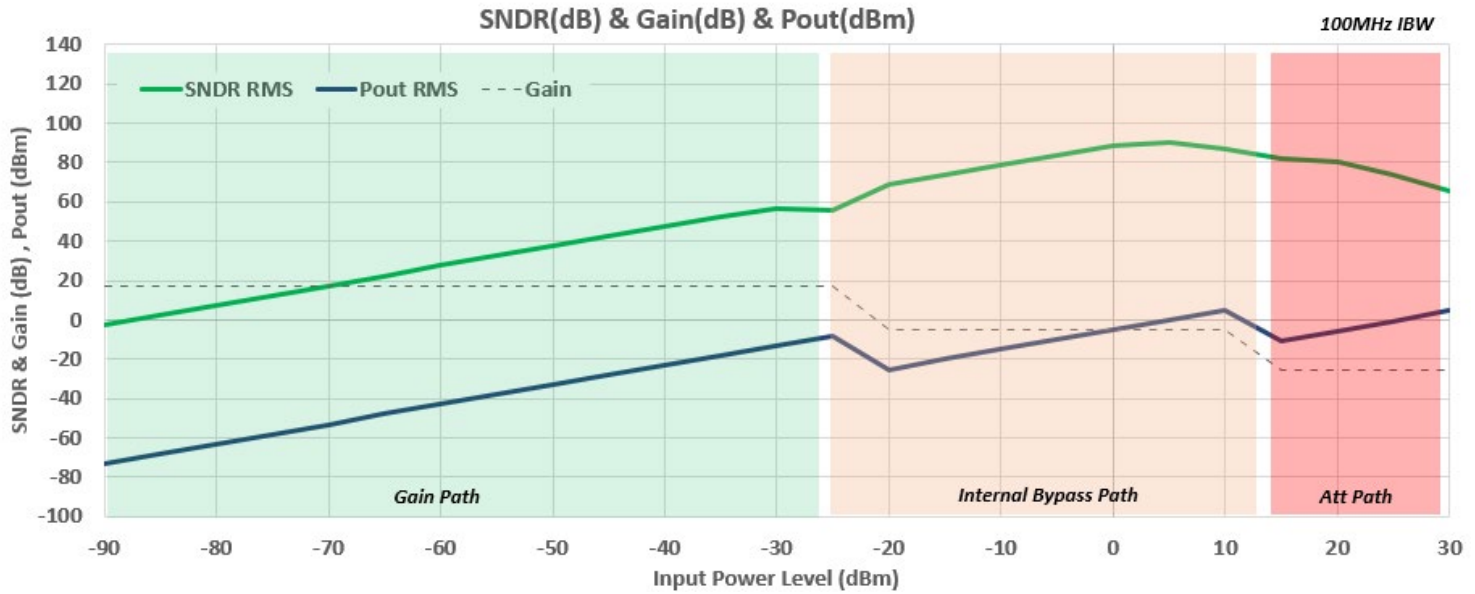
KEY FEATURES

- Broadband SOI DSA and GaAs power amplifier
- Amplifier detector output
- Optional bias controller
- High dynamic range
- Internal NVG option
- 4.2 W power dissipation
- 8 mm × 6 mm size



ADRF5591: 18-55GHz Gain Ranging SiP for RX Chains



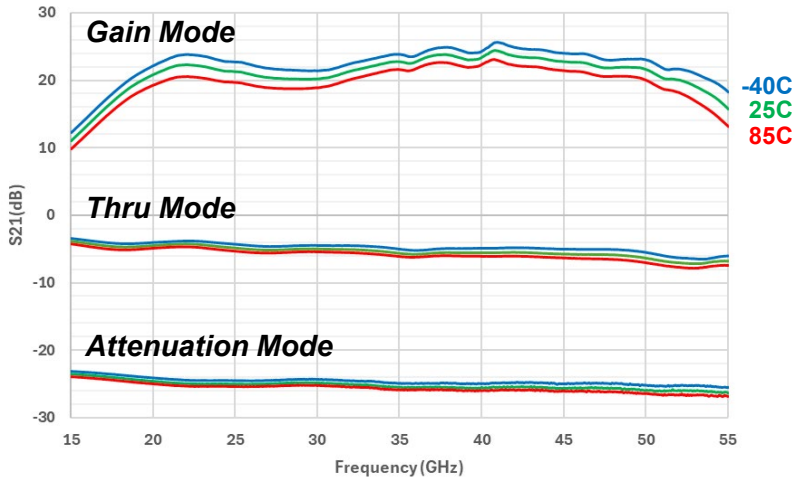


- SOI switch, GaAs amplifier
- Internal optional bias controller
- Attenuator for high dynamic range
- **No External Components**
- 400mW power dissipation in gain mode
- 13 mm x 7.5 mm size

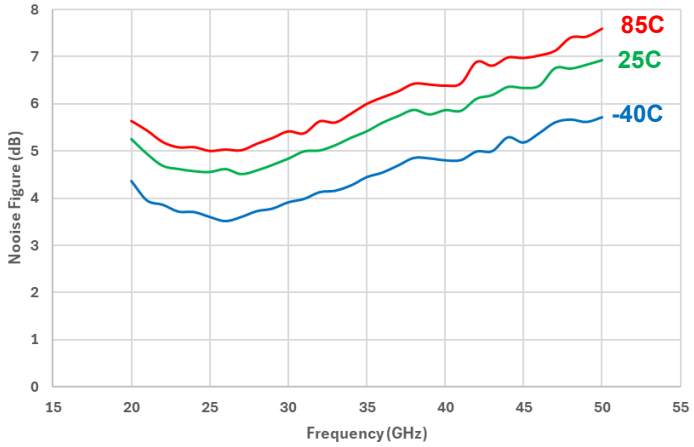
Paramater	Gain Path	Thru Path	Att. Path	Unit
Gain	20	-4	-24	dB
NF	6	4	24	dB
Input IP3	6	44	46	dBm
IP1dB / OP1dB	-2 / 17	> Pin Max	> Pin Max	dBm
Pin Max	20	24	24	dBm
Switching time	20			ns

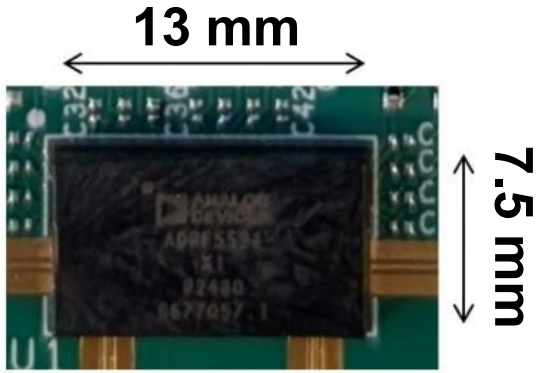
Product Highlights – ADRF5591 - 18-55GHz

Gain

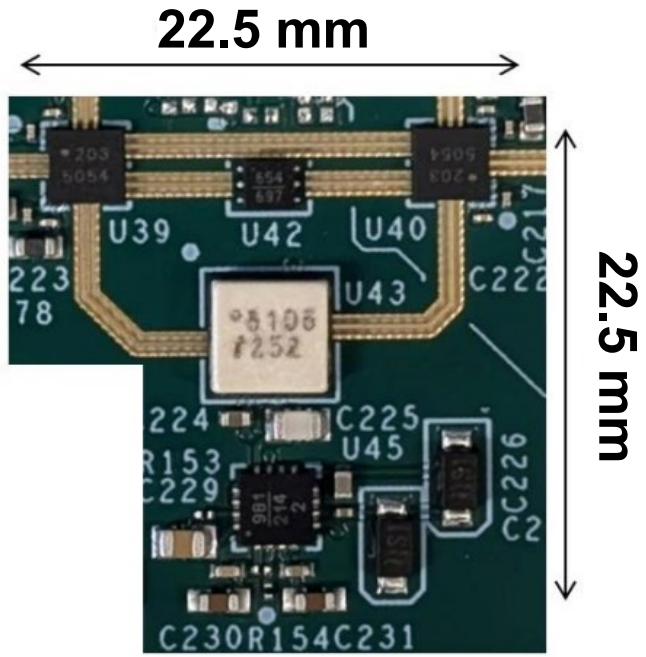


Noise Figure





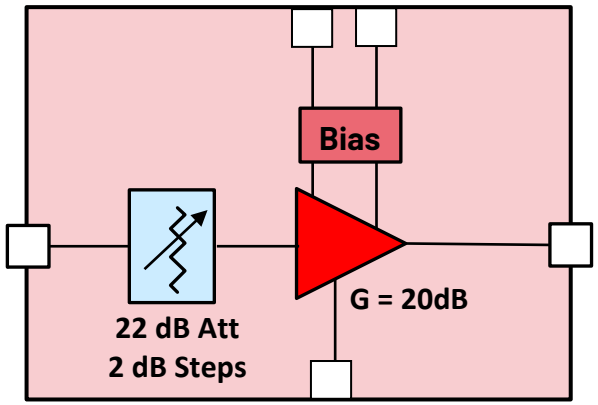
ADRF5591

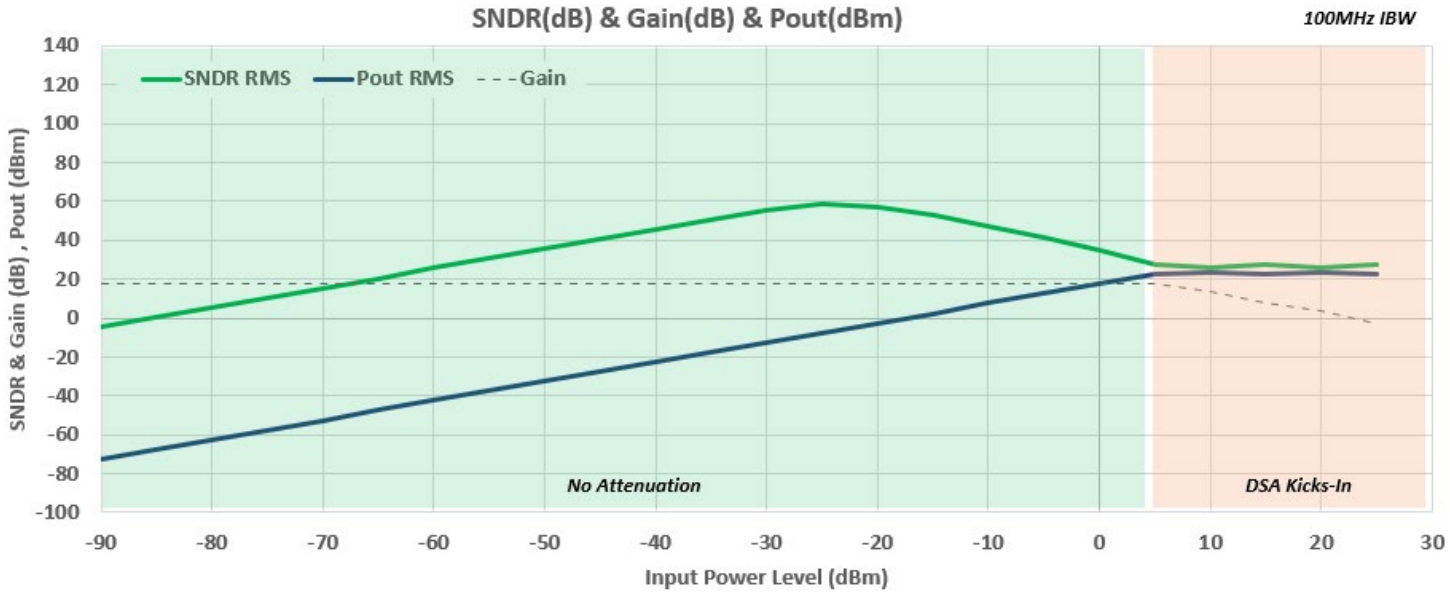


**Snippet from Missouri PCB*

>80% area savings compared to discrete solution

ADRF5592: 18-55GHz Gain Ranging SiP for TX Chains





- Broadband DSA + AMP
- Amplifier detector output
- Internal bias controller
- High Dynamic Range
- 4.2W power dissipation
- Internal NVG Option
- **8mm x 6mm size**

Parameter	Max Gain State	Min Gain State	Unit
Gain	18	-4	dB
NF	8	30	dB
Output IP3	35	35	dBm
IP1dB / OP1dB	10 / 27	> Pin Max	dBm
Pin Max	22	25	dBm
Gain Switching Time	100		ns

RF Front-End Solution for Apollo MxFE

Target Applications:

- Electronic Warfare
- Phased Array Antenna
- Satcom
- Multi-band Radar
- Instrumentation

RF Front-End Designs for high-speed data converters:

- 20&55GHz Tx/Rx Chains
  - Coarse Gain Ranging with Wide Dynamic Range
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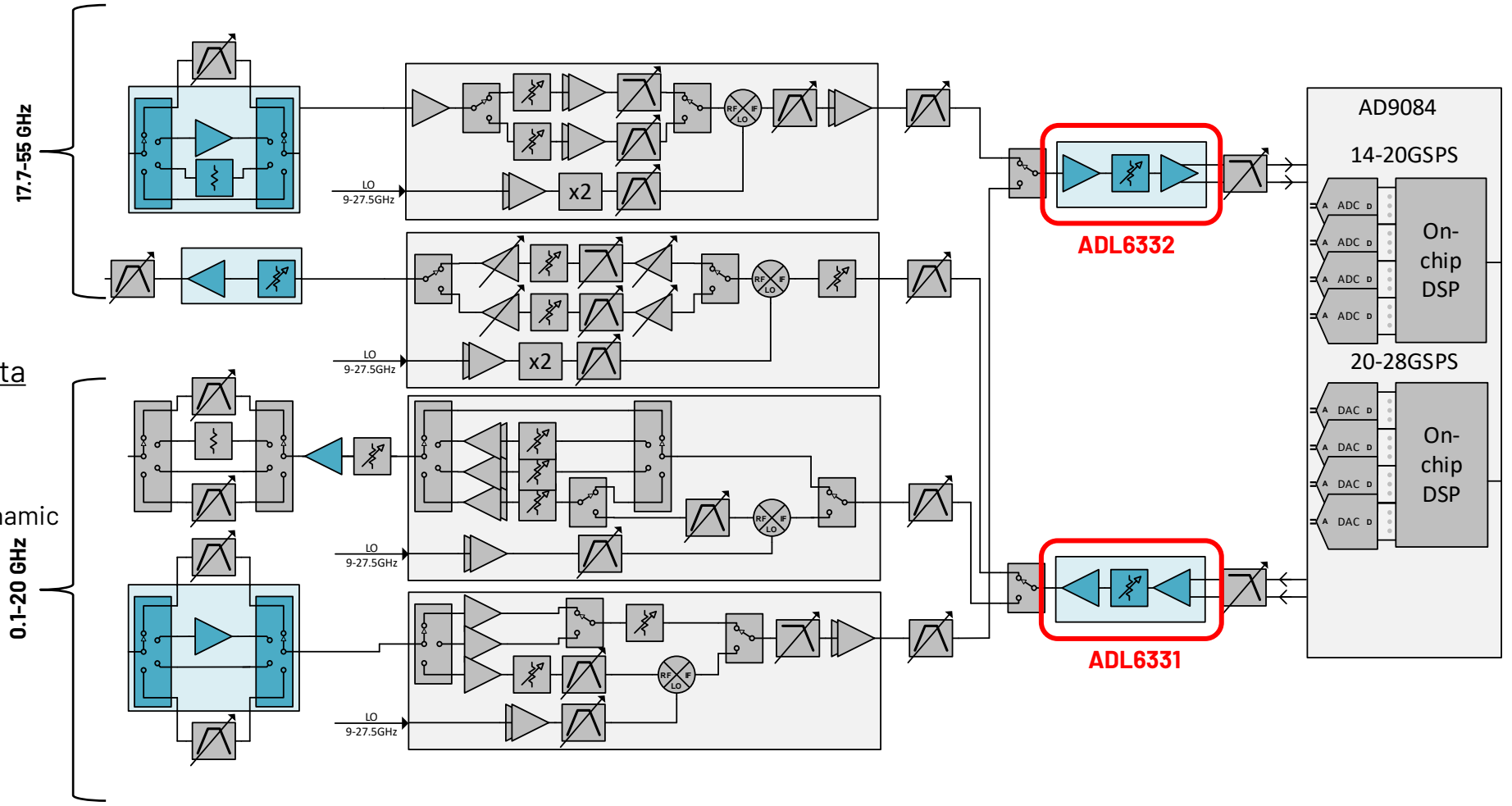
    - Blocker Rejection



TX-VGA and RX-VGA

TX-VGA for interfacing to the Apollo MxFE DAC

- ADL6331A: 380MHz to 8GHz
- ADL6331B: 1GHz to 15GHz

RX-VGA for interfacing to the Apollo MxFE ADC

- ADL6332A: 380MHz to 8GHz
- ADL6332B: 1GHz to 15GHz

Single 3.3 V supply

24-terminal, 4.0 mm x 4.0 mm LGA

Fully programmable through a 3-wire/4-wire SPI

APPLICATIONS

- Aerospace and defense
- Instrumentation and test equipment
- Communication systems

ADL6332: RX-VGA

Broadband RxVGA interfacing LNA and beamformer to RF-ADC

Operating frequency range

- ADL6332-A: 0.38 GHz to 8.0 GHz
- ADL6332-B: 1.0 GHz to 15.0 GHz

50 Ω single-ended input and 50 Ω differential output

RF DSA range: 24.0 dB with 1.0 dB step

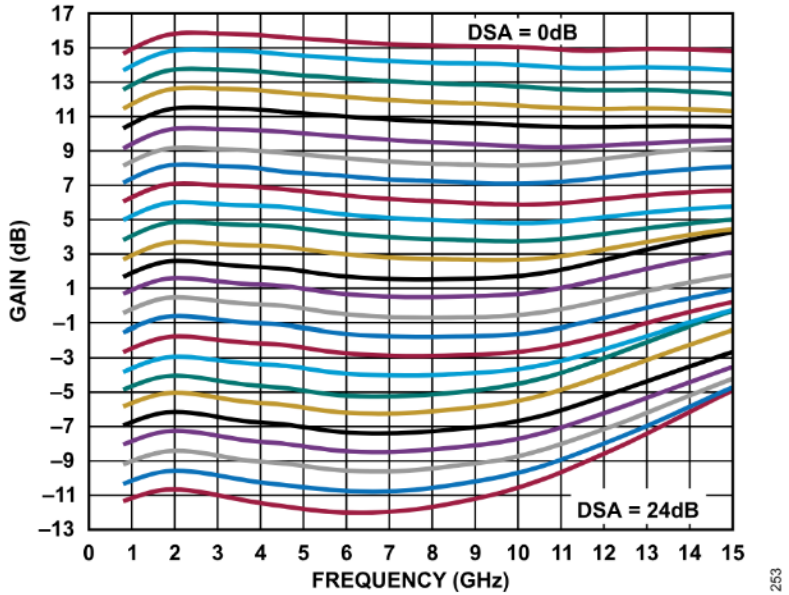
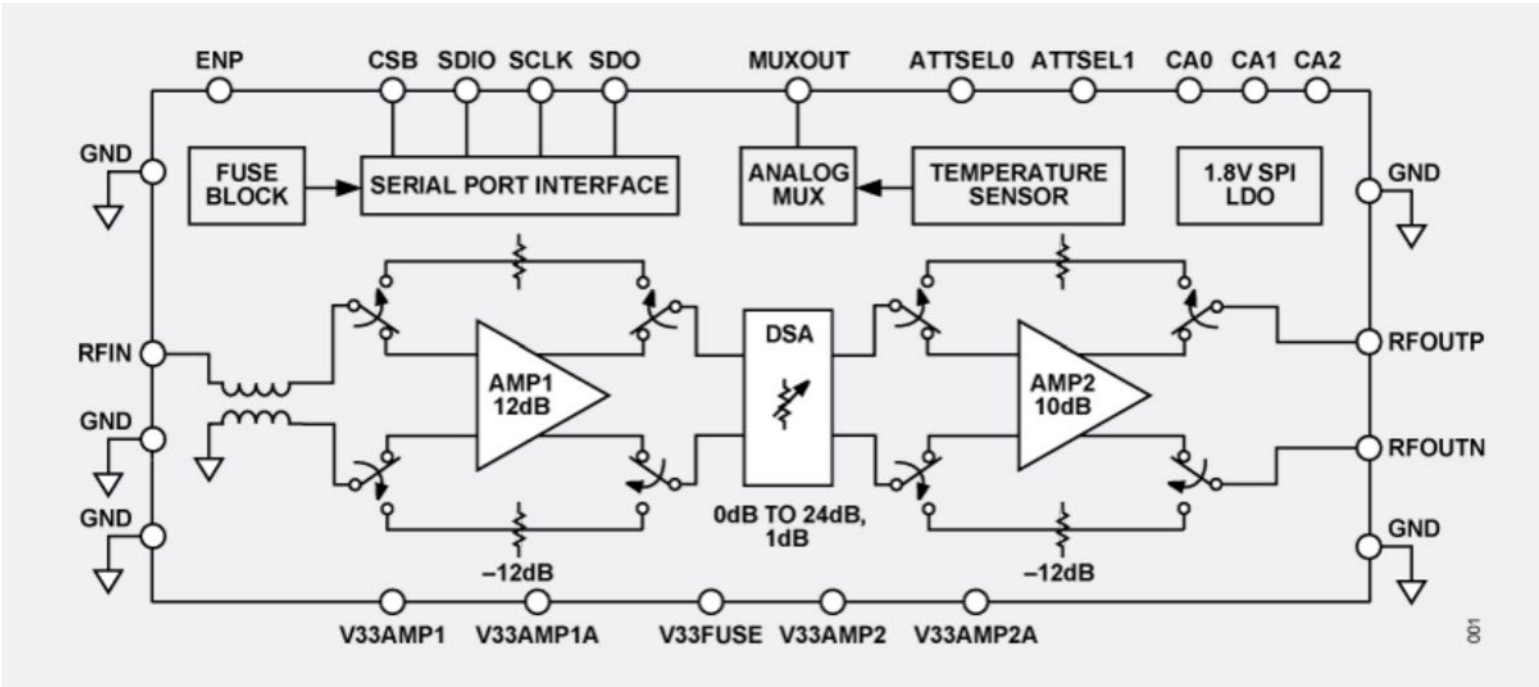


Figure 53. Gain vs. Frequency, 1.0 dB DSA Steps



ADL6332: RX-VGA

ADL6331 and ADL6332 have similar performance

The difference is the location of the RF balun being located to the input for the RX-VGA ADL6332

Plots from ADL6332-B

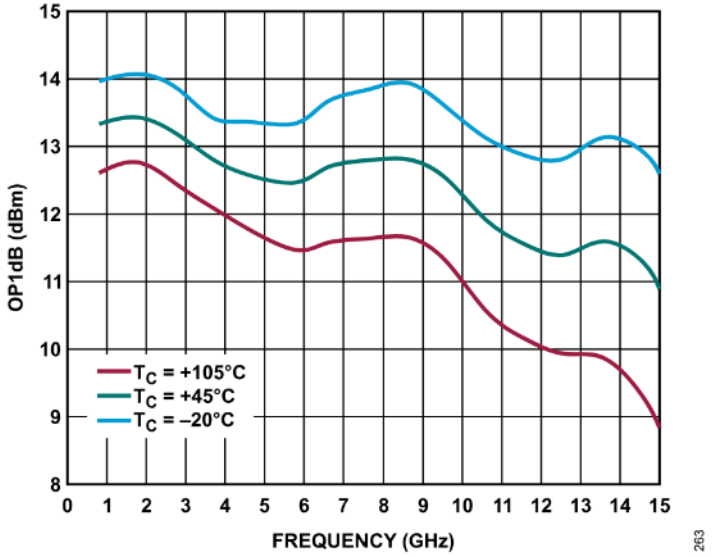


Figure 63. OP1dB vs. Frequency for Various Temperatures

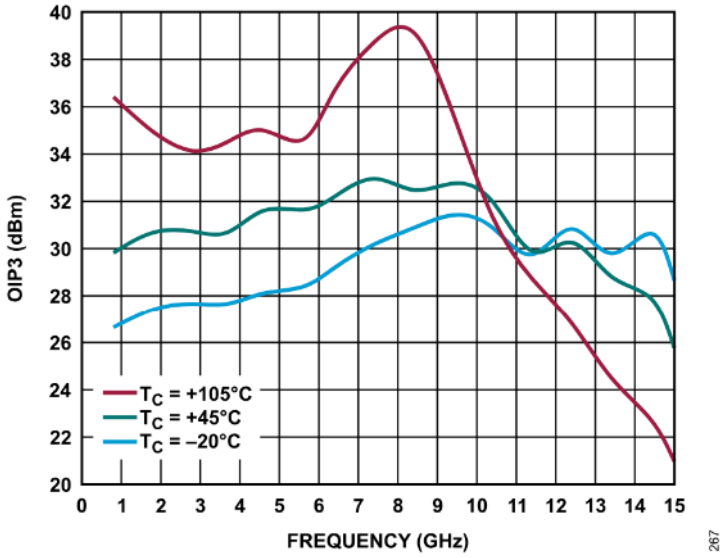


Figure 67. OIP3 vs. Frequency for Various Temperatures

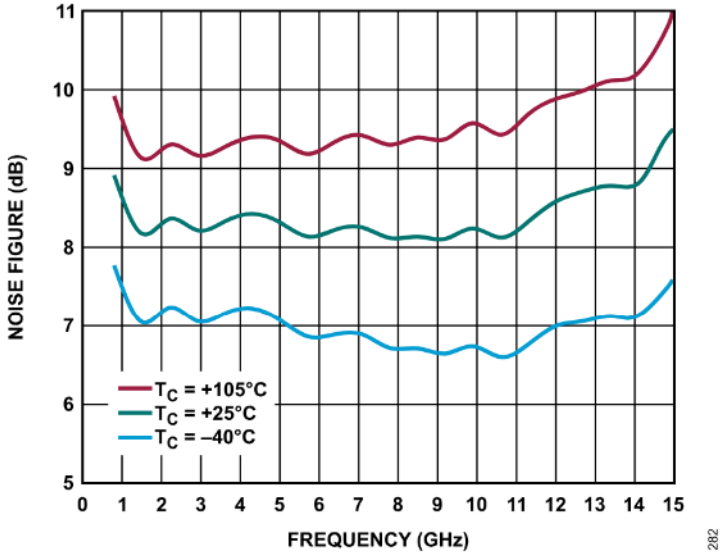


Figure 82. Noise Figure vs. Frequency for Various Temperatures

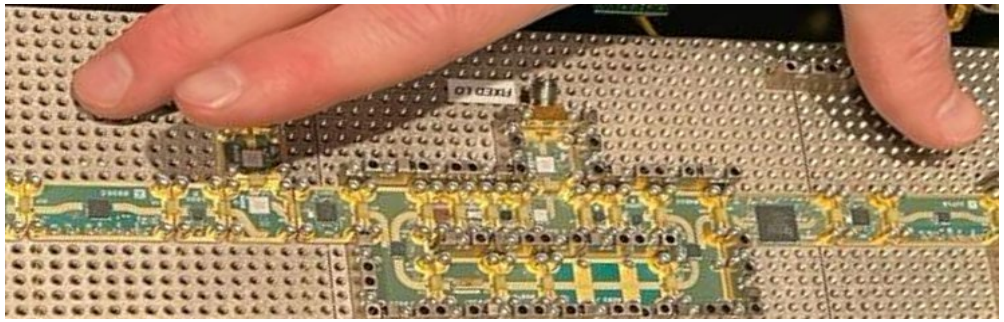
Up/Down conversion and LO generation

Problem statement – Up/down conversion

Wideband UDC chains must cover 0.1-55 GHz with high spur rejection and rapid frequency agility while remaining compact.

Challenges:

- Maintaining NF, linearity, and gain flatness across extremely wide RF bands
- Discrete signal chains can achieve performance but take up too much space
- Control networks for RF components can take up significant pin count on FPGAs

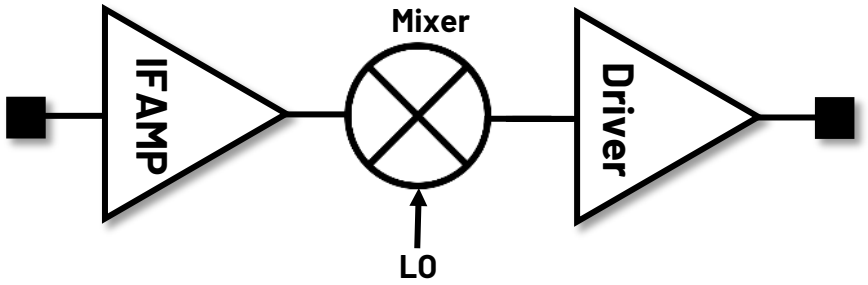


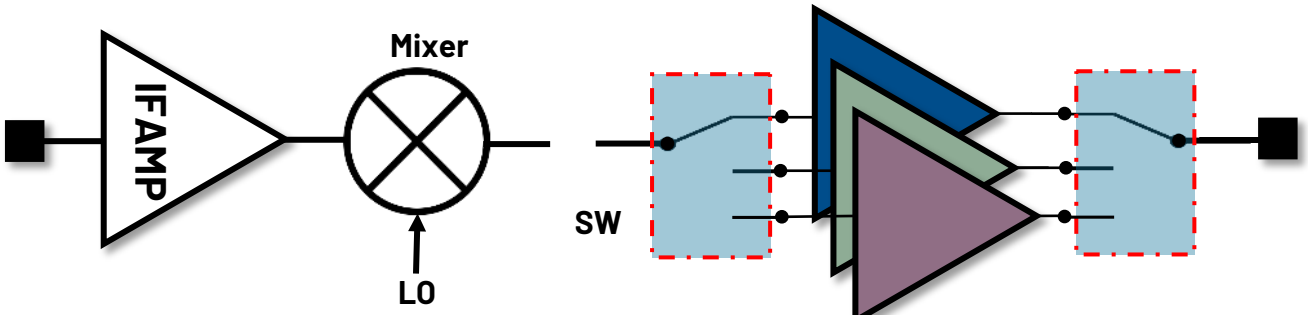
Legacy discrete solution

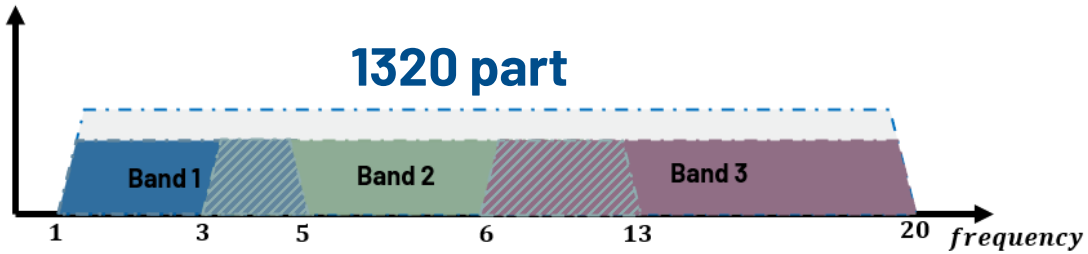
A "to scale" image showing the level of integration

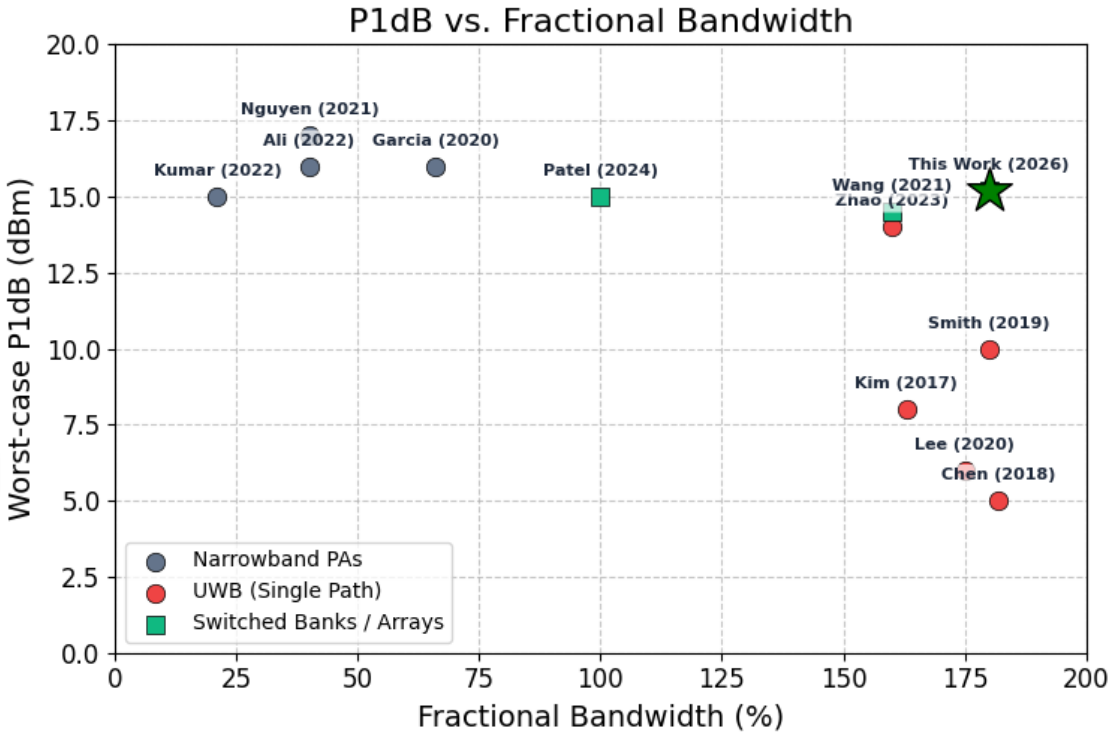
ADMV1455

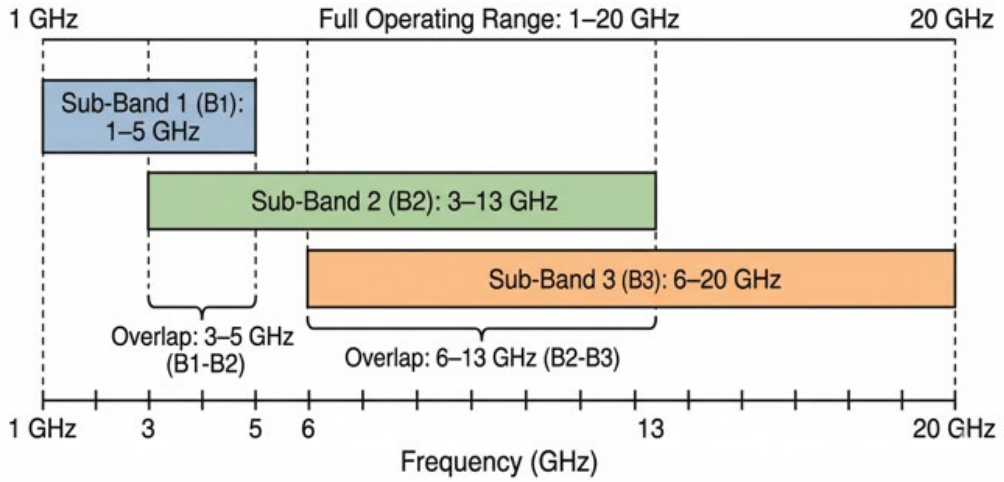
The Up Converter Architecture Selection



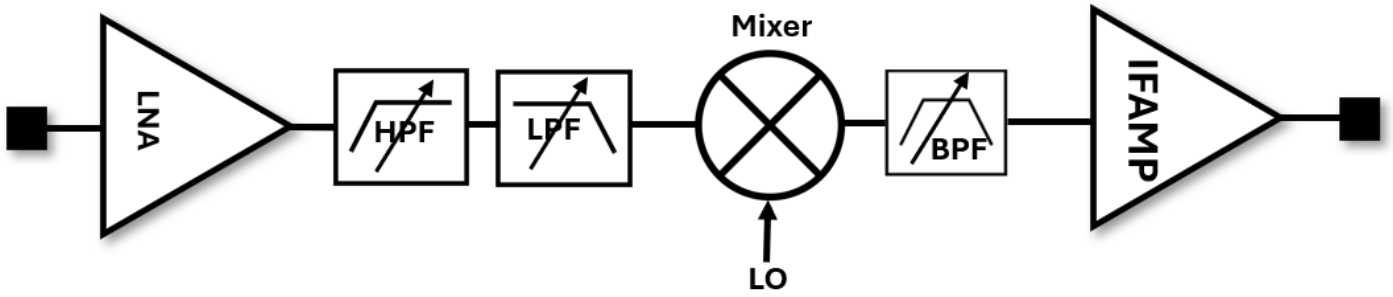


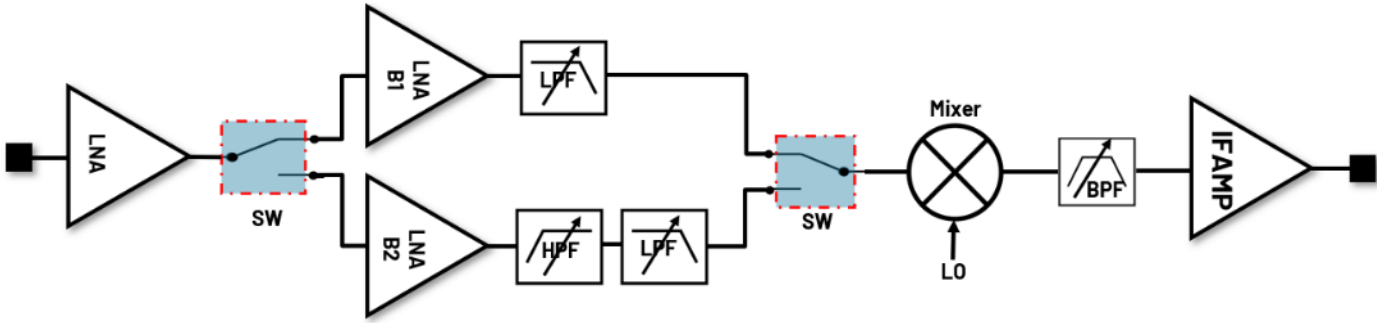


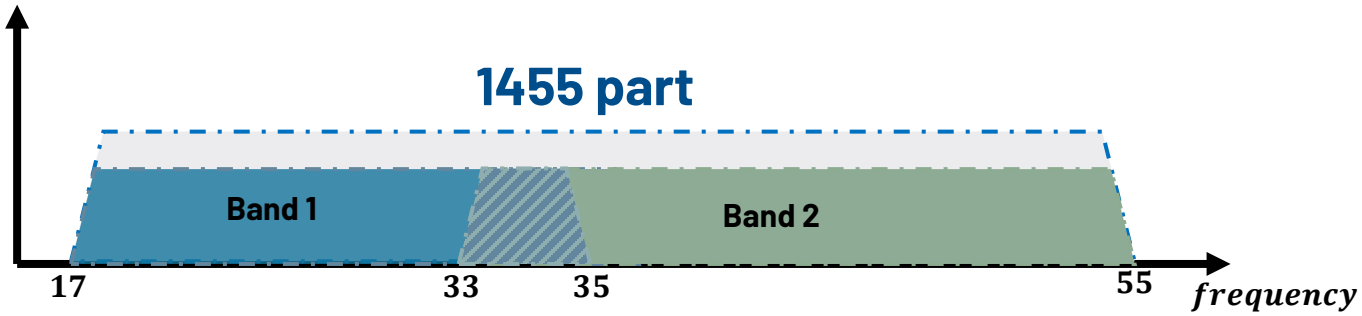


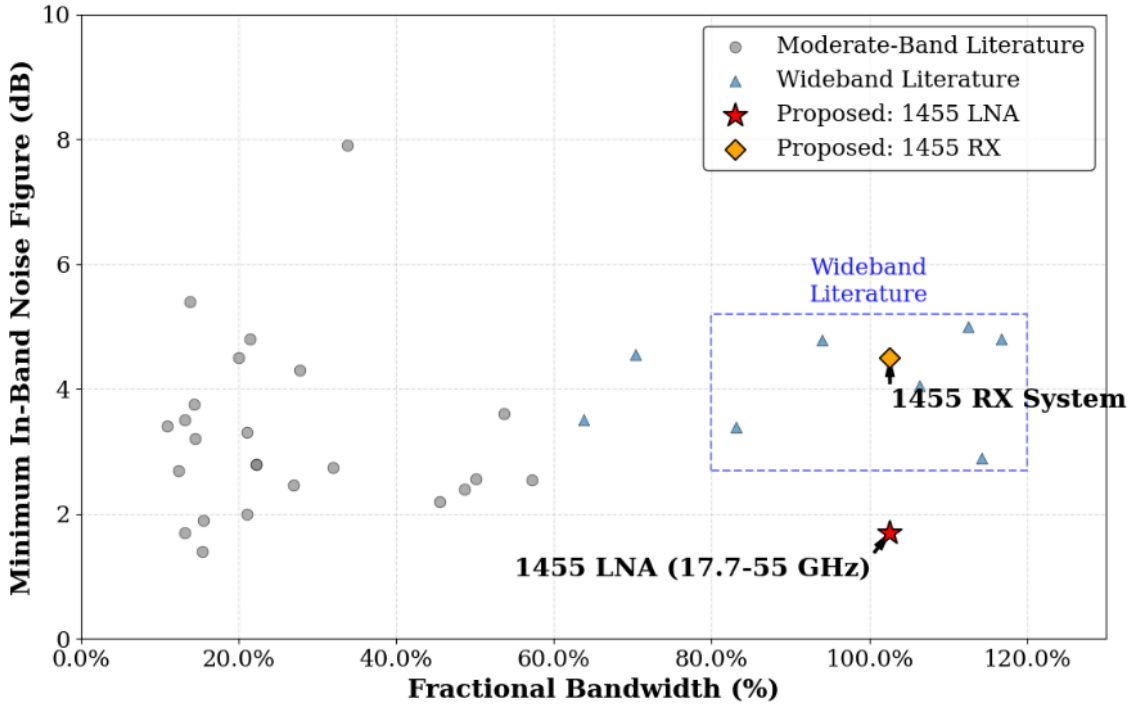


The Down Converter Architecture Selection



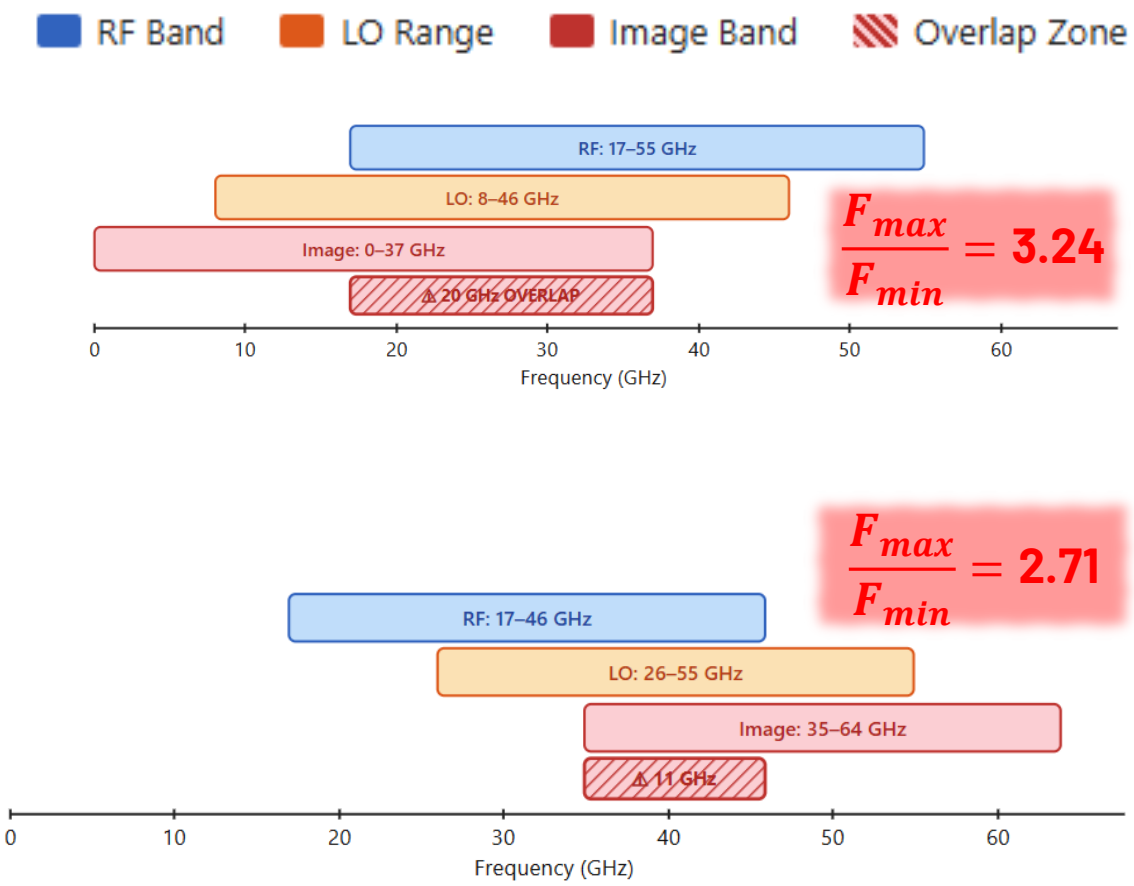






The Down Converter Passband Tuning Ratio Comparison

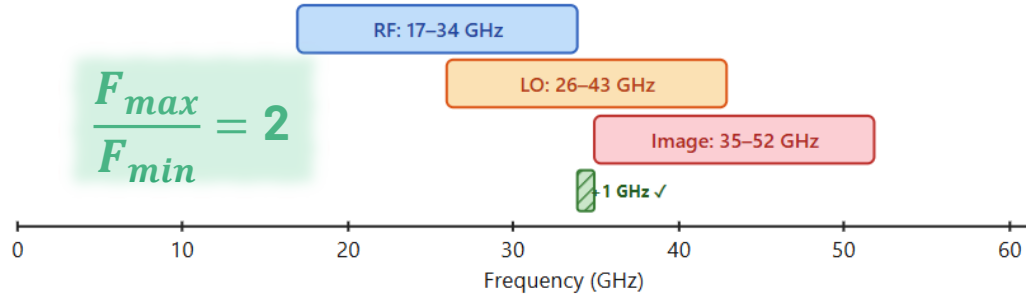
Wideband approach



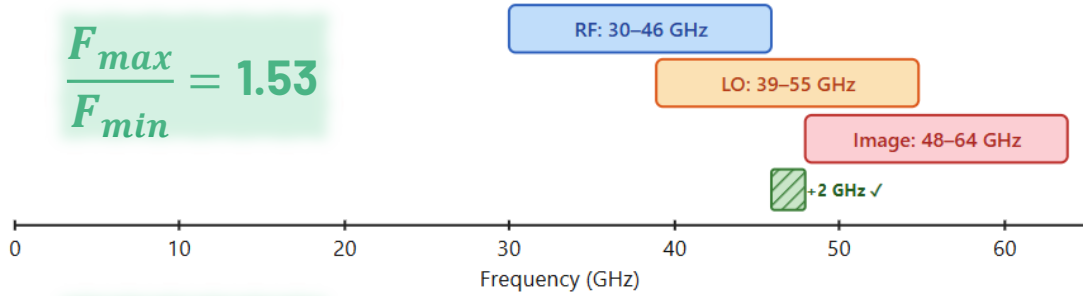
$$\frac{F_{max}}{F_{min}} = 3.24$$

$$\frac{F_{max}}{F_{min}} = 2.71$$

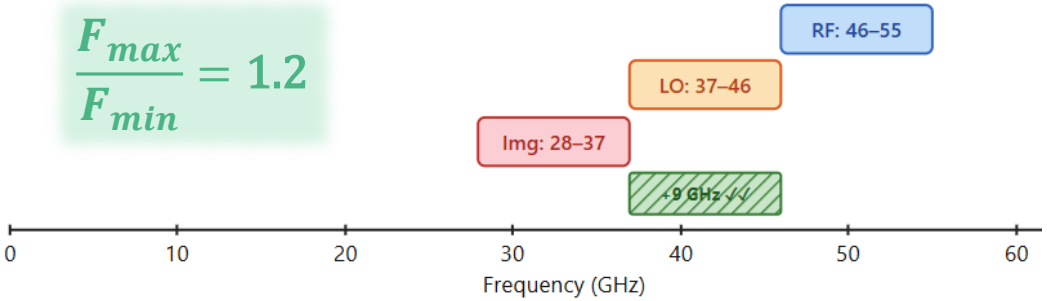
Splitting approach



$$\frac{F_{max}}{F_{min}} = 2$$

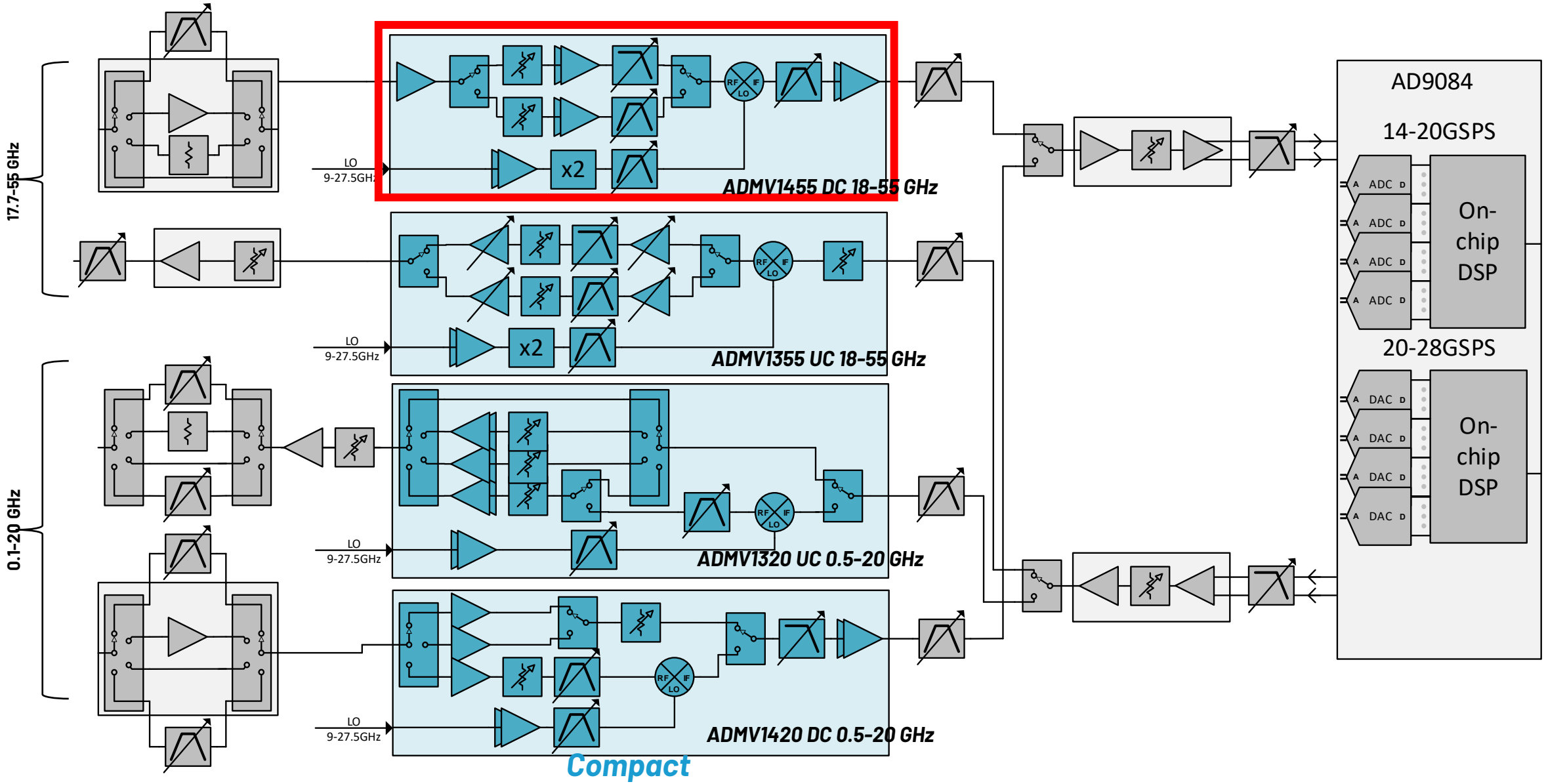


$$\frac{F_{max}}{F_{min}} = 1.53$$



$$\frac{F_{max}}{F_{min}} = 1.2$$

The Up/Down Converter Tuner ICs



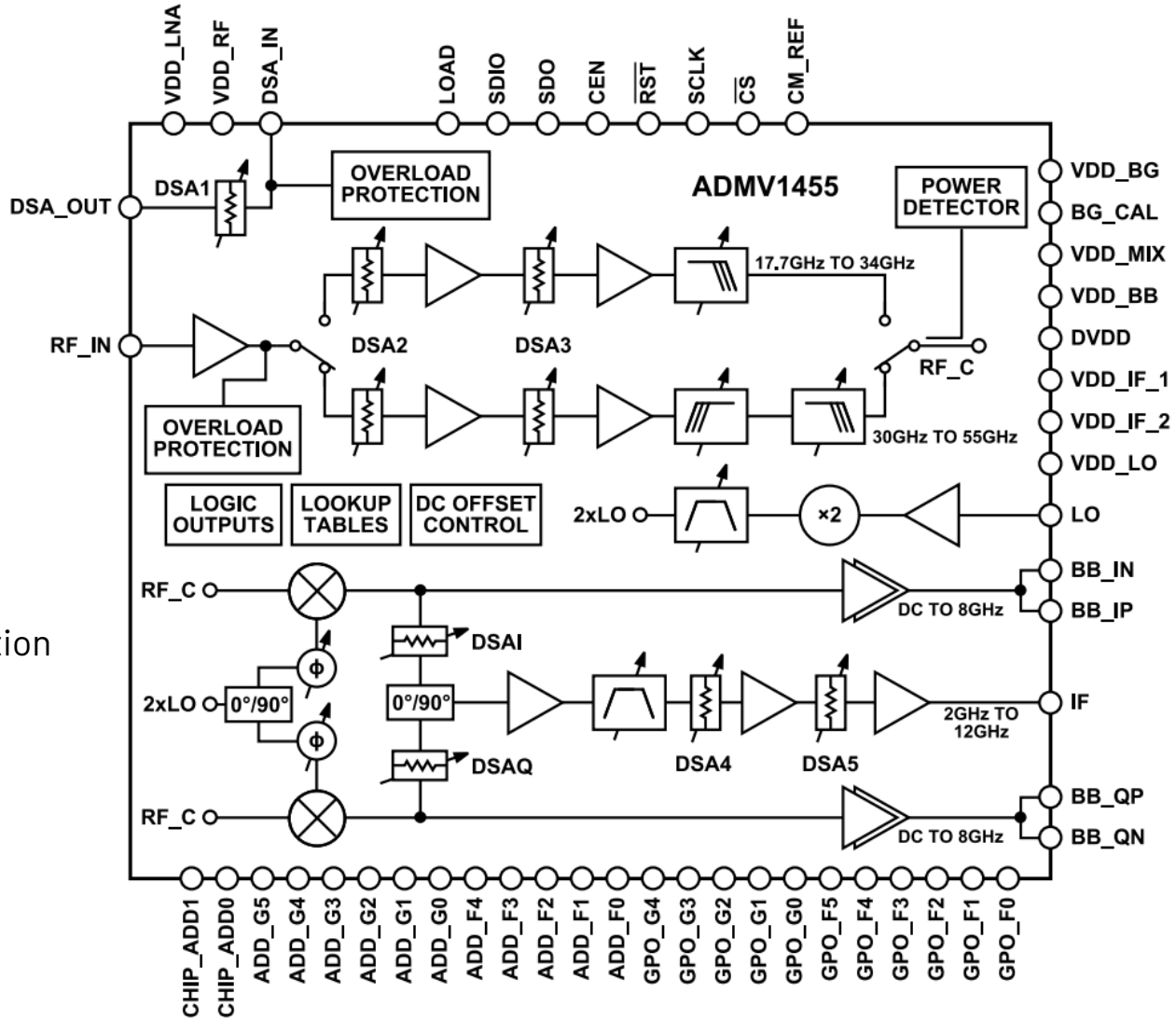
Compact Tuner ICs

ADMV1455: 17.7-55GHz Freq. Down Converter

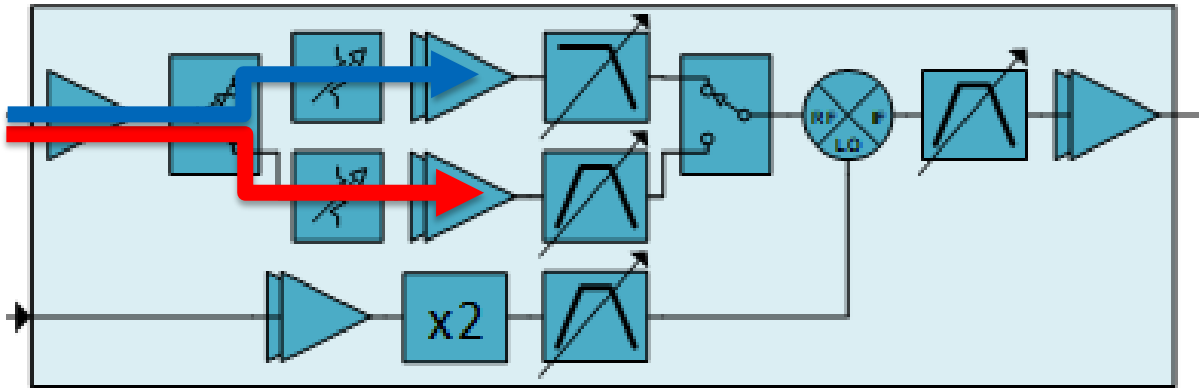
6x6.5mm BGA

Key Features ADMV1455

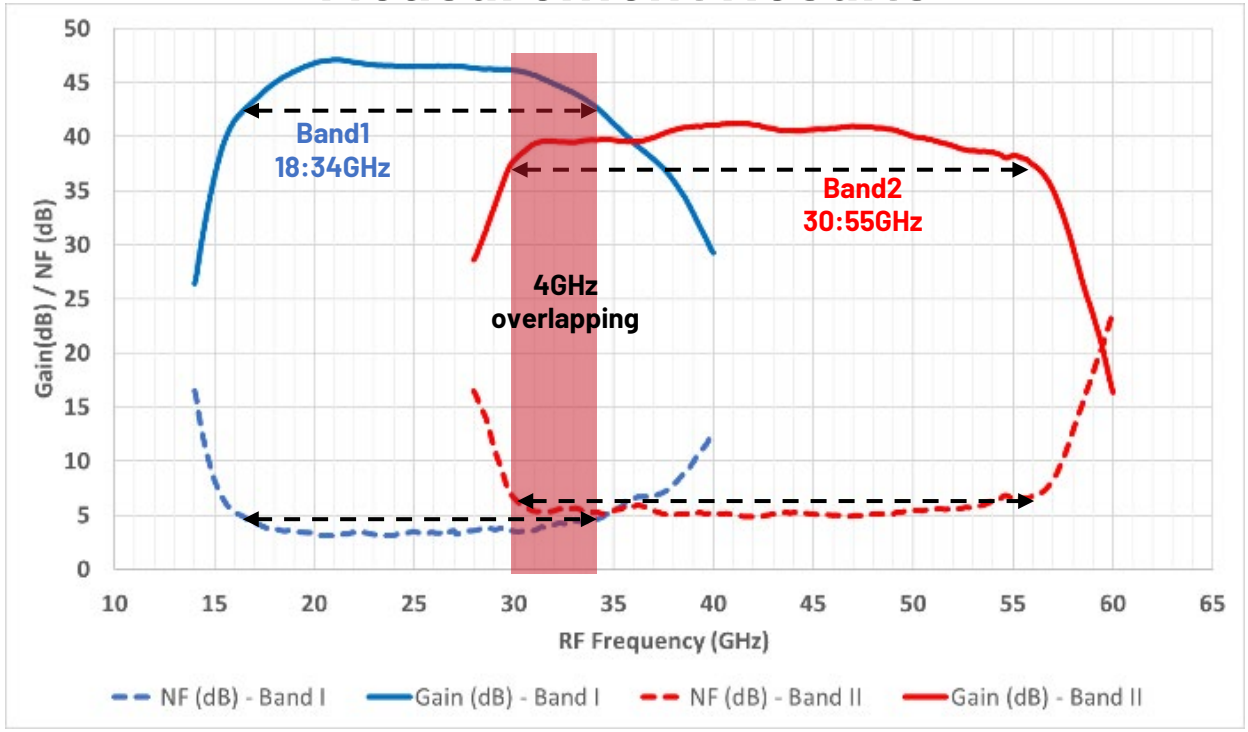
- Frequency Planning:
  - RF Freq. : 17.7-55 GHz (two bands 17.7-34 GHz, 30-55GHz)
  - IF Freq. : 2-12 GHz
  - BB Freq. : DC-8 GHz
  - LO Freq. : 8.85-27.5 GHz
- Performance (IF mode, RF_IN Path, High Band):
  - Gain:48dB, IP1dB/IIP3:-34dBm/-24dBm, NF:4.5dB
- Gain Control range: RF/IF, step: 36 dB/30dB, 1dB step
- RF/LO/IF Tunable filters
- IMR calibration knobs: Phase 1Deg, Amp 0.1dB
- I/Q BB Programmable (common-mode voltage, DC offset)
- Power detectors with programmable power-down overload protection
- Power consumption: **1W** from 1.8V & 2.5V supplies
- NVM factory calibration to minimize part to part variations
- Simple SPI: 3-wire or 4-wire
- General-purpose logic outputs for integration with other chips
- Look-up tables for fast frequency hopping applications



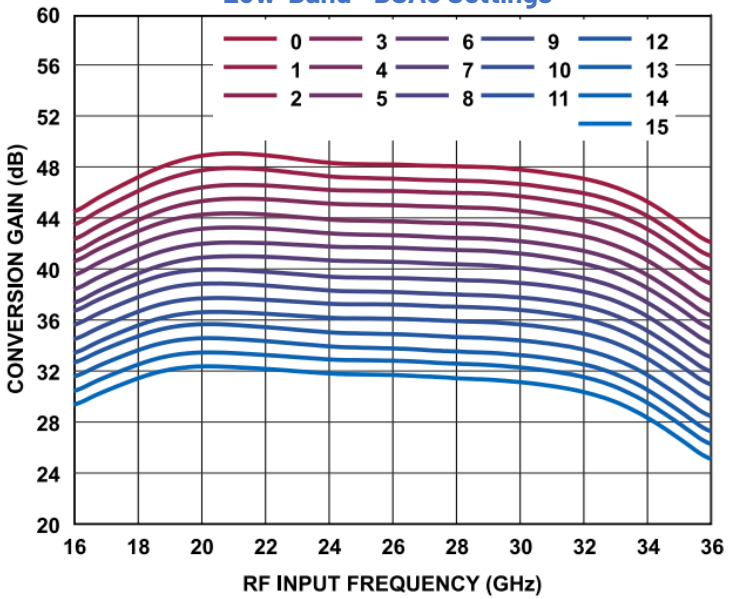
ADMV1455: 17.7-55GHz Freq. Down Converter



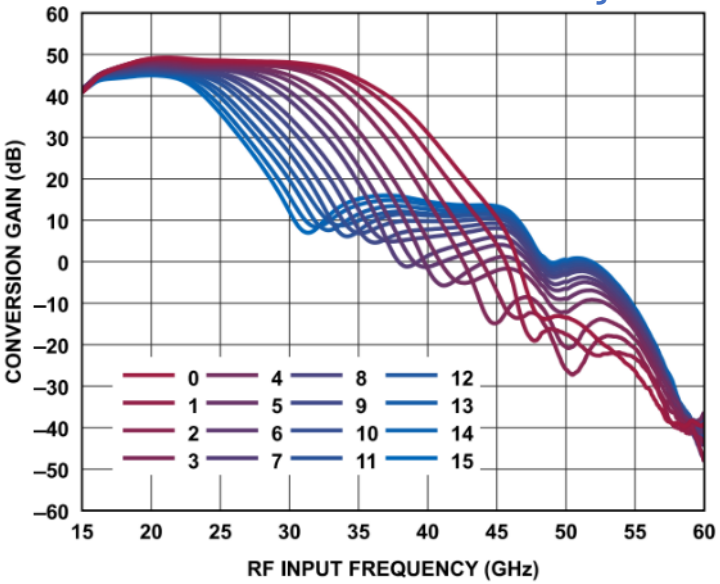
Measurement Results



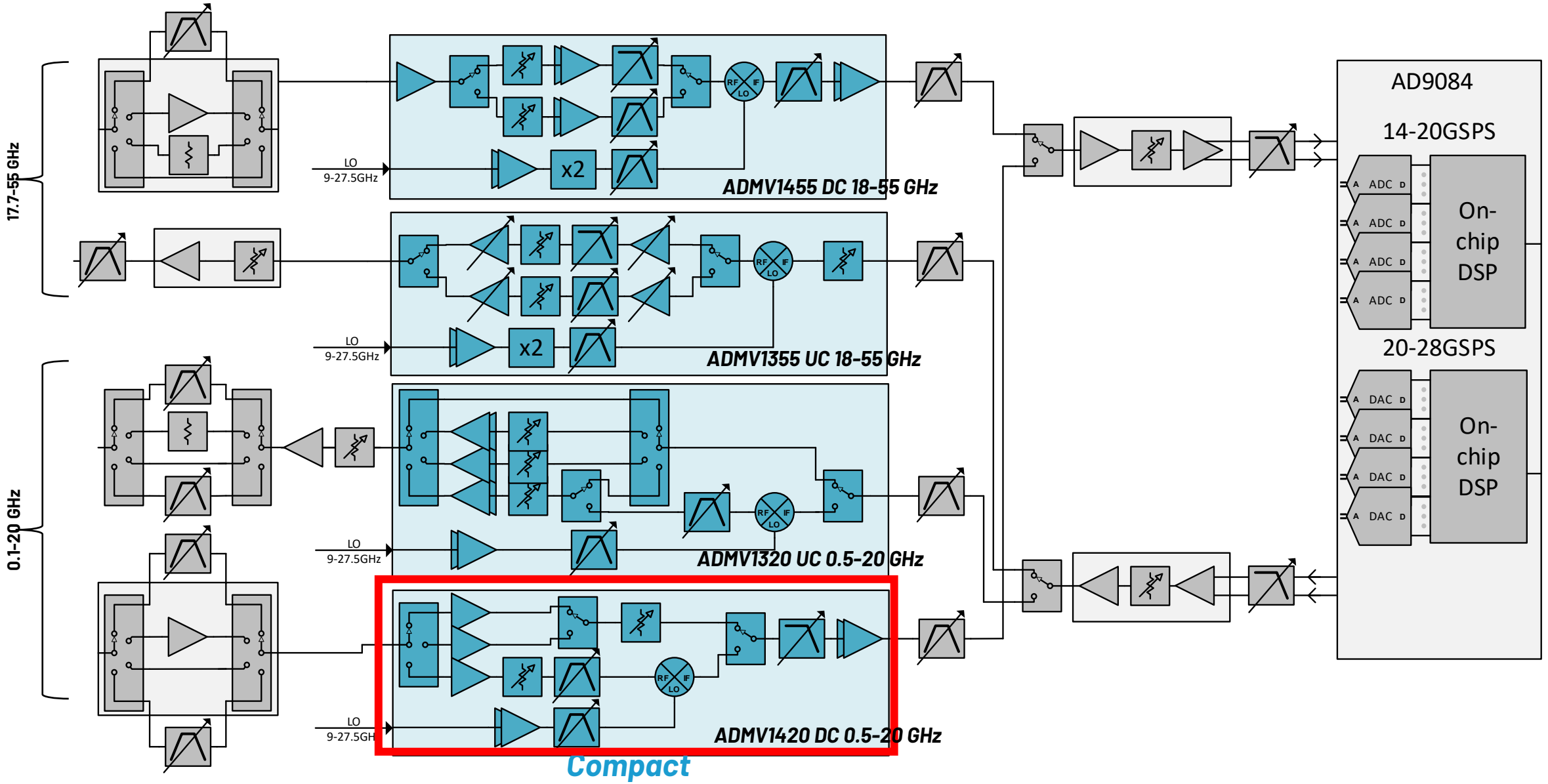
Low-Band - DSA3 Settings



Low-Band – Low-Pass Filter Settings

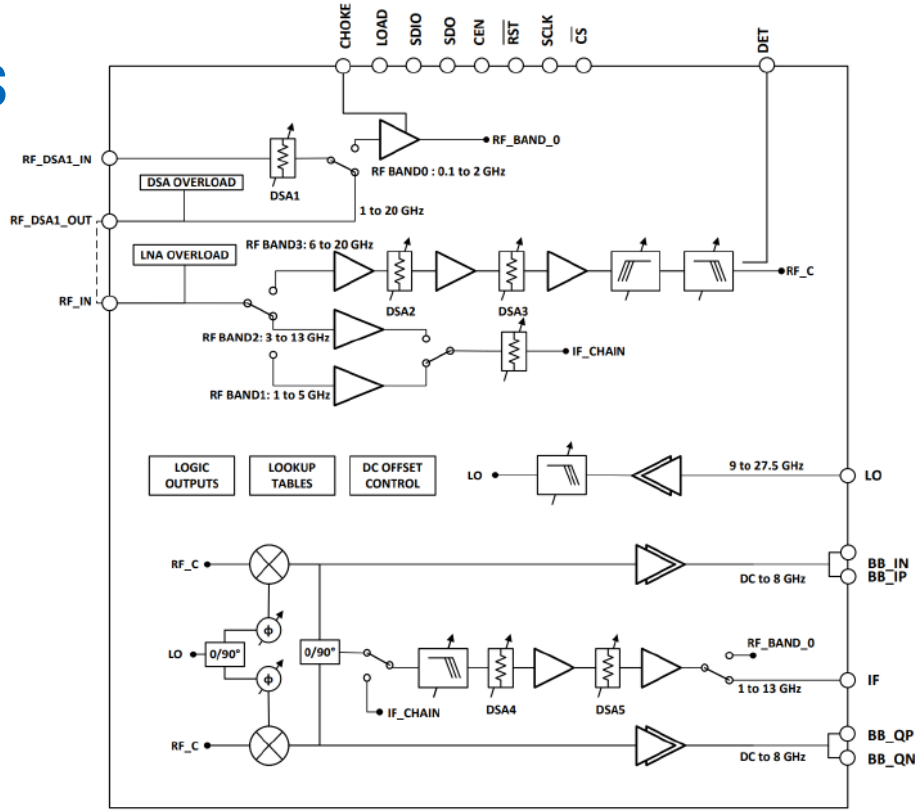


The Up/Down Converter Tuner ICs



Compact Tuner ICs

DC Block Diagram & Main Features



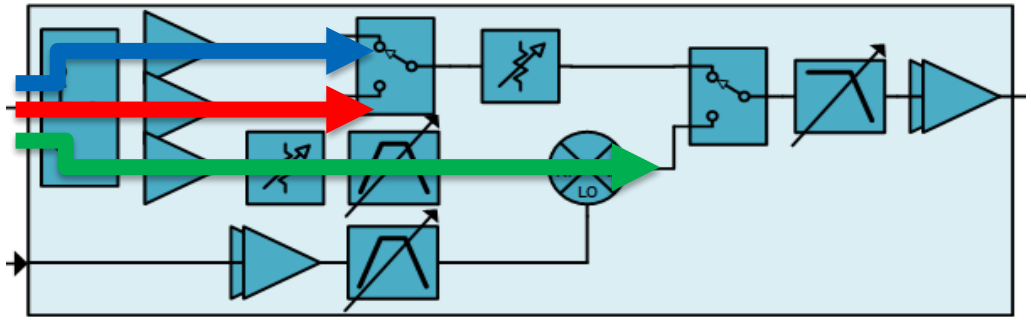
Key Features ADMV1420

- RF freq: 0.1-20GHz (4 bands)
  - Direct sampling: **B0**:0.1-2GHz, **B1**:1-5GHz, **B2**:3-13GHz
  - Mixer mode: **B3**: 6-20GHz
- IF freq: 1-13GHz (2 bands 1-5, 3-13GHz)
- BB freq: DC-8GHz
- LO freq. range: 9-27 GHz
- Gain: 20-25dB (B1/2:25dB, B3:20dB)
- Noise Figure: 7-9dB (B1:7dB, B2:8dB, B3:9dB)
- IP1dB/IIP3: -10dBm/0dBm
- Gain Control range: (B1/2:45dB, B3:51dB), 1dB step
- LO/RF tunable filters
- IMR cal. Knobs Phase 1deg, Amp 0.1dB
- RF detector at the Mixer input

Key Features ADMV1420 cont.

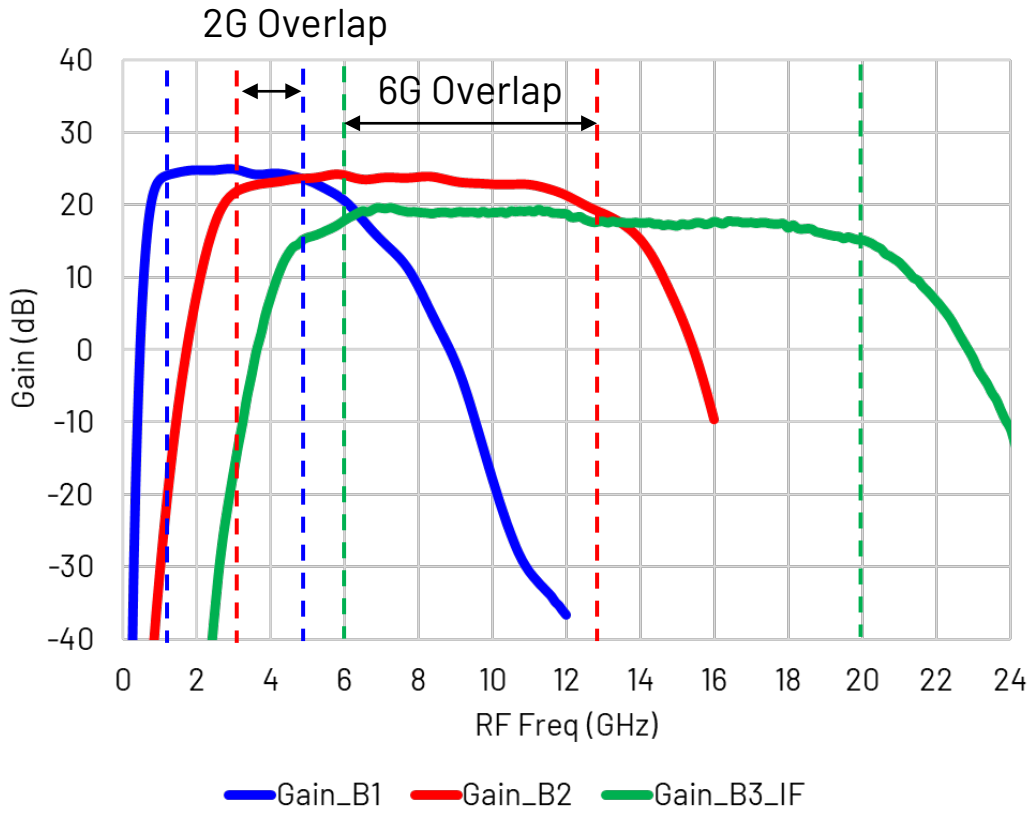
- Overload detectors at RFin & DSAin
  - Protect the part from unwanted large blockers
  - Programable threshold
- Power consumption:
  - Direct sampling: B0: 200mW, B1: 560mW, B2: 530mW
  - Mixer mode: B3 IF Mode: **1.1W**, B3 BB Mode: 1.8W

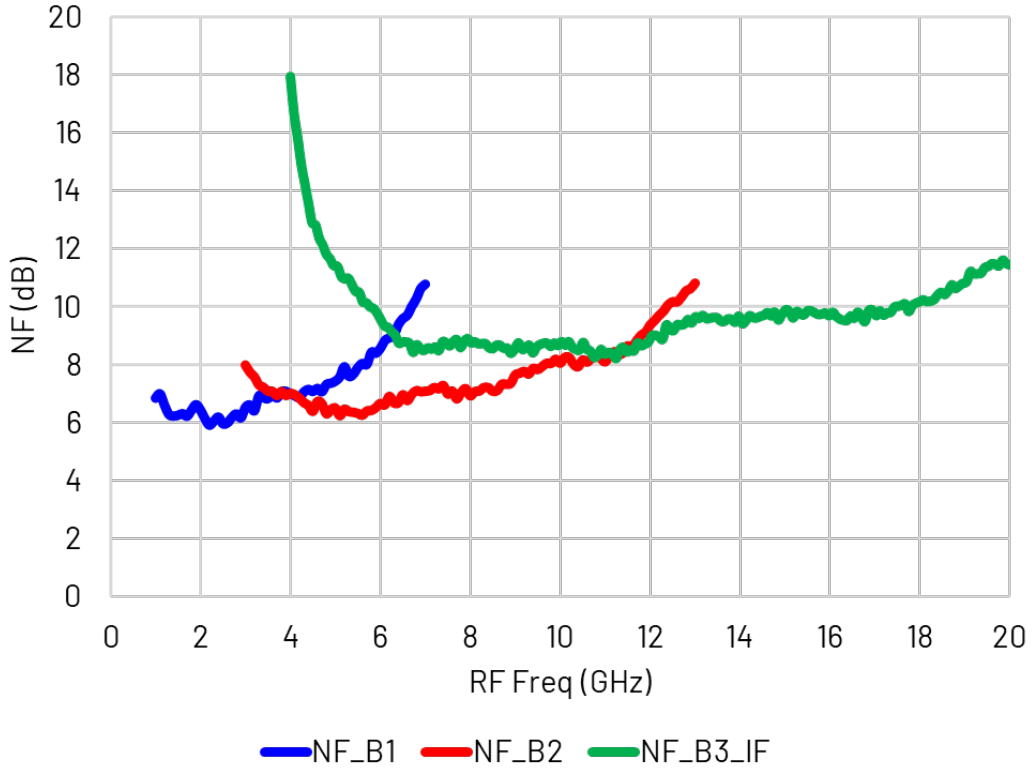
Measurements Summary: Gain & NF



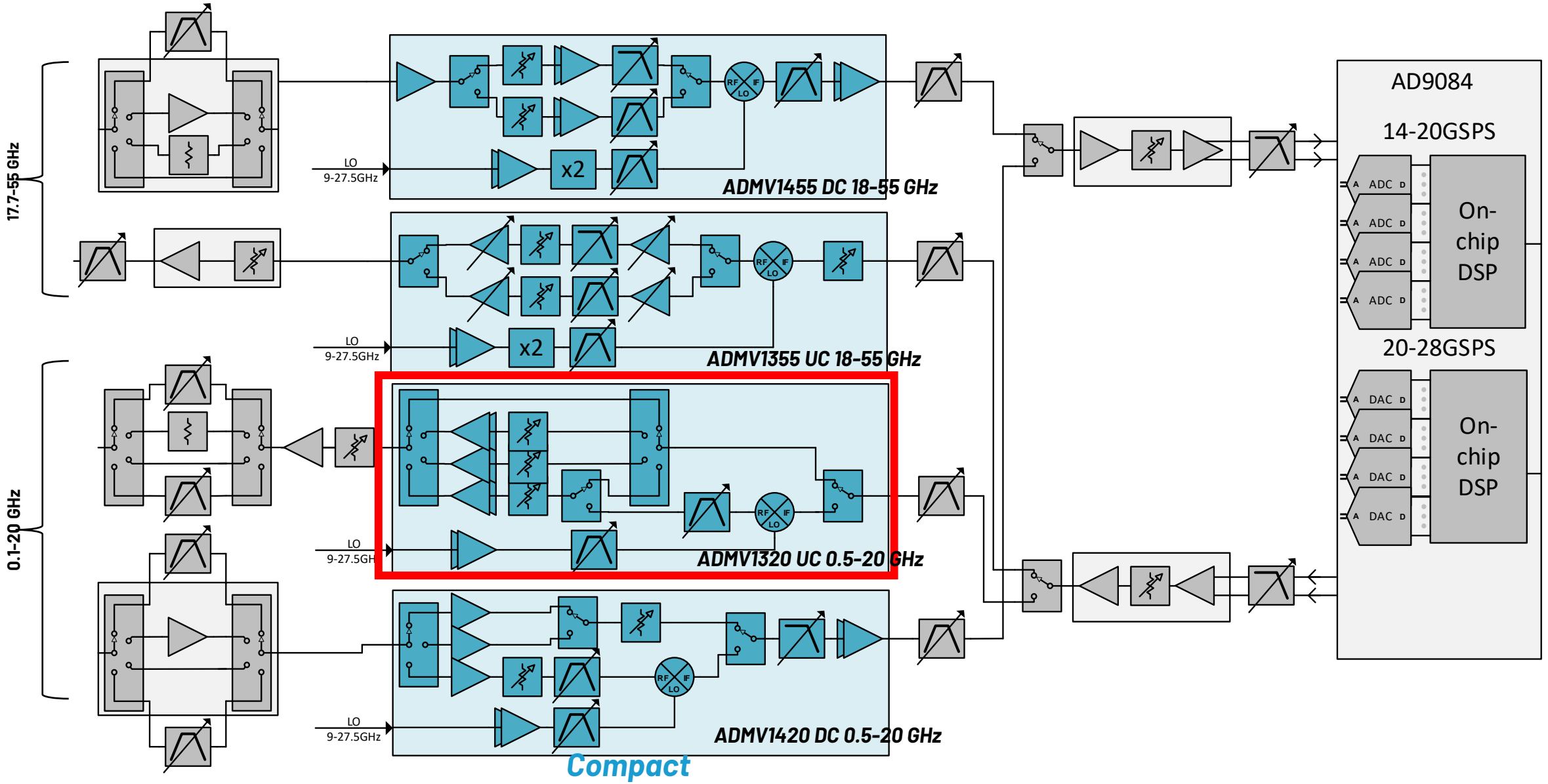
ADMV1420 Performance:

- Wideband gain 20-25dB
- NF: 6-10dB
- Overlap between freq. bands





The Up/Down Converter Tuner ICs



Compact Tuner ICs

ADMV1320: 0-20GHz Freq. Up Converter

Key Features ADMV1320

- RF freq: 0-20GHz (4 bands)
  - Direct sampling: **B0**:0-2GHz, **B1**:1-5GHz, **B2**:3-13GHz
  - Mixer mode: **B3**: 6-20GHz
- IF freq: 1.7-9GHz
- BB freq: DC-12GHz
- LO freq. range: 9-27 GHz
- Gain: 15-20dB (B1:17dB, B2:20dB, B3:17dB)
- OP1dB: 18-14dBm (B1:16dBm, B2:17dBm, B3:15dBm)
- OIP3: 25dBm
- Gain Control range, step: 30dB range, 1dB step
- LO/RF tunable filters
- IMR cal. Knobs Phase 1deg, Amp 0.1dB
- LO Nulling loop
- Power consumption is **1.15W** for mixer IF mode

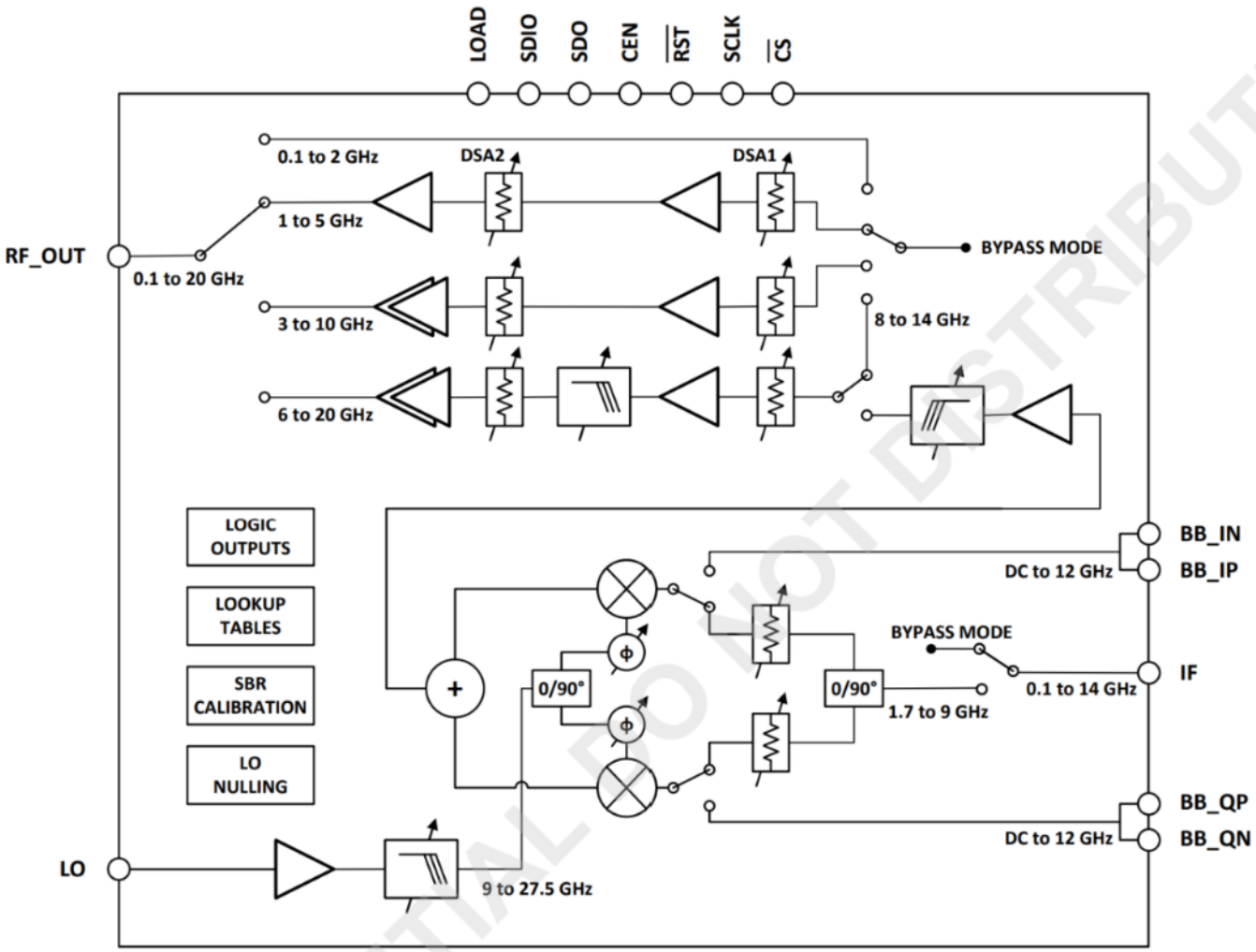
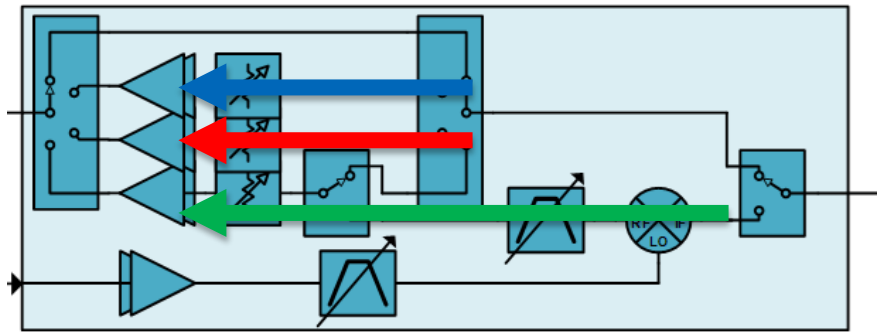


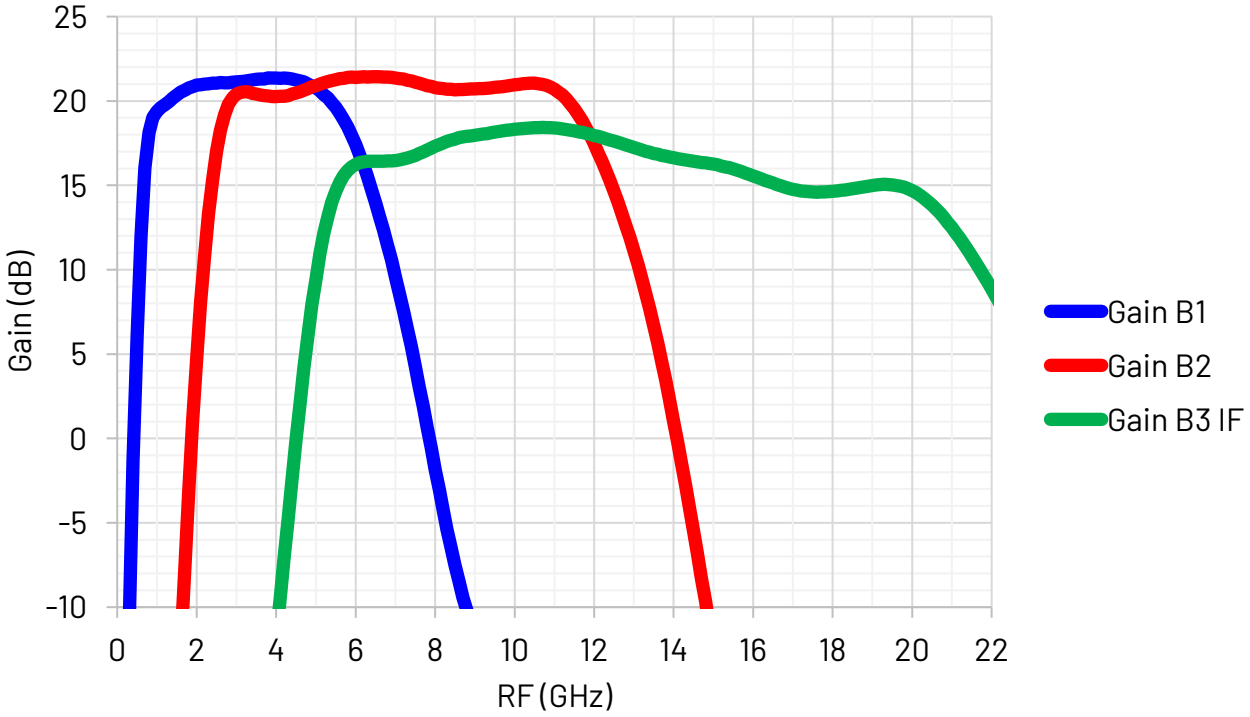
Figure 1.

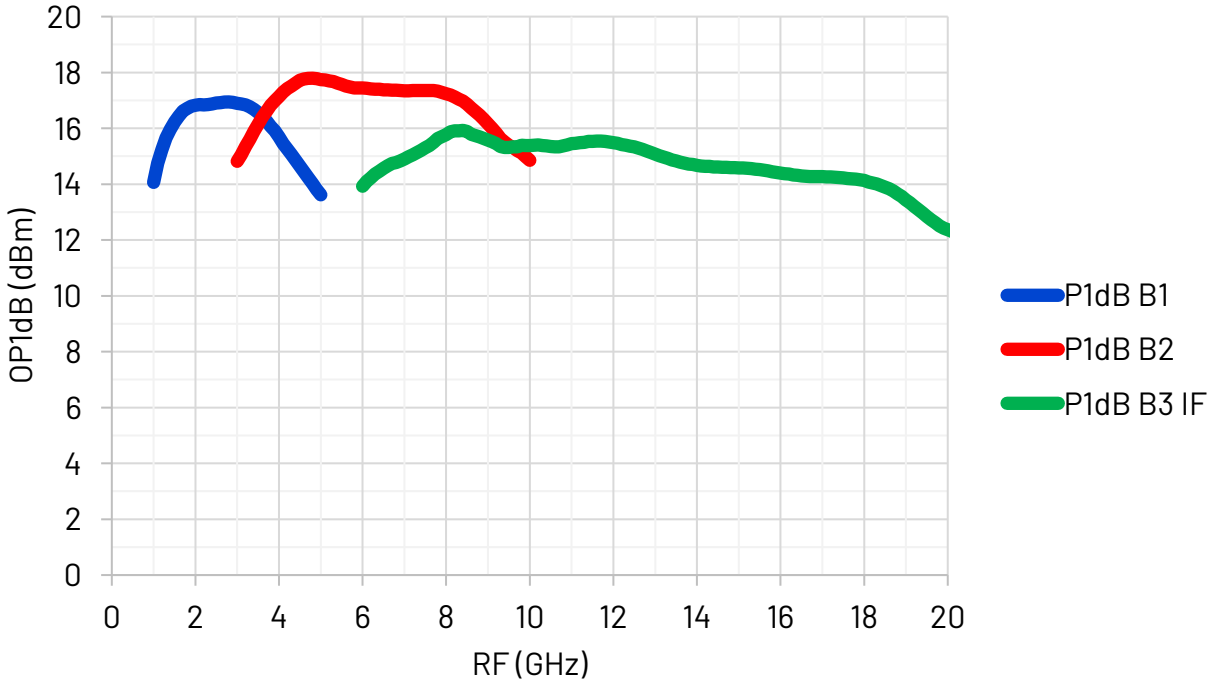
Measurements Summary: Gain & OP1dB

ADMV1320 Performance:

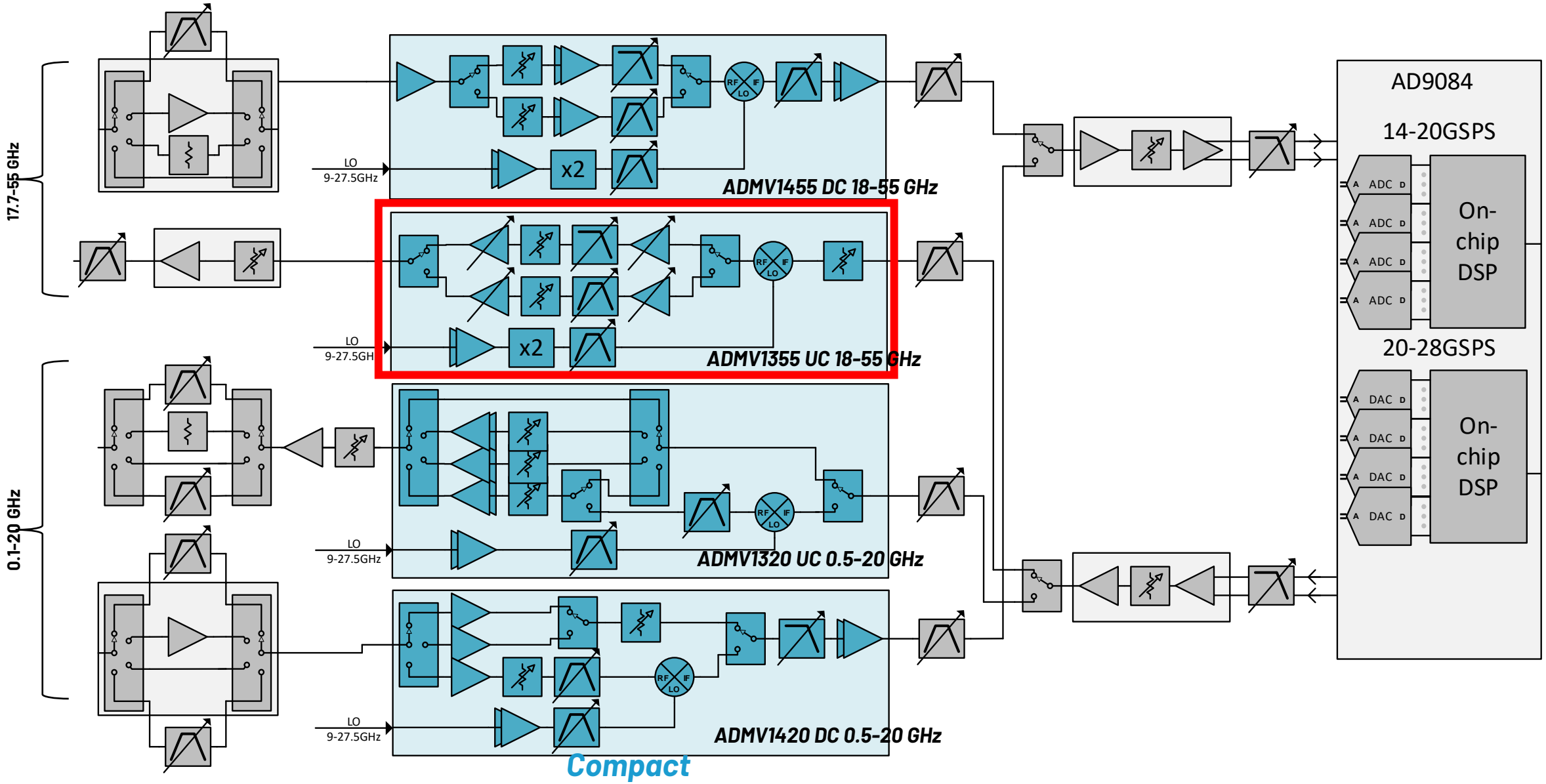
- Gain: 15-20dB
- OP1dB > 14:18dBm







The Up/Down Converter Tuner ICs



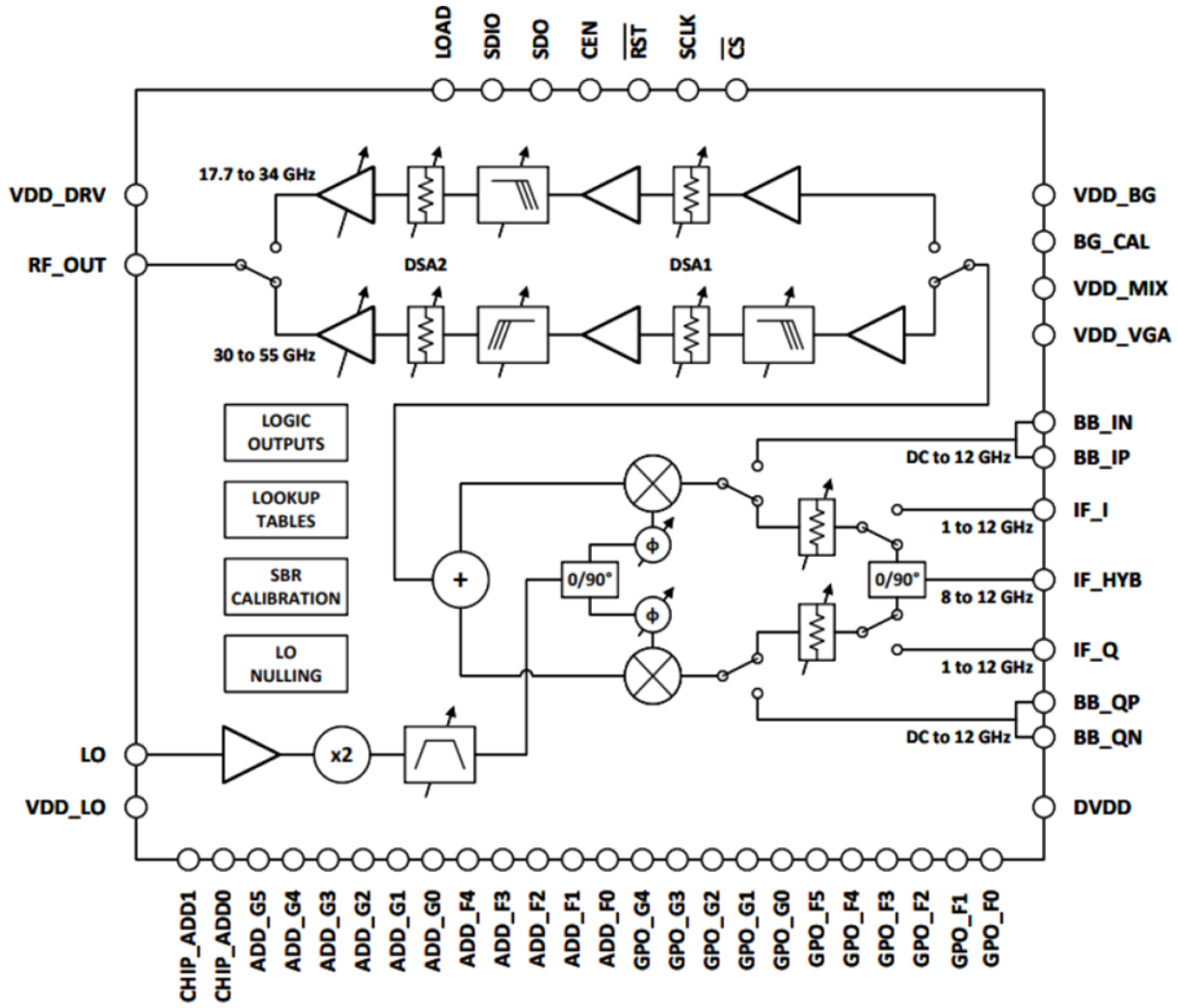
Compact Tuner ICs

ADMV1355: 18-55GHz Freq. Up Converter

Key Features ADMV1355

- RF freq: 18-55 GHz (two bands 18-34, 30-55GHz)
- IF freq: 1-12 GHz (two bands 1-4, 3-12GHz)
- BB freq DC-12 GHz
- Gain: 20dB
- OP1dB/OIP3: 15dBm/25dBm
- Noise Figure: 15dB
- Gain Control range, step: 30 dB, 1dB step
- LO/RF Tunable filters
- IMR cal knobs Phase 1Deg, Amp 0.1dB
- Power consumption: **0.9W** from 1.8V & 3V supplies

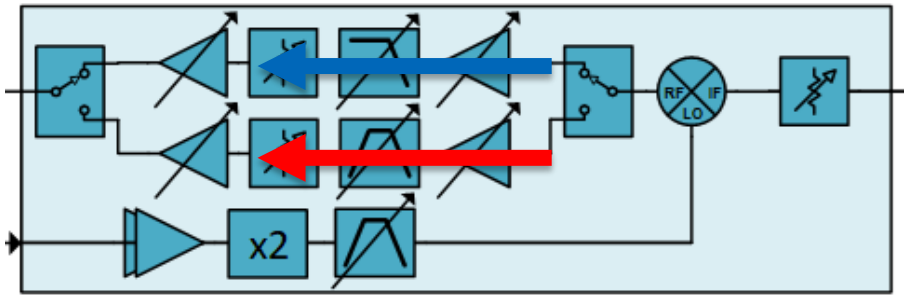
6.5x6mm BGA

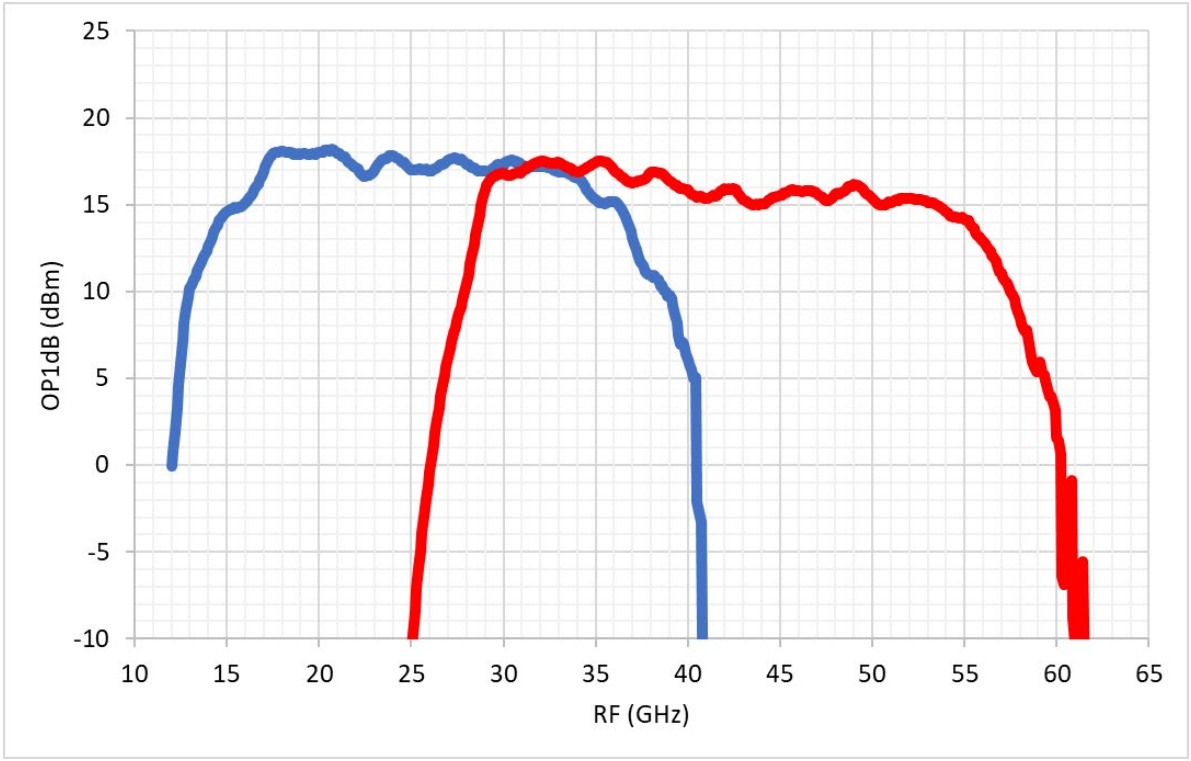


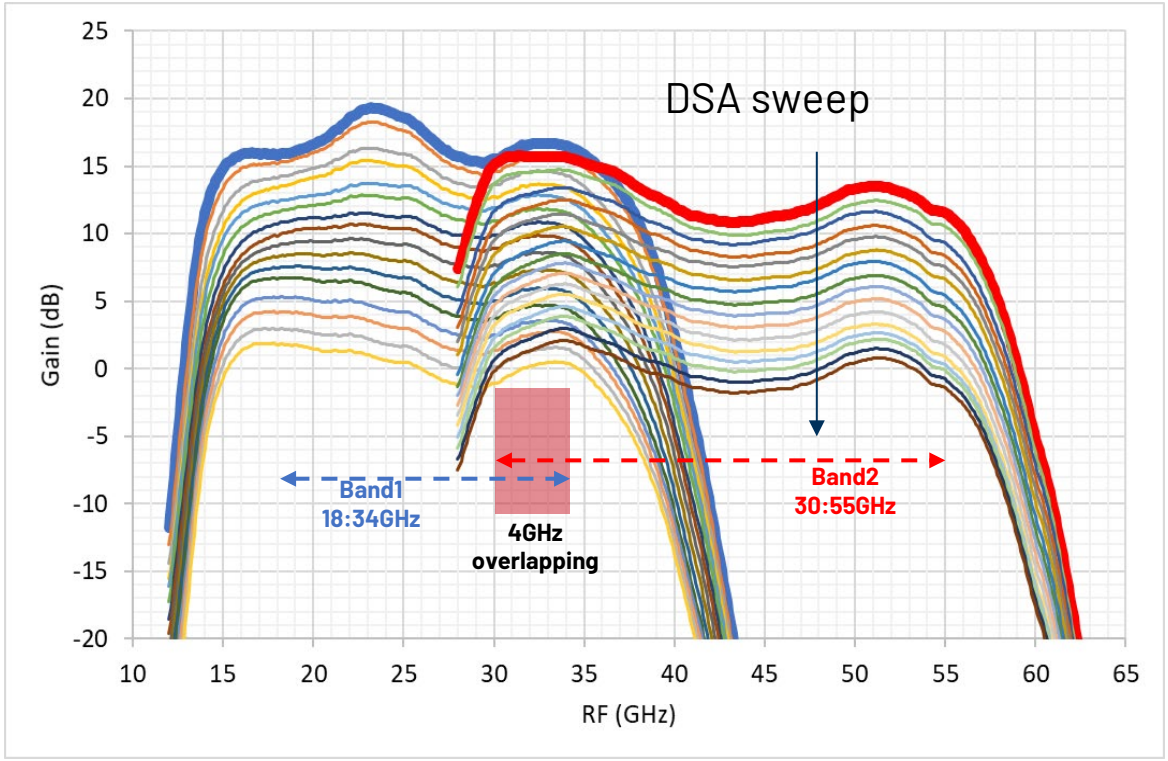
ADMV1355: 18-55GHz Freq. Up Converter

ADMV1355 Performance:

- Gain: 13-18dB
- OP1dB > 15-17dBm

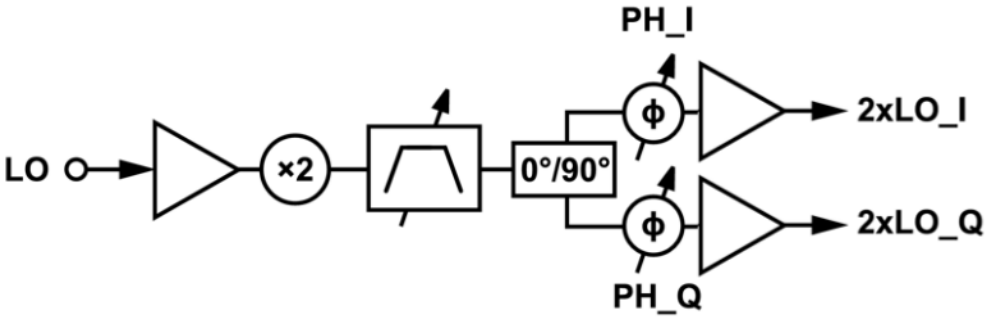




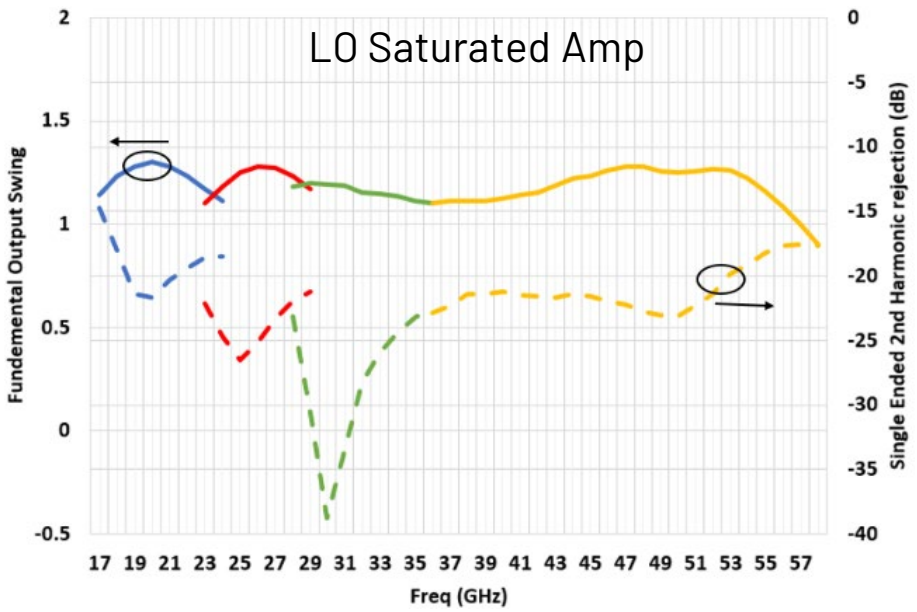


LO Generation

- Input LO freq range: 8.85-27.5 GHz (Single Wideband design with harmonic traps)
- LO input power range [-7dBm to –3dBm] LO freq<25Ghz
- LO input power range [-3dBm to 0dBm] LO freq>25Ghz
- Internal X2 Multiplier (with 8-bits band control and harmonic traps)
- Tunable LO harmonic rejection Filters
- IQ phase correction with a 5-bits I & Q Phase Shifters
- Typical Phase Shifter resolution ~0.6° with +/-20° range, across 32 states.

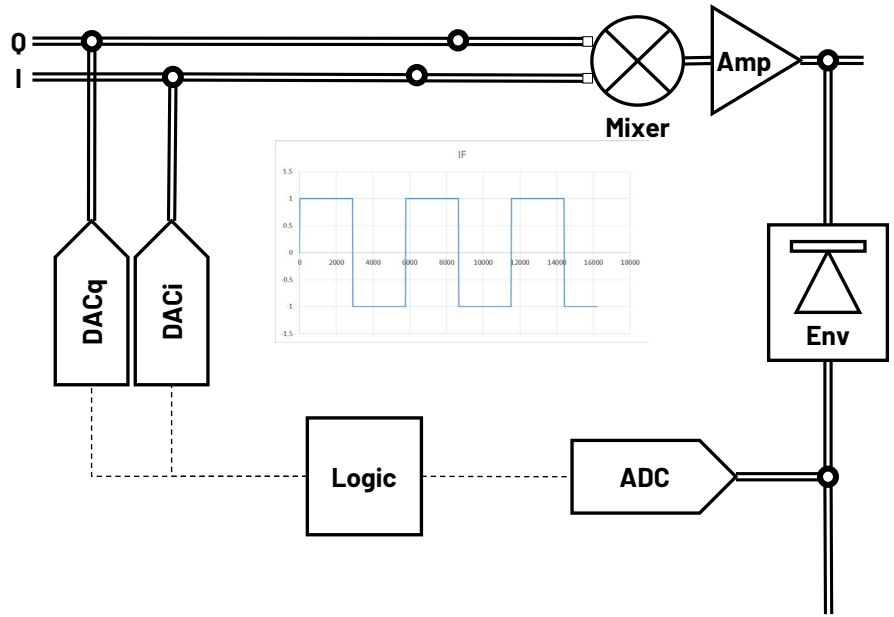


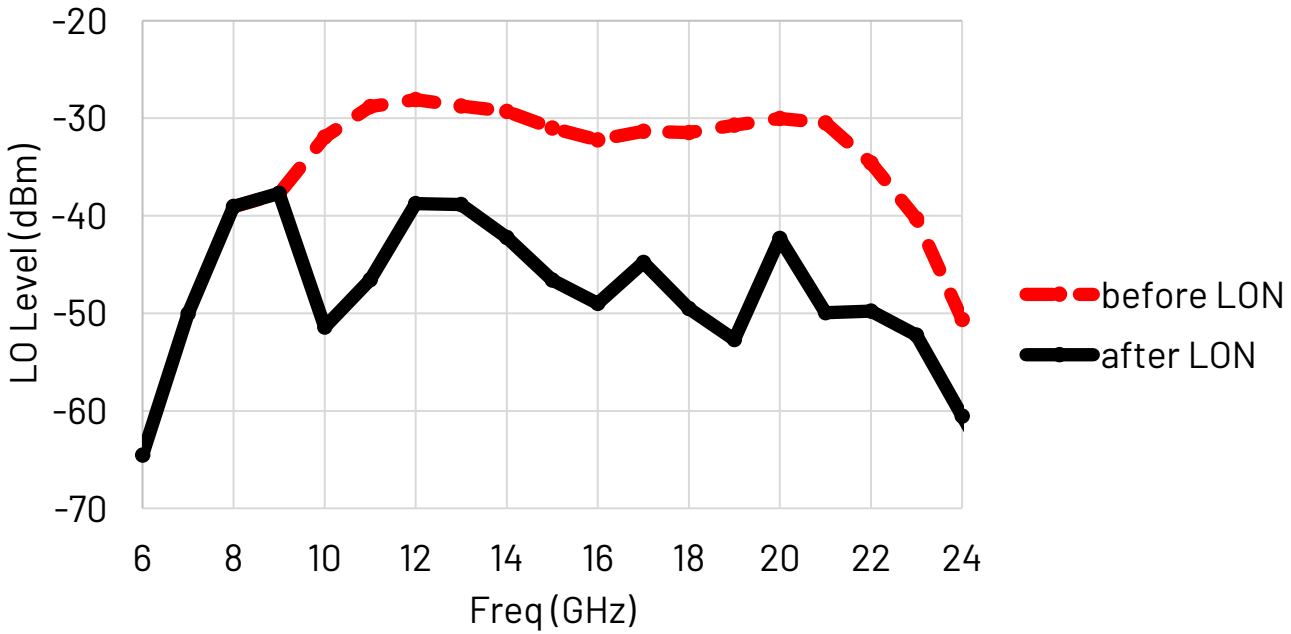
LO Chain Diagram



LO Nulling Loop

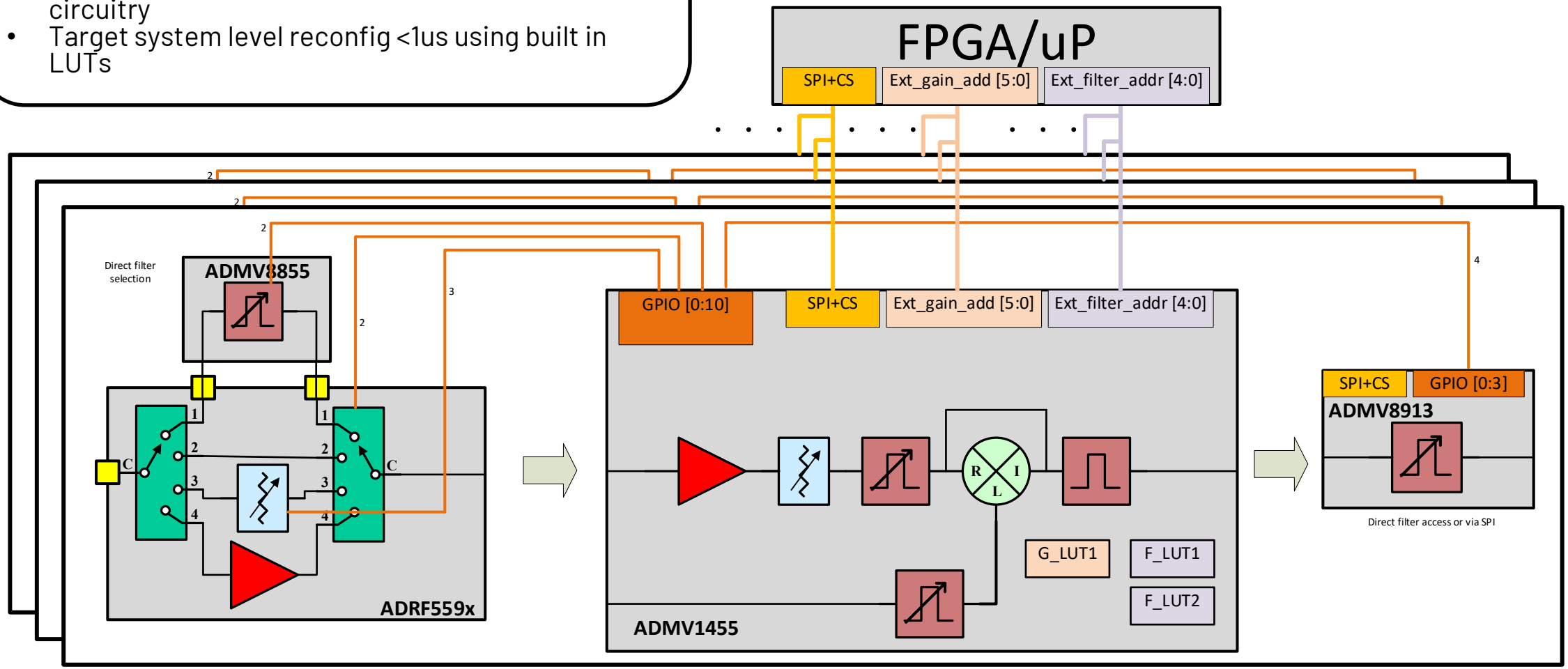
- Offline calibration
- Depends on injection of +ve and –ve DC offset using DAC at IF port
- The logic calculates the difference which represents the real LO leakage of the mixer
- Depending on the polarity of the difference, the DAC injection increases in the +ve or the –ve direction until the loop cancels this difference so achieving good LO feedthrough





Control and Timing

- Control of multiple channels and/or multiple bands from single address bus
- Separate control for Gain/Level and Frequency tuning
- RF Converter RFIC acts as hub for surrounding circuitry
- Target system level reconfig <1us using built in LUTs



Filtering

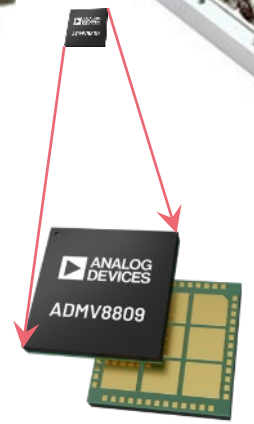
Problem statement – Filters within Multi-Octave Systems

Switched fixed filters cannot meet the flexibility, rejection requirements and size constraints of 0.1-55 GHz multifunction systems.

Challenges:

- PCB real estate of filter solutions is too large
- Providing low-loss, high-rejection tunability across multi-octave frequency spans
- Supporting fast band changing for adaptive applications

Discrete/Modular vs Tunable Compact Filters



Modular Fixed Filters with RF Switches:

Pros: Loss, Rejection, Switching Speed, Linearity

Cons: SIZE, COST, Limited Flexibility

Tunable Compact Filters:

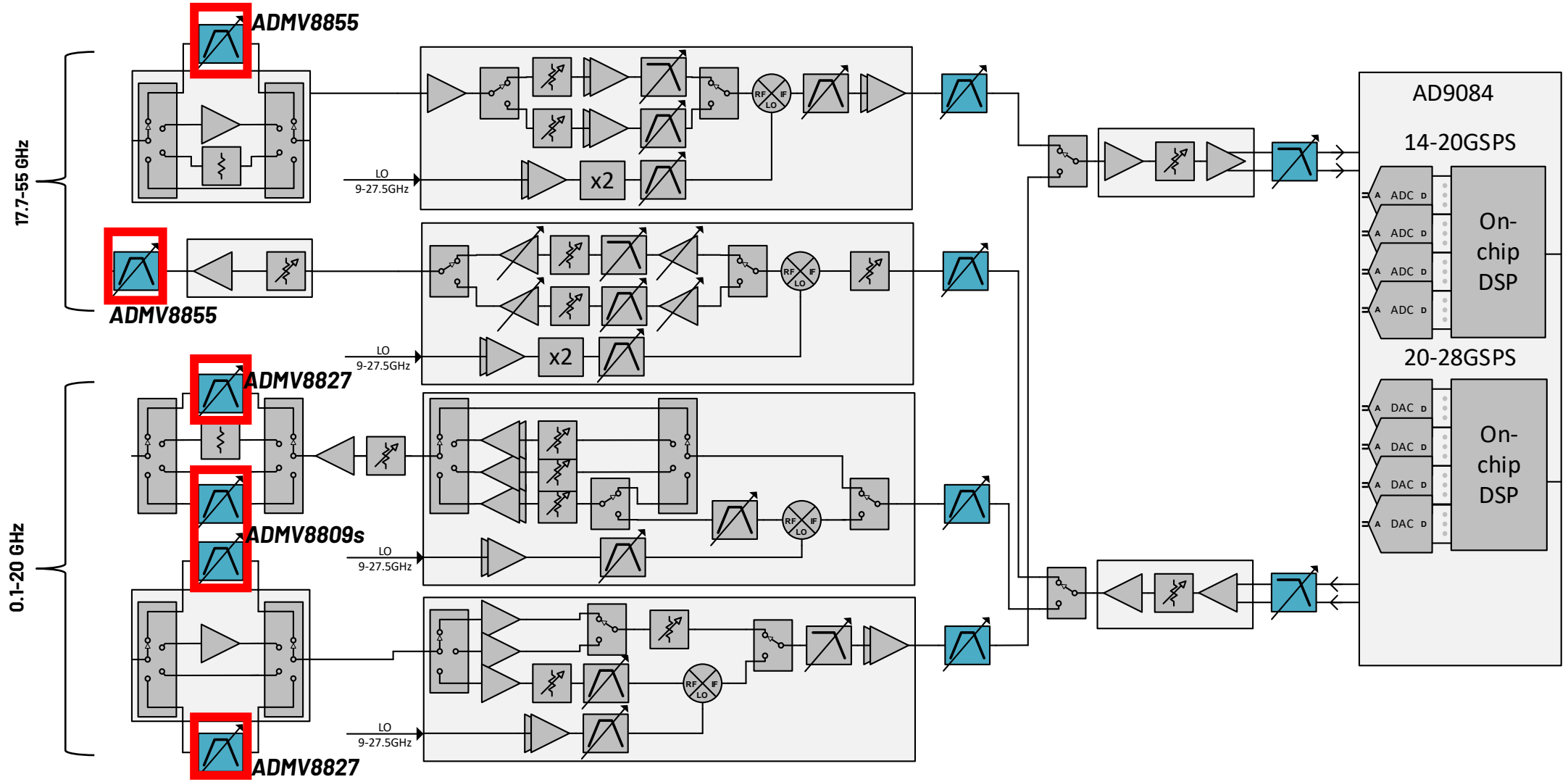
Pros: Size (Scales with 1/(tuning range)), Corner Frequency Flexibility, Cost

Cons: Loss, Rejection, Switching Speed, Linearity

ADI Solution to Adaptive RF Filters:

- Size & Cost: 3-8mm large and 1mm tall SMD packaging at pricing orders of magnitude lower than Modules!
- Loss : Integrating Silicon ICs and Hi-Q components inside package!
- Rejection: Optimization between Rejection, Loss and Tuning (Target 40-50dBc Rejection on PCB)
- Switching Speed: 500ns useful for most applications (100-200ns target when possible)
- Linearity: 45dBm IIP3 comparable to Modules (Much better than Varactor based solutions)
- Flexibility: Tuning of Corner Frequencies for Adaptive Rejection (Tuning with minimal impact on Loss)

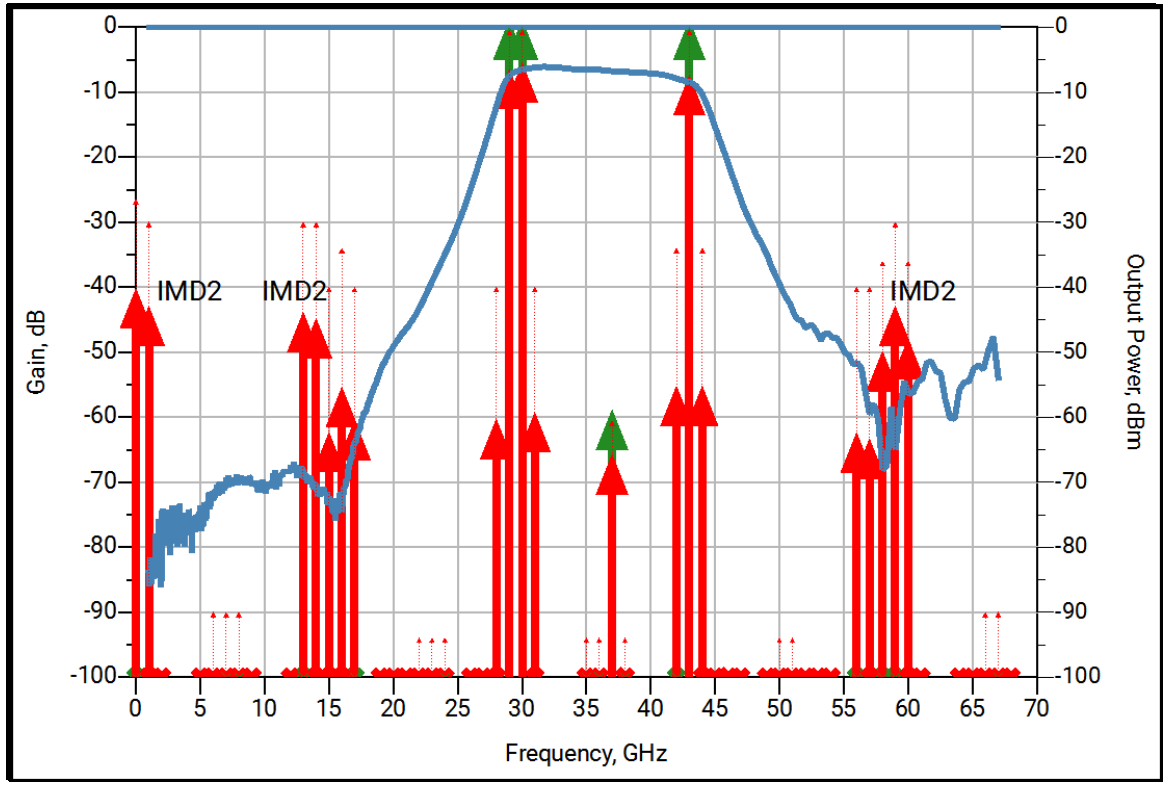
FrontEnd Filters:ADMV88XX



SpuriousFreeDynamicRange Limitations at FrontEnds

Intermod Scenario for ultra-wideband system:

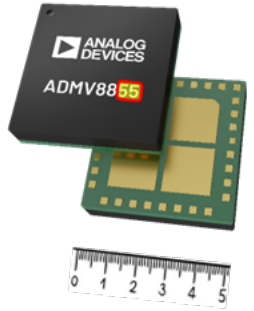
- Signal of Interest at 37GHz
- 3 relatively strong Signals/Interferers
  - 30dB below IIP2 and 20dB below IIP3
- IMD2s are strong at -30dBc (2nd HD -36dBc)
- IMD3s at -40dBc (-34dBc with 3 carrier mix)
- 20dB Attenuation Can Help
  - IMD3s go down by 60dB but IMD2s by only 40dB
- Sub-Octave Filtering!
- Strong Signals within Filter Passband
  - IMD2s are outside Band of Interest
  - IMD3s can be handled with Gain Ranging

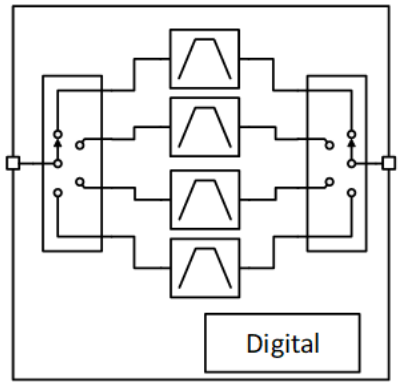


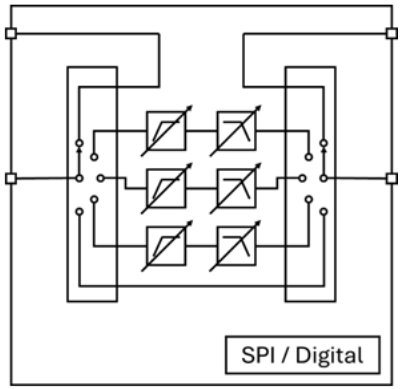
FrontEnd Filters for Out-of-band Interferers

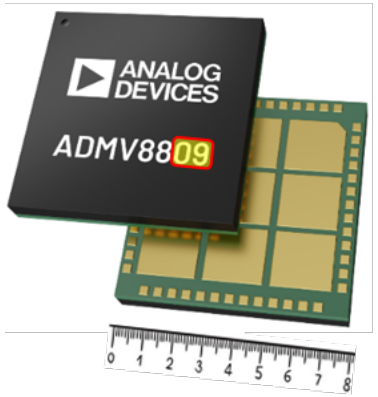
Key Features of ADMV88xx filters:

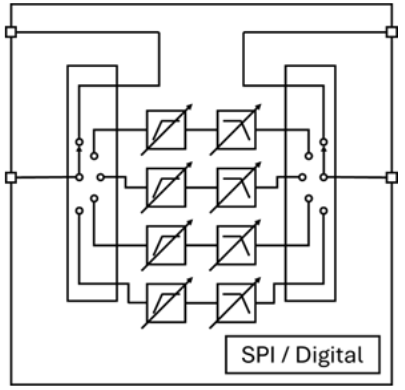
- **Sub-Octave Filtering** for Out-Of-Band Interference Rejection
- Coverage from **0.5GHz to 55GHz**
- **Corner Frequency Flexibility up to mmW**
- Typical **500ns** switching time. **<150ns** when Switching SPNT only
- High Linearity 45dBm typical IIP3
- **Cover/Absorber NOT needed for typical 50dBc rejection on PCB**
  - **Minimum 40dB Rejection of IP2s with Additional 20dB Down the Chain**
- Bypass / Through RF Paths Available
- SPI interface for HPF/LPF cutoff frequency adjustment
- External address pins enable multiple devices on the same SPI bus
- Parallel interface for random access to On-Chip lookup table (LUT)
- Space qualified and extended temperature range











FrontEnd Filter ADMV8855: 17-55 GHz BPF

Sub-Octave Filtering with 4 discrete mmW channels

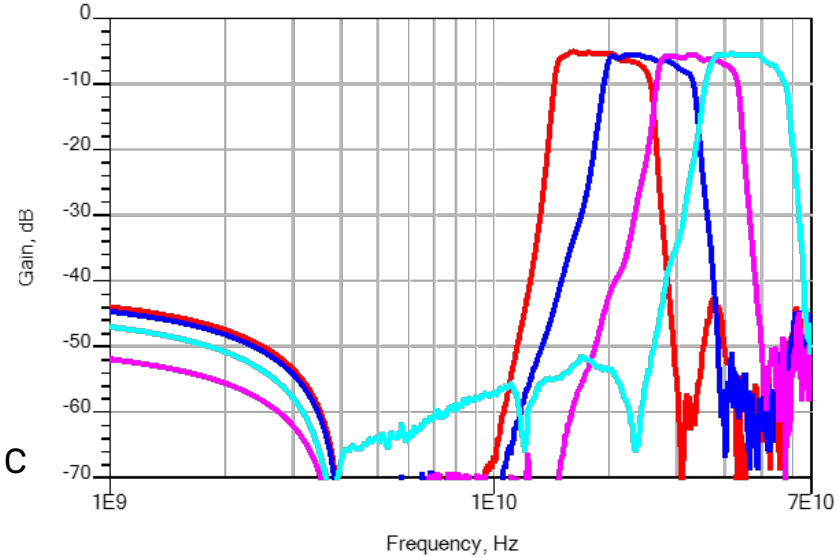
16-26GHz, 22-34GHz, 30-44GHz and 40-56GHz

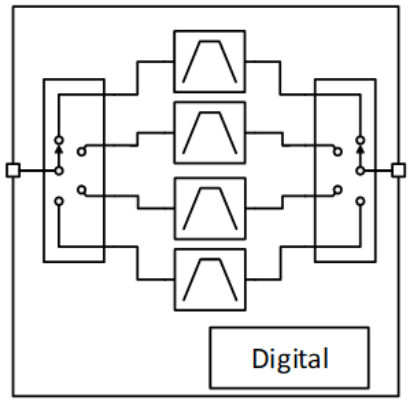
Switching Speed **<150ns**

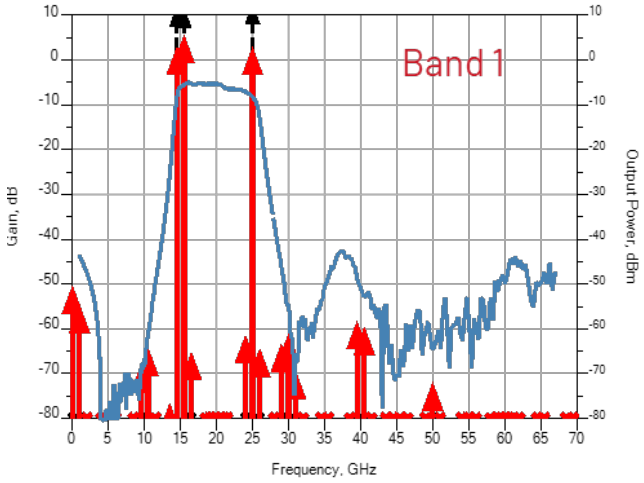
Low Loss Filtering at mmW

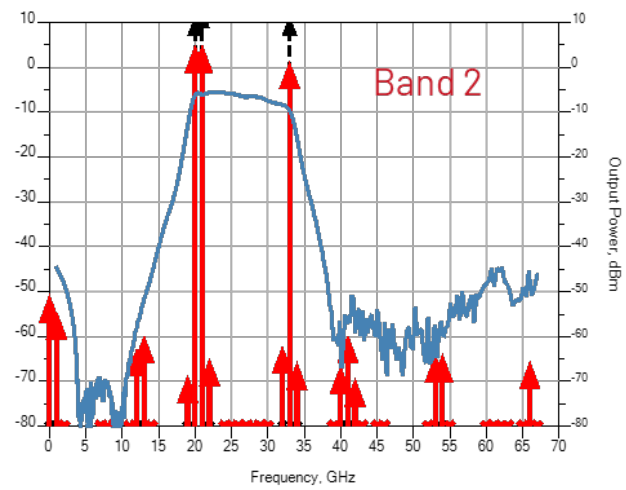
High Linearity allows high dynamic range

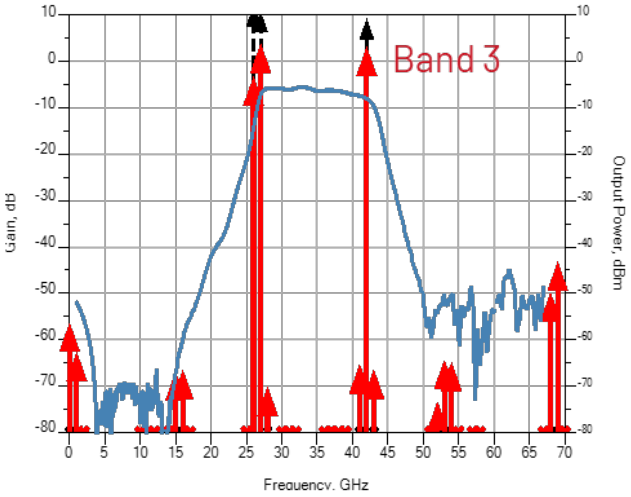
Pin 10dBm → self-generated IMD2s & IMD3s < -60dBc

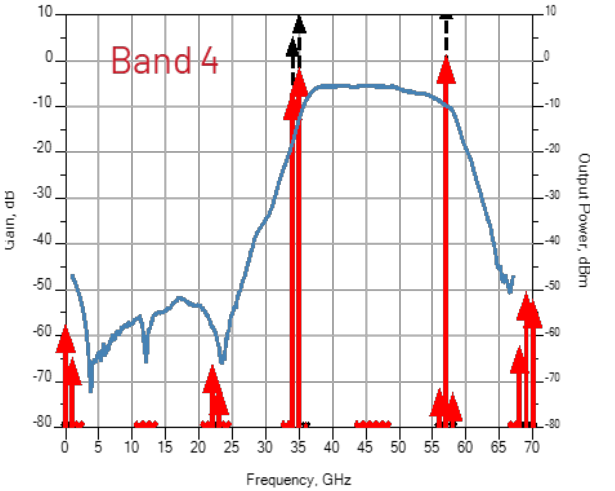












FrontEnd Filter ADMV8827: 6-26.5 GHz HPF+LPF

3Bands+Byp+Thru Widest BW States

6-12.5GHz, 10.5-18.5GHz, 16.5-26.5GHz

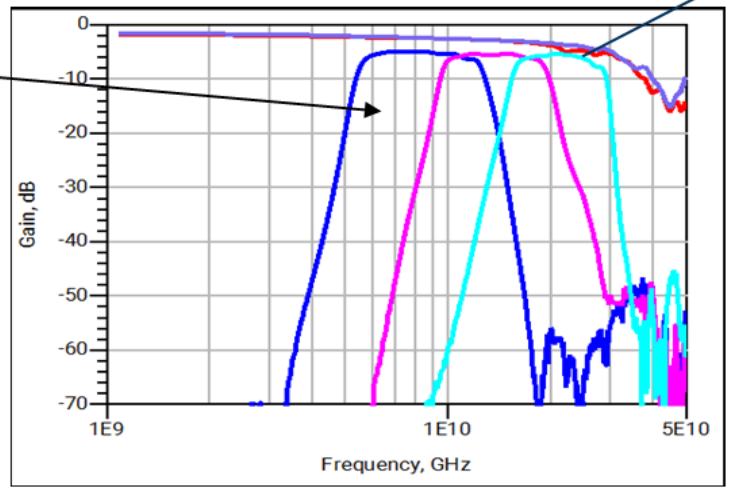
*Bypass can be used to **extend lower range** (i.e. ADMV8809)*

Sub-Octave Filtering with 3 Adaptive Channels

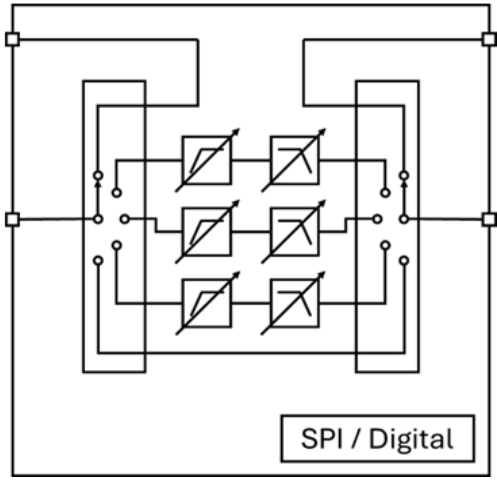
Each HPF/LPF have 8 states

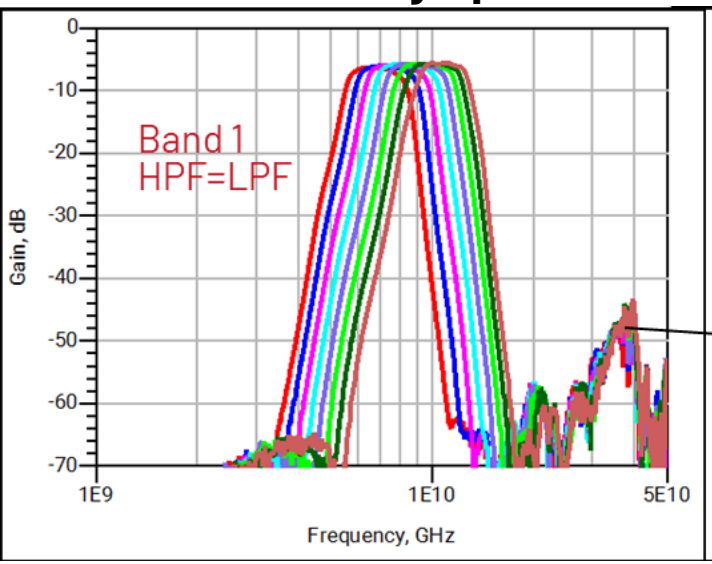
HPF=LPF States, i.e. Sub-Octave Bands shown below

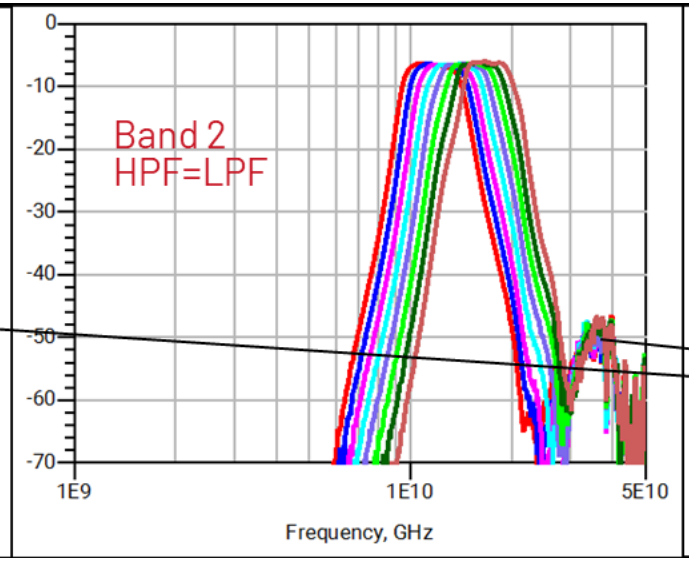
>50dBc re-entry up to 30GHz

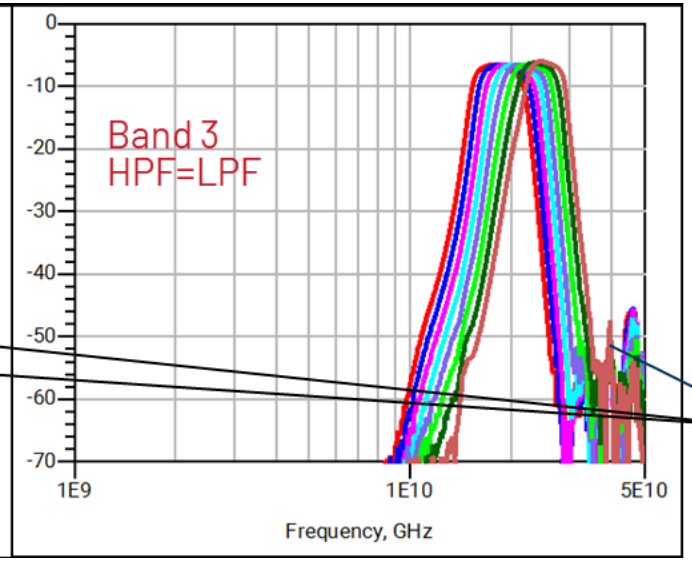


Note that Thru has better high frequency response









Absorber sheets will bring further improvement at high end

FrontEnd Filter ADMV8809: 0.5-9 GHz HPF+LPF

4Bands + Byp Widest BW States

0.5-1.2GHz, 1.1-2.4GHz, 2.2-5GHz, 4.5-9GHz

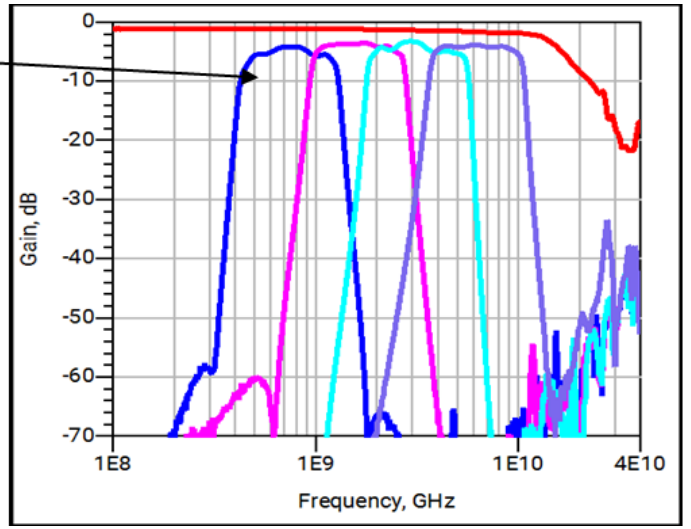
Bypass *can be used for* ***lower frequency filtering***

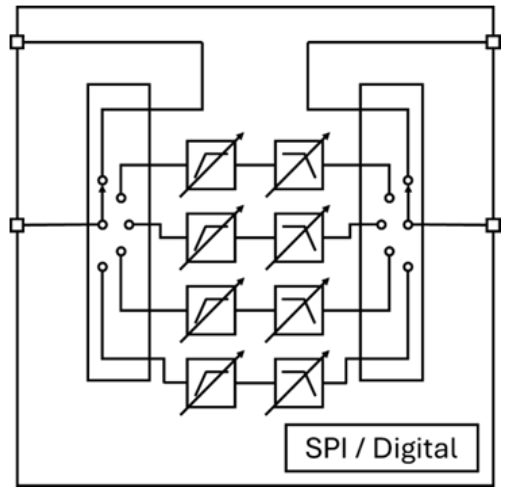
Sub-Octave Filtering with 4 channels

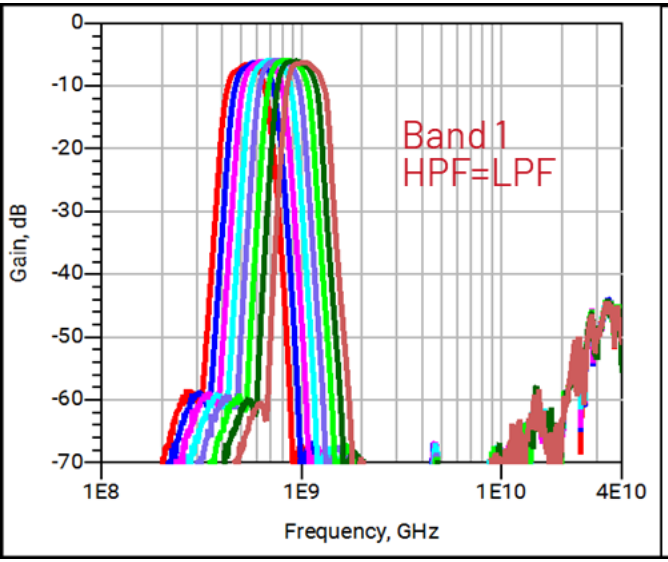
Each HPF/LPF have 8 states

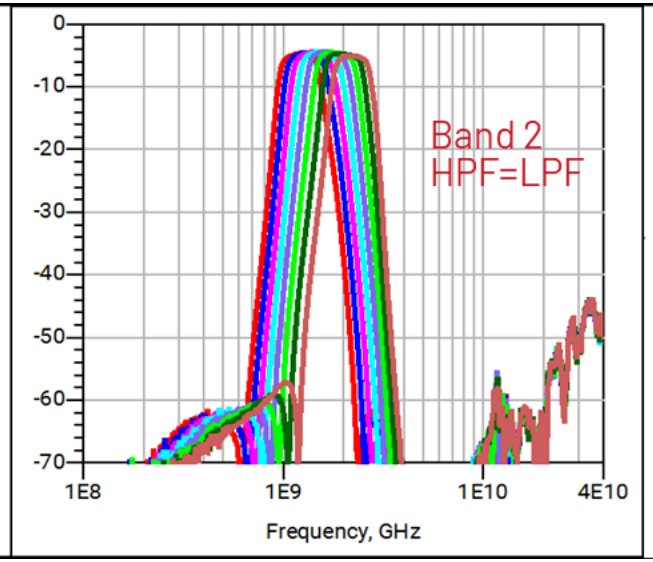
HPF=LPF States, i.e. Sub-Octave Bands shown below

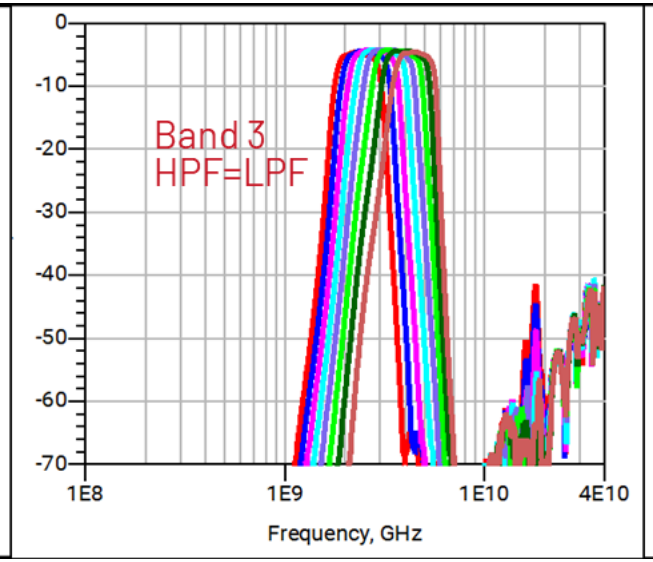
>50dBc re-entry up to 18GHz

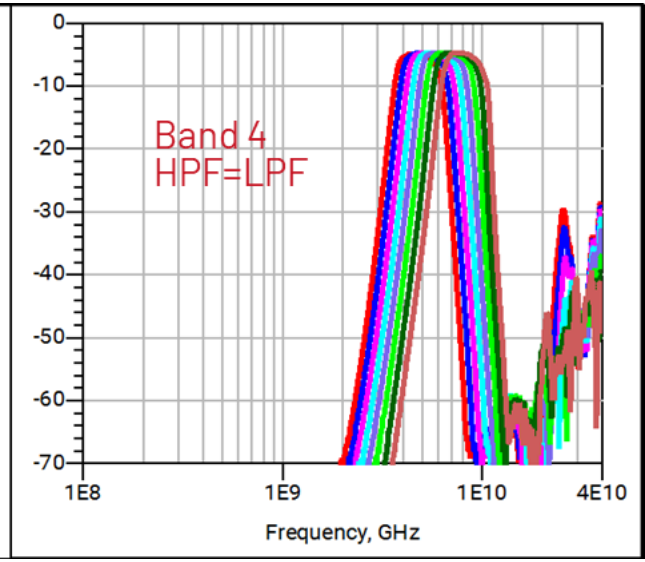




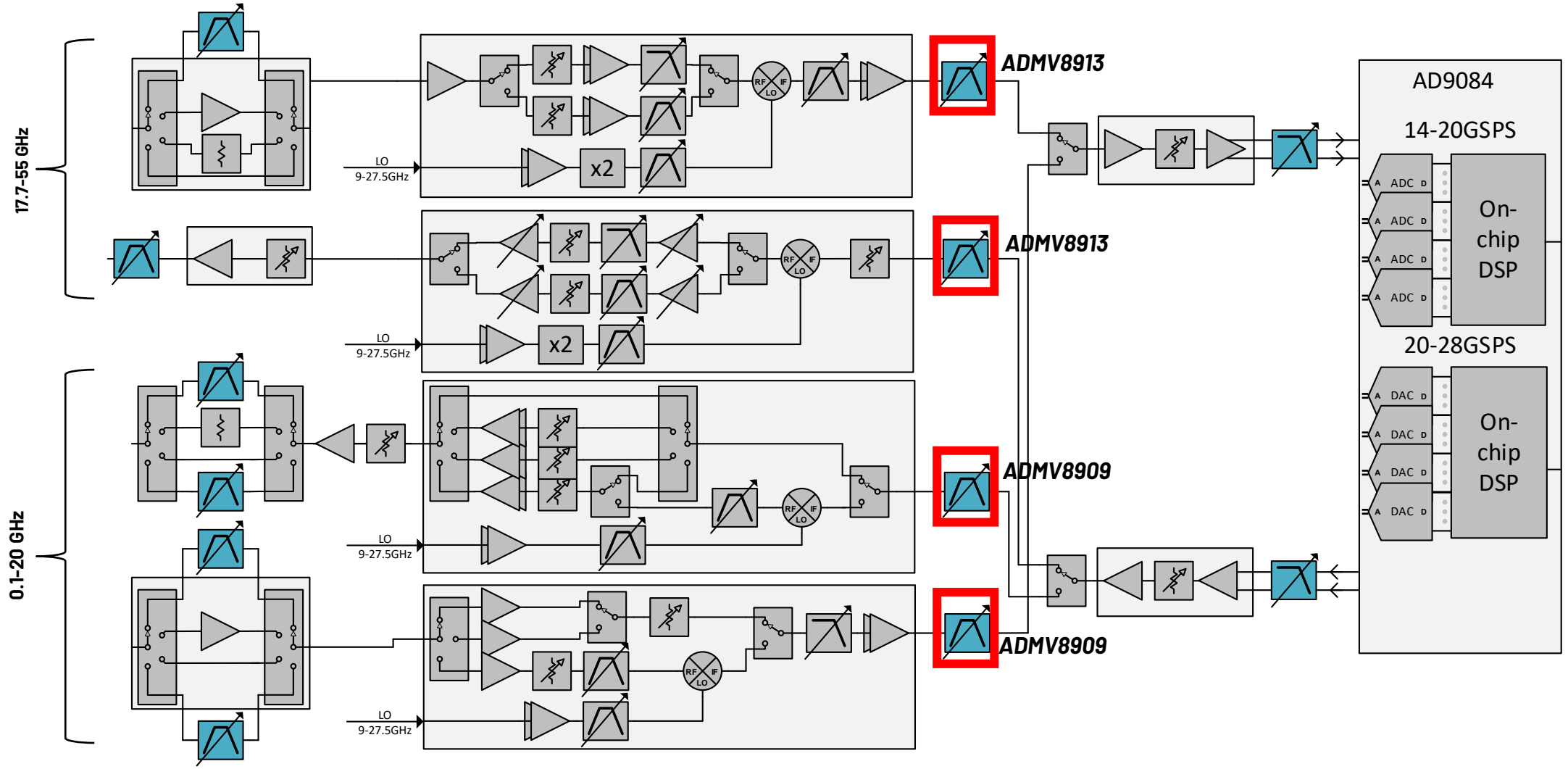








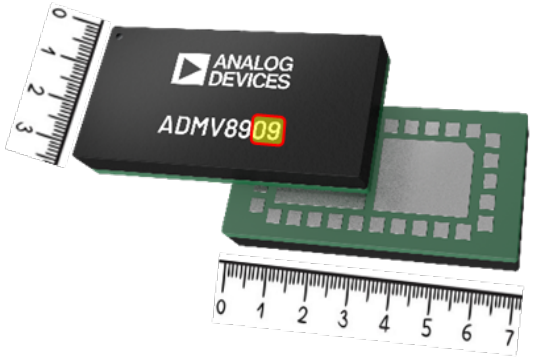
IF Filters:ADMV89XX

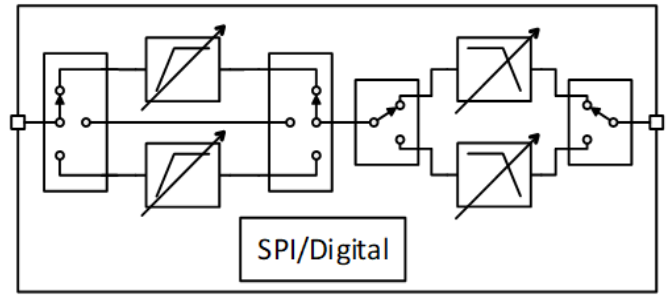


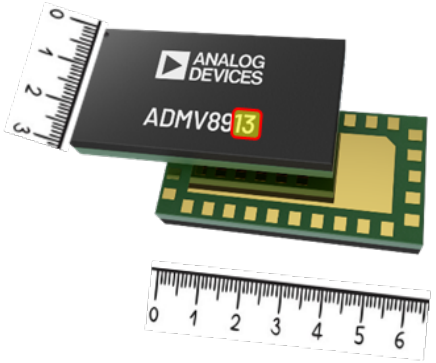
IF Filters Complementary to Frontend Filters

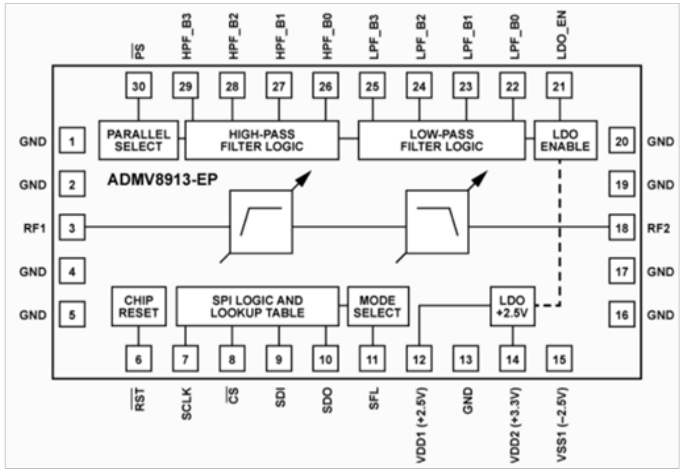
Key Features of ADMV89XX filters:

- **Image, Alias, LO & Spurious Rejection**
- ADMV89**09** for **DC to 9GHz** and ADMV89**13** for **7-13GHz**
- Typical 500ns switching time
- High Linearity, IIP3 typically around 45dBm
- 2 parts with same footprint for interchangeability
- Shield or cover NOT needed
- SPI interface with external address pins for multiple devices on the same SPI bus
- Parallel interface for all 8 control bits
- Space qualified and extended temperature range









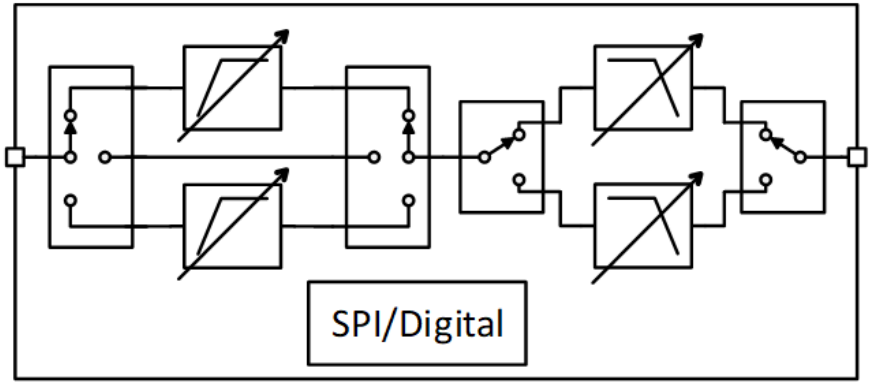
ADMV8909: Tunable DC-9GHz

1st Stage (HPF) : **Through** or **High Pass Filter** adjustable from **2GHz to 5GHz**

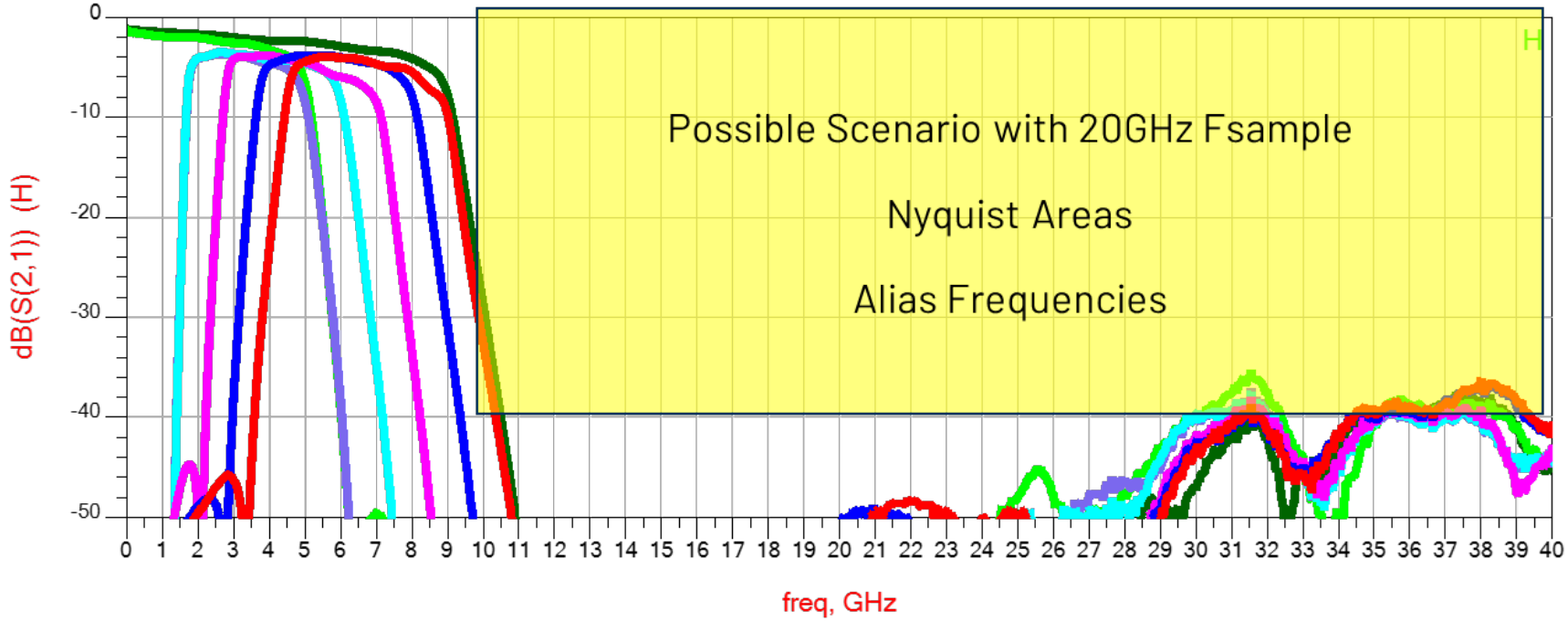
2 bits for SP3T and 2 bits for the HPFs (1+2x2^2= **9 states**)

2nd Stage (LPF): **Low Pass Filter** adjustable from **5GHz to 9GHz**

1 bit for SP2T and 3 bits for the LPFs (2x2^3= **16 states**)



Any combination of Through, HPF and LPF is possible



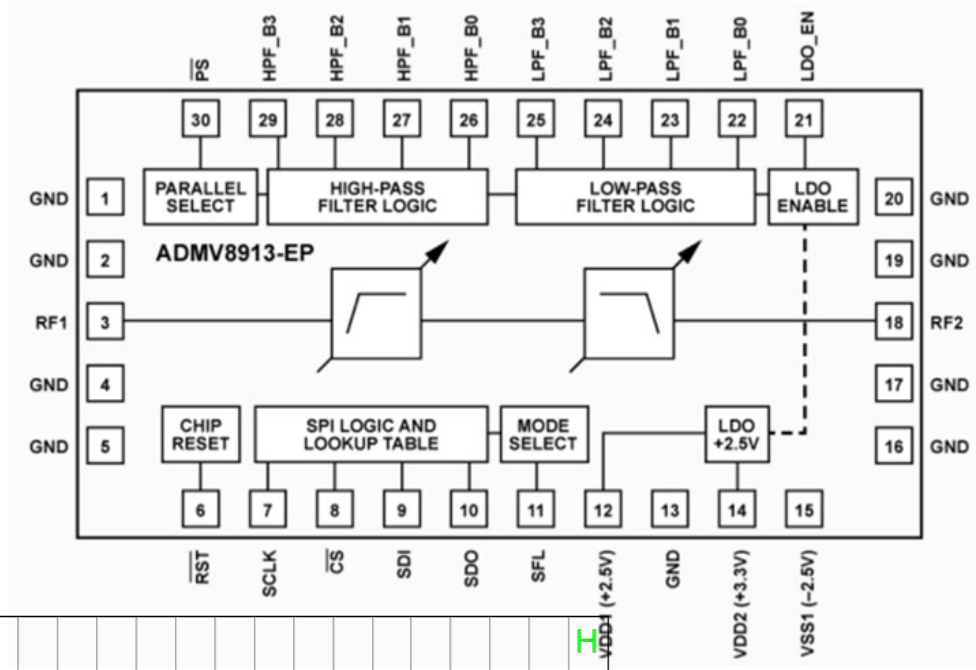
ADMV8913: Tunable 7-13GHz

1st Stage (HPF): **High Pass Filter** adjustable from **7GHz to 12GHz**

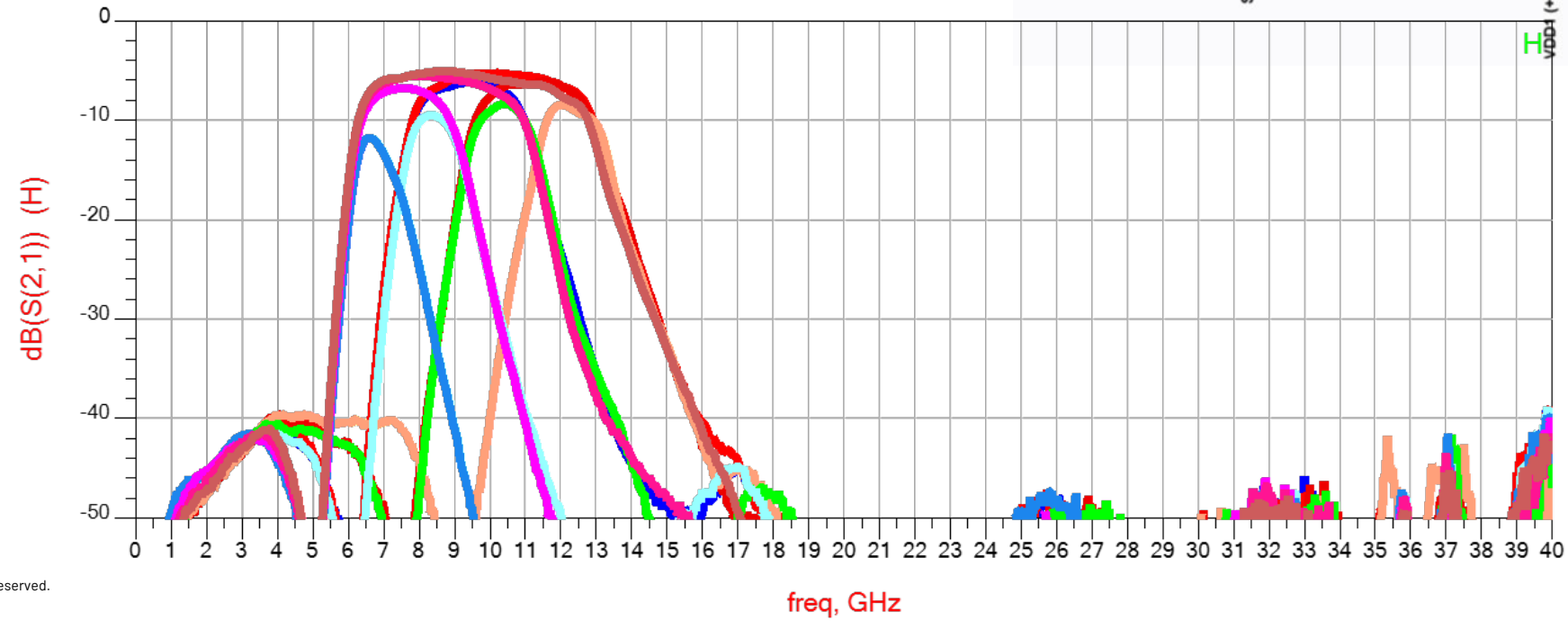
4 bits **16 states** for the HPF

2nd Stage (LPF): LPF adjustable from **7GHz to 13GHz**

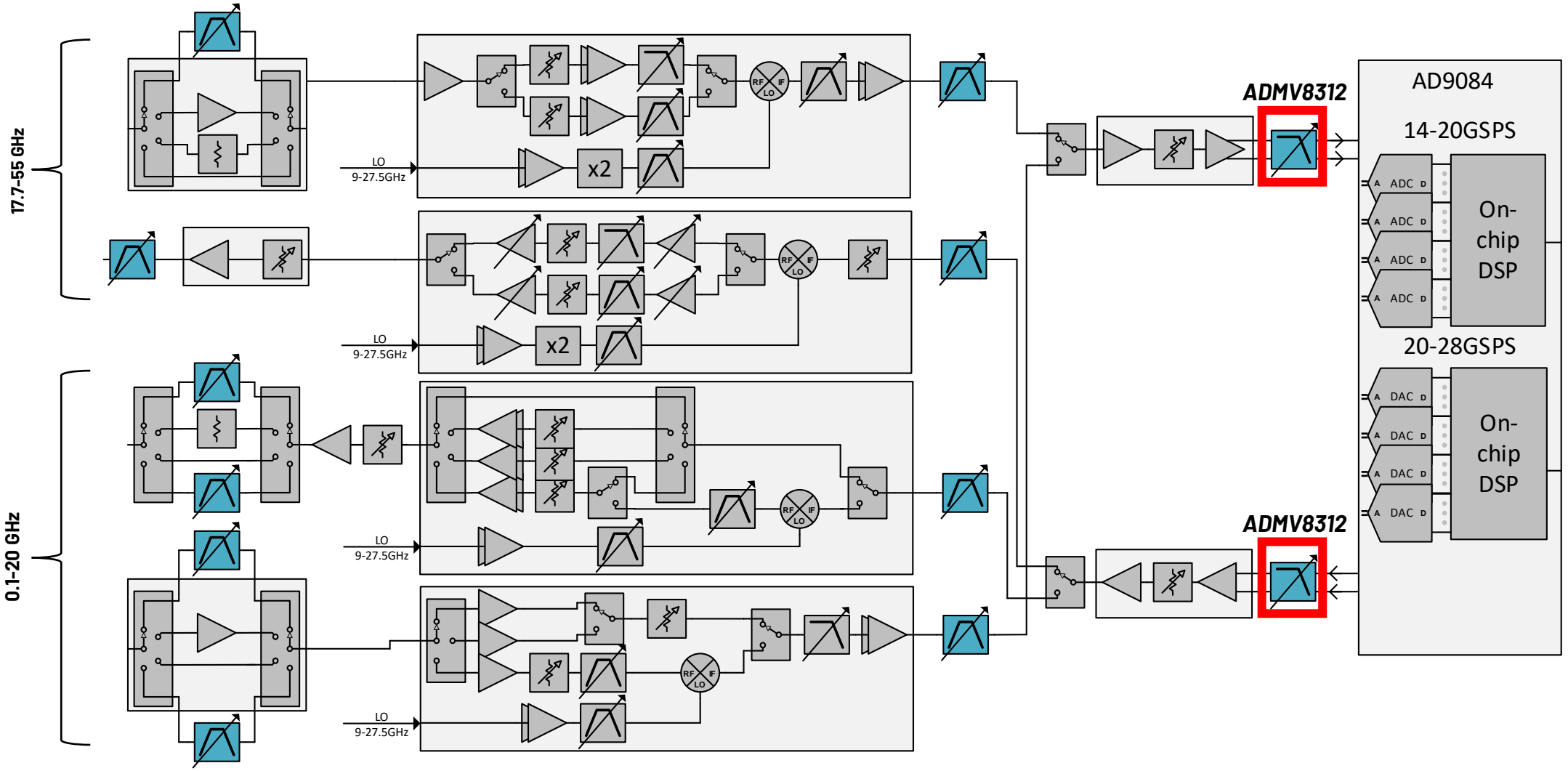
4 bits **16 states** for the LPF



10 combinations out of a possible 2^8 combinations:

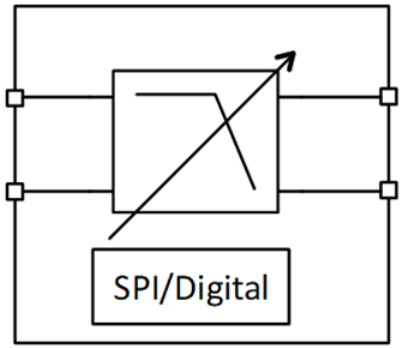


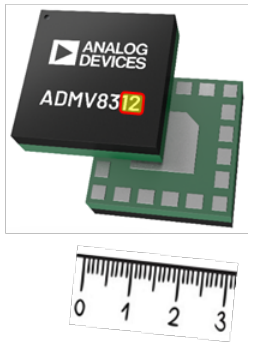
DAC/ADC Interface Tunable Low Pass Filter : ADMV83XX

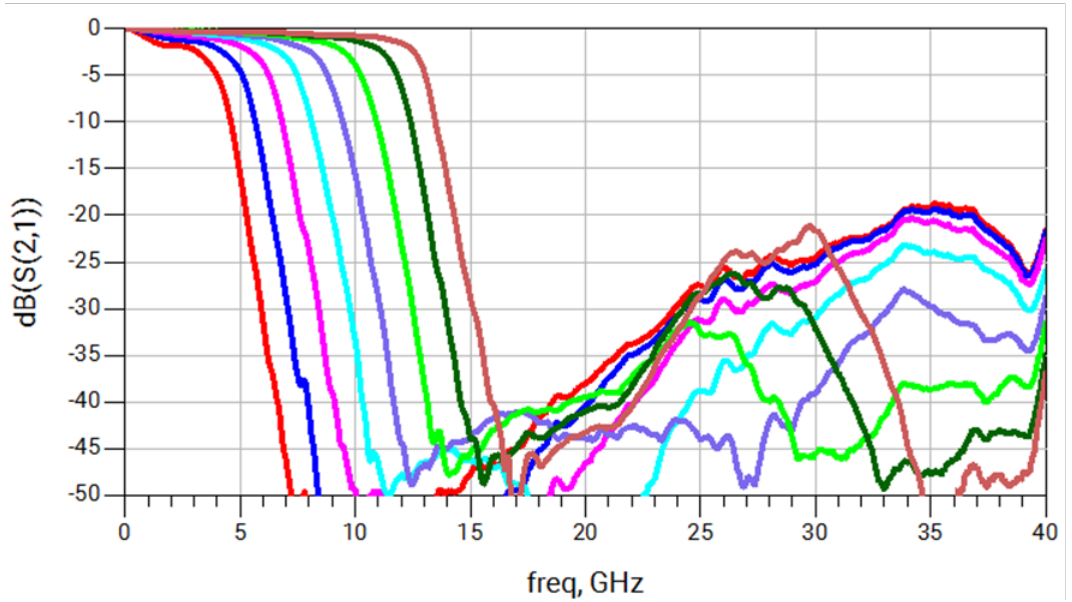


Tunable Differential LPF – Alias/Noise Suppression

- **Key Features of ADMV83xx filter(s) :**
  - ADMV83**12** Corner tunes from **4 to 12 GHz with 8 states**
  - Reject **Alias Signal/Noise in Rx** or **DAC Spurs in Tx**
  - **Very small footprint**
  - **Differential RF Ports.** Matches ADI Apollo Diff-50 Ohm
  - SPI interface for corner frequency setting
  - External 2 address pins enable multiple devices on the same SPI bus
  - **Parallel interface** for faster or simpler control
  - Space qualified and extended temperature range







Digitizer Sub-system

Problem statement - Digitizer

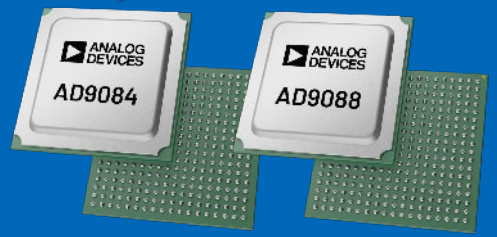
Next-generation RF systems need converters that combine high bandwidth, high dynamic range, on-chip DSP, and deterministic timing.

Challenges:

- Capturing GHz-wide signals under high blocker conditions
- DSP processing in RF systems consumes high power – offload FPGA with integrated DSP
- Signal conditioning using DSP techniques
- Achieving multi-chip coherence and fast reconfiguration

Apollo MxFE® – 4T4R and 8T8R

Released



4 Channel 20GSPS Rx, 28GSPS Tx

8 Channel 8GSPS Rx, 16GSPS Tx

RF Bandwidth: DC to 18GHz

Frequency Agile across L,S,C, X, Ku-Band

- Up to 10GHz iBW per channel in Full Bandwidth (2T2R)

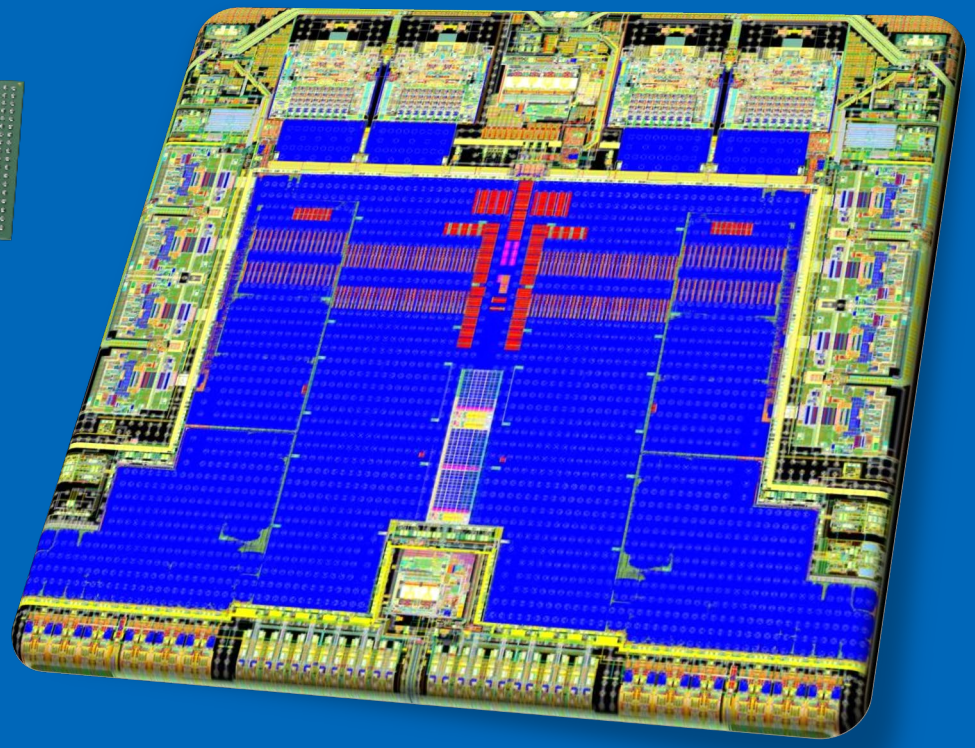
Programmable & Dynamically Reconfigurable DSP

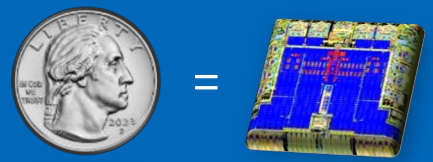
- Coarse & Fine Decimation / Interpolation 1x-1536x
- Coarse & Fine Independent FFH NCOs

Offload FPGA Compute from Fabric to ASIC

- FFT Sniffer, PFILT, CFIR, FSRC

Integrated Balun 50 Ω Single-Ended Input





Apollo MxFE™ Capabilities – Beyond Sample Rate

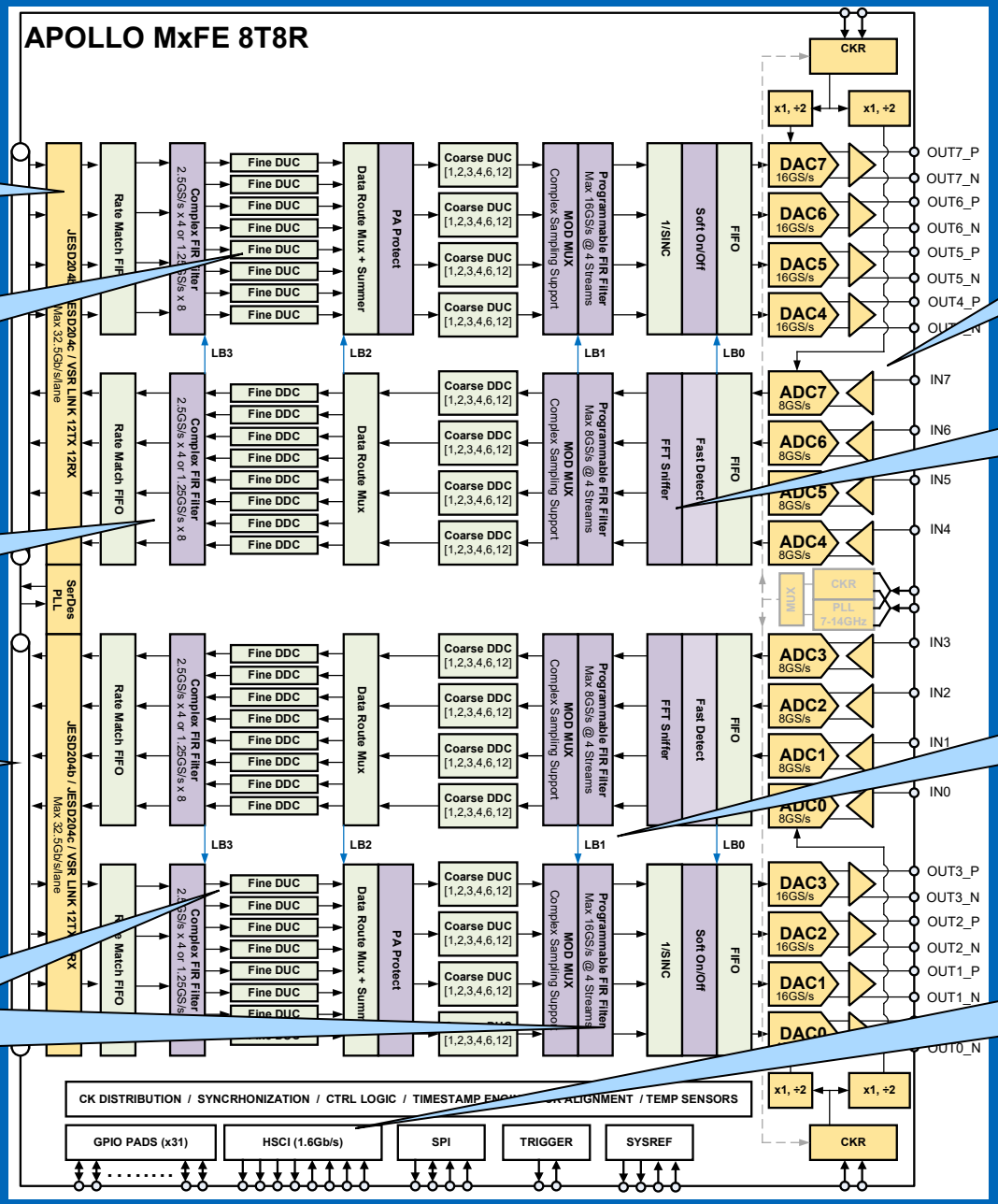
SERDES
24 lanes @ 27.8Gbps provide 780Gbps payload; VSR & JESD support

Integrated DDC/DUC
On chip decimation & interpolation from 1x-1,536x, with fast hopping NCOs

FSRC (4T4R only)
Decimate/interpolate by 1x-2x with 64b fractional word support

Dynamic Re-Config
Low latency, coherent modification of on chip DDC/DUC supported

Programmable Filters
Full rate PFILT and IQ rate CFIR integrated; user programmable coefficients



Single Ended Rx
50Ω input, single ended connects more easily to RF front end (differential variant also available)

FFT Sniffer
512 point FFT based sniffer on chip for full Nyquist signal monitoring

Loopbacks
Low latency loopback from Rx to Tx with embedded DSP in loop

HSCI
High speed control interface for rapid device reconfiguration

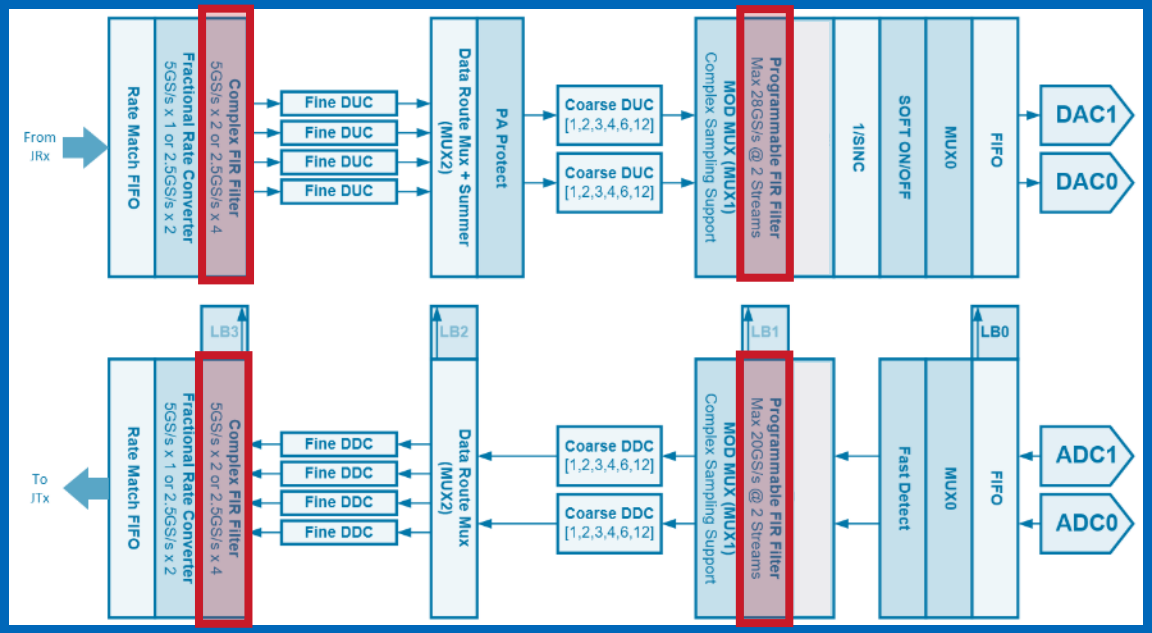
Versatile Signal Conditioning using On-chip digital filtering

#1 : Equalization of analog gain/phase impair ments over frequency

#2: Crosstalk correction with matrix compensation filtering

#3: Quadrature error correction with half complex filtering

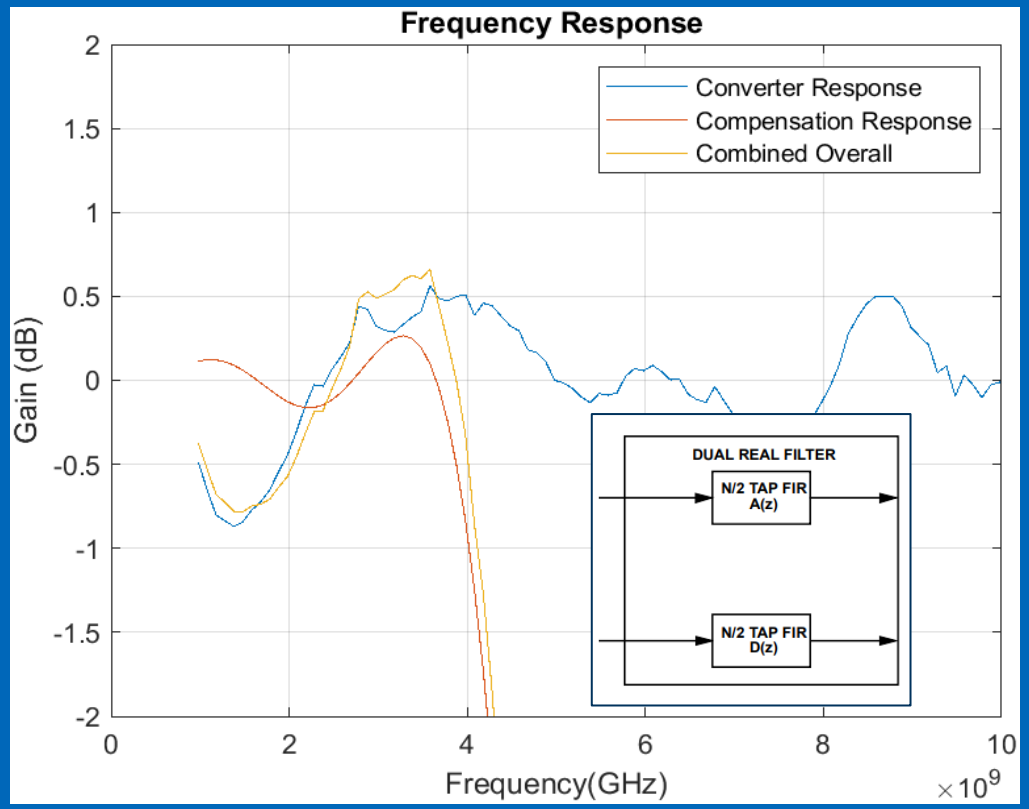
#4: Channel averaging for **3dB/Hz NSD improvement**

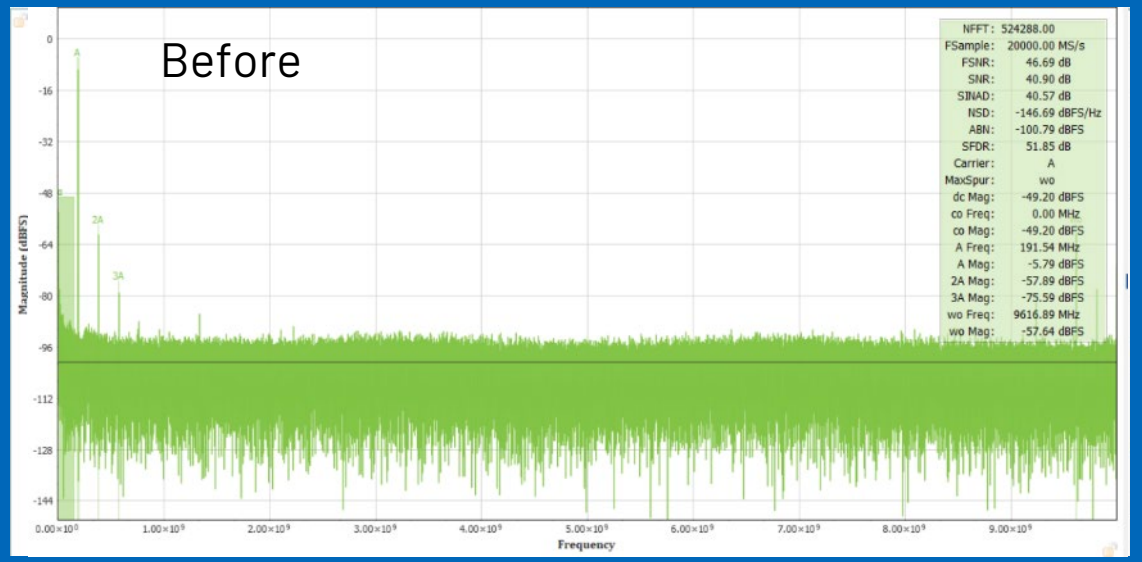


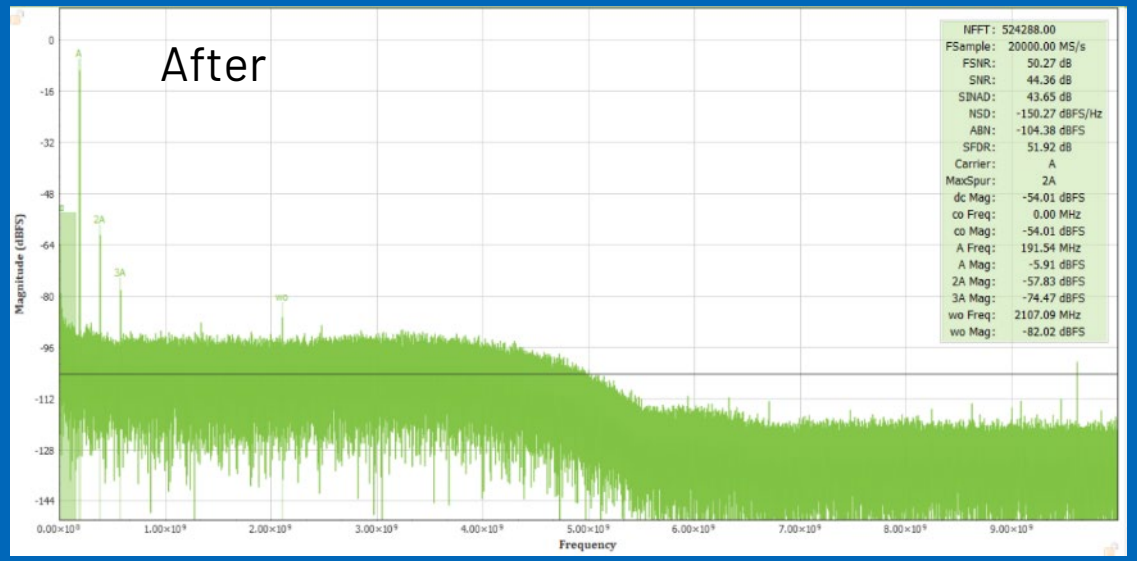
- CFIR performs fine per channel equalization at baseband rate
  - 16 taps per channel
  - Max 2.5Gsps each for 2 fine channels or 5Gsps for a single fine channel (AD9084)
- PFILT performs coarse filtering at converter sampling rate
  - 32 total taps
  - 5 available configurations
  - Max 28Gsps for each of 2 streams

PFILT : Equalization Example (Rx)

- Design coefficients in Matlab based on ADC measurement to apply desired compensation response (equalization, HPF, BPF, etc)

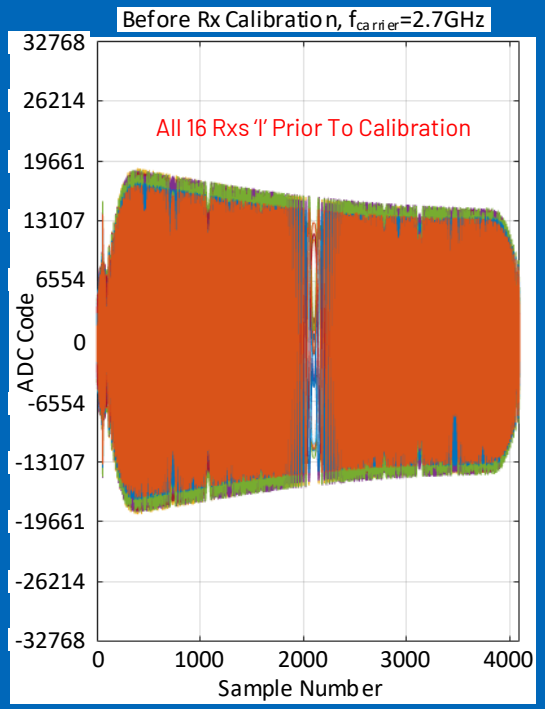




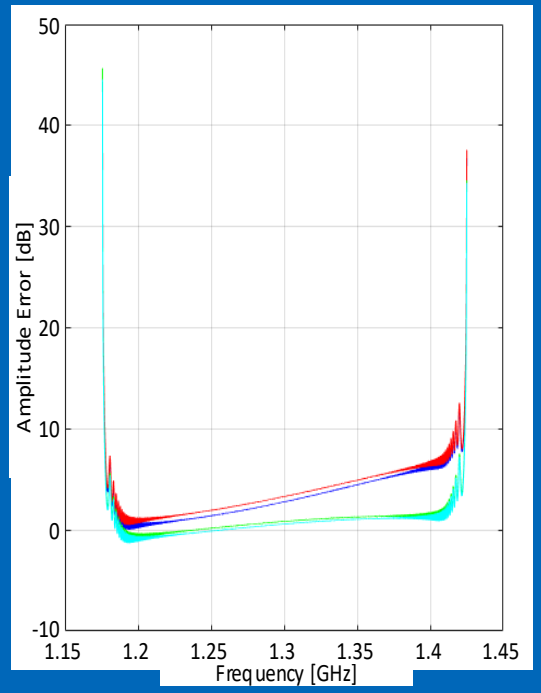


Hardened PFILT/CFIRs Correct Amplitude/Phase

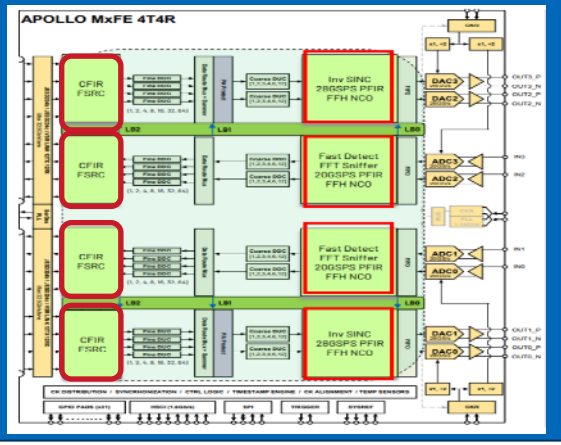
PFIR/CFIR Filters In Hardened DSP

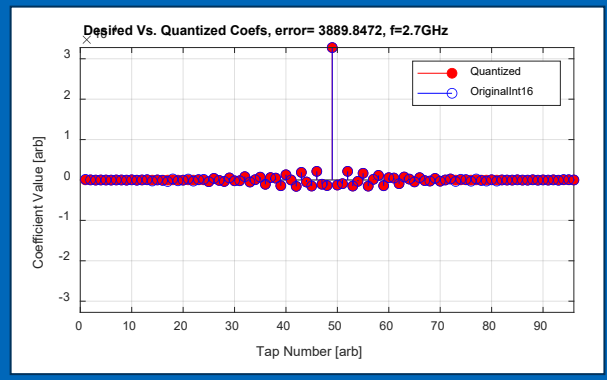


- Capture a receive path

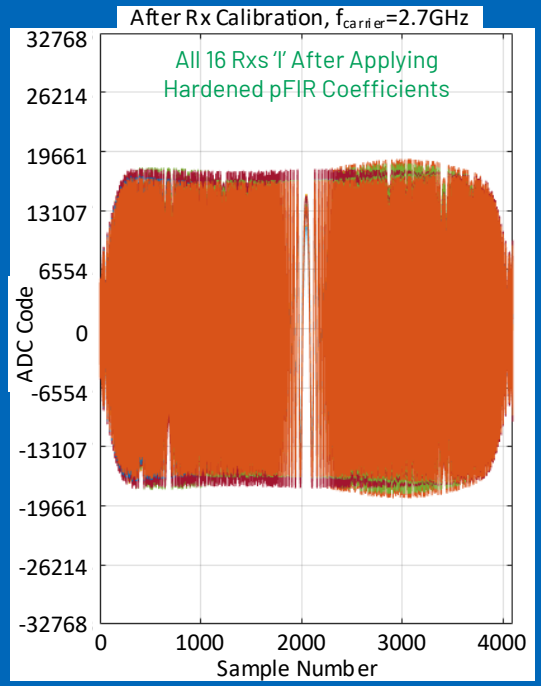


- Compute frequency-dependent error
  - Magnitude
  - Phase





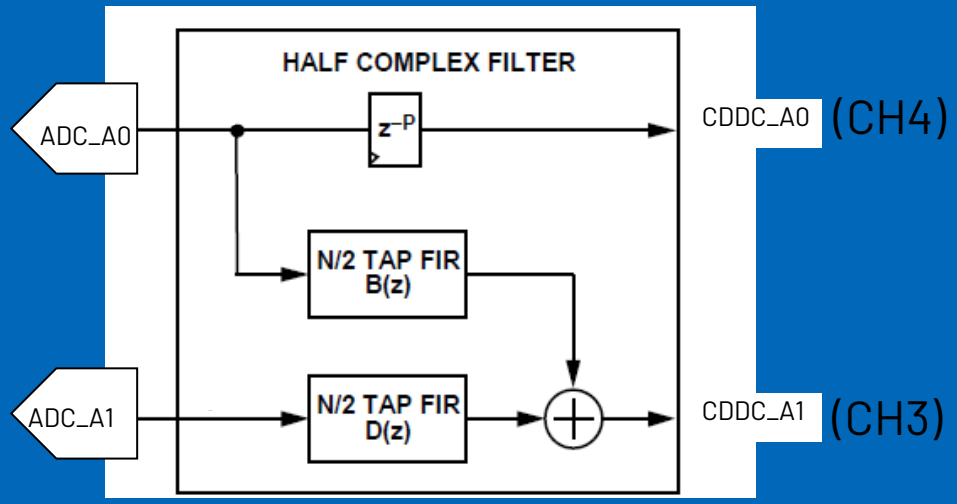
- Design hardened PFIR/CFIR coefficients for each channel
- Load coefficients into Apollo

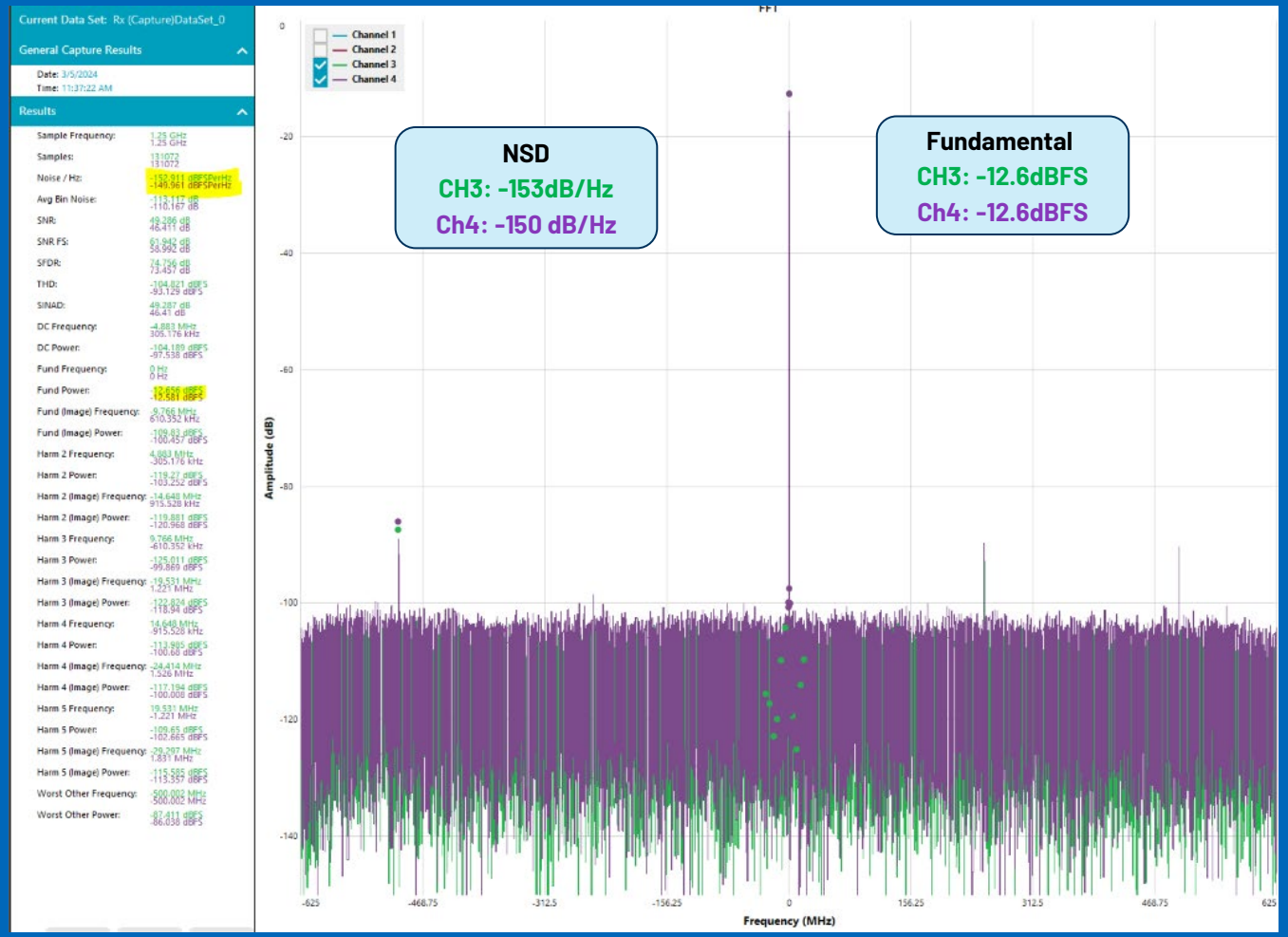


- Recapture receive path
- Observe calibration
  - Amplitude
  - Phase

Channel Averaging: NSD improvement by 3dB

- ADCs sampling rate : 20Gsps; decimation by 16 => 1.25GHz iBW
- Two ADCs per side capture same Ain
- Programmable filter combines two ADC outputs (Channel 3, green) into CDDC_A1
- Ain is passed through CDDC_A0 (Channel4, pink) for comparison





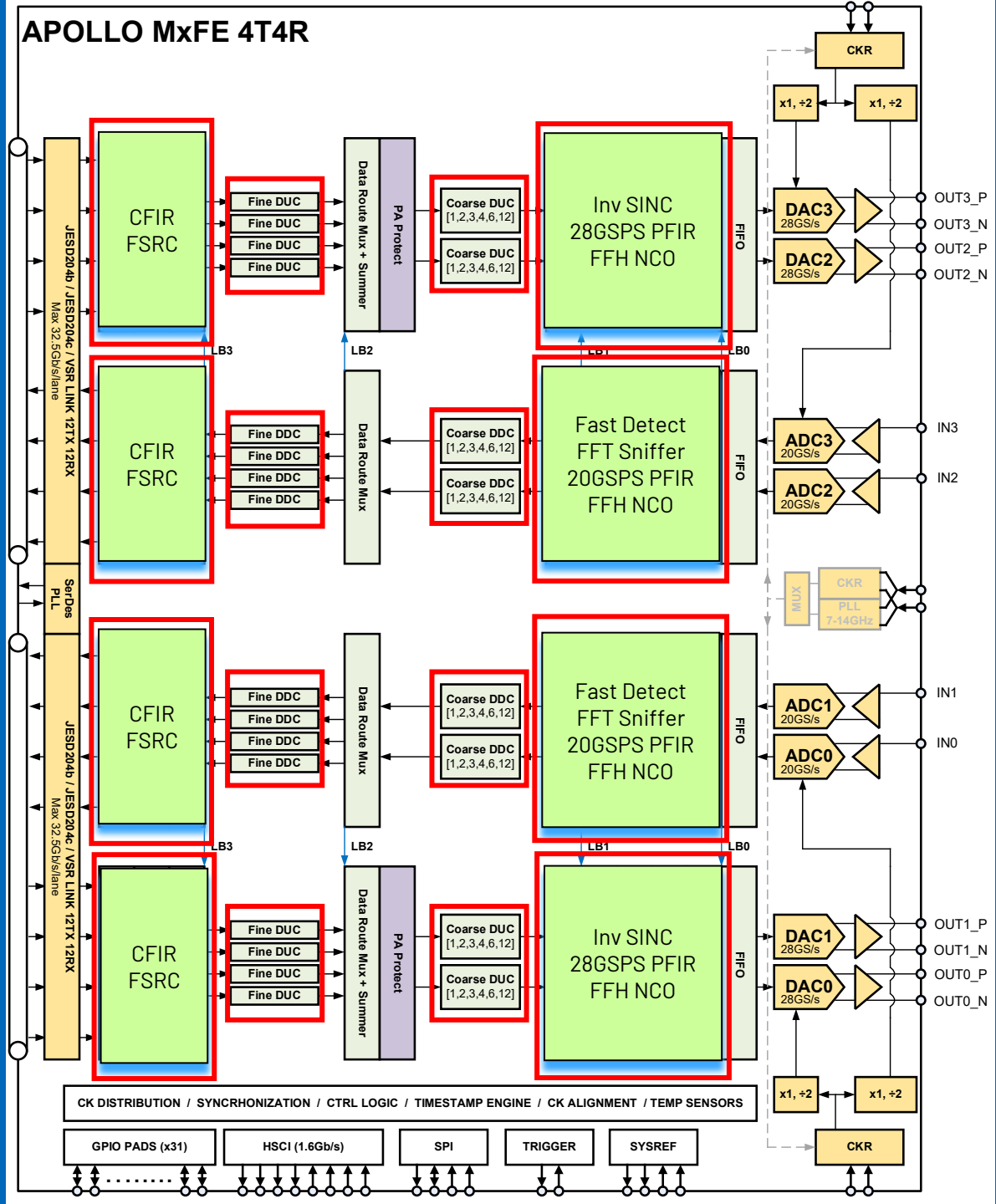
Dynamic DSP Reconfiguration

Datapath reconfiguration of CDDC/CDUC, FDDC/FDUC, PFILT/CFIR and FSRC Blocks

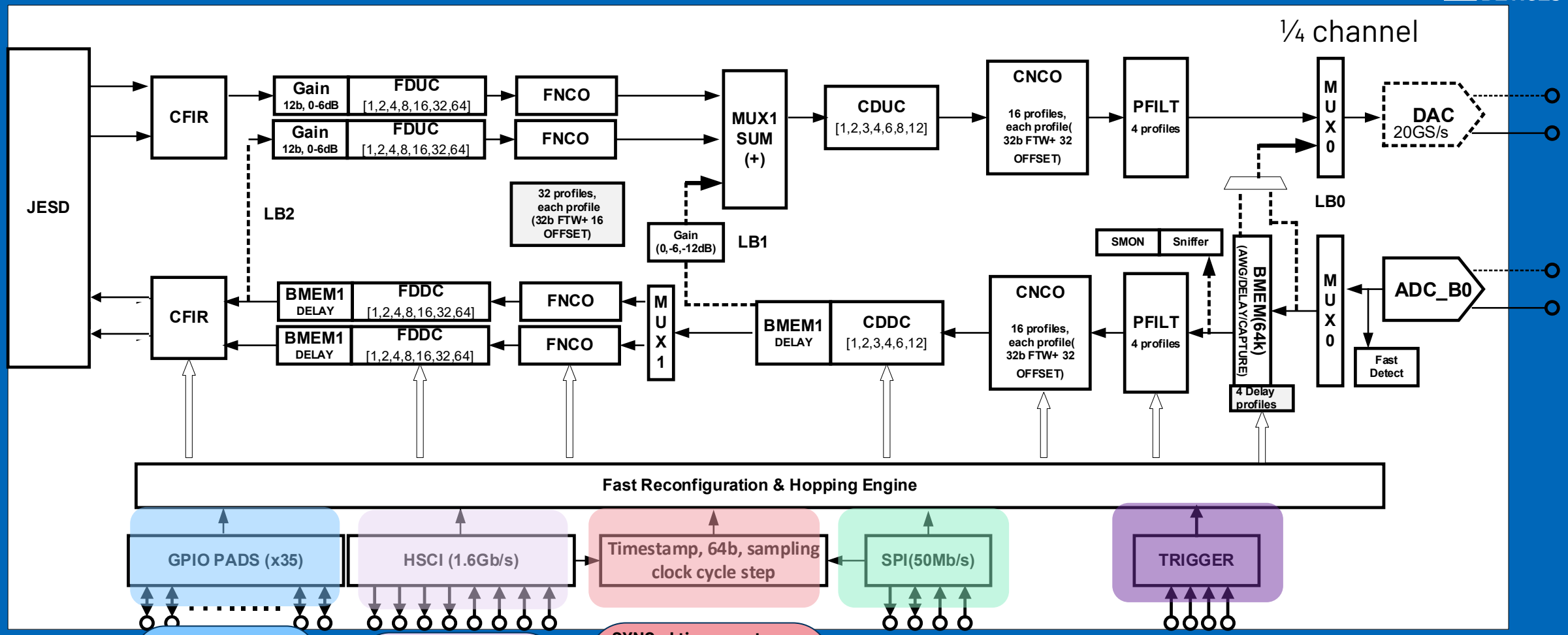
Phase Coherency and Deterministic Latency maintained via Subclass 1

JESD Link remains enabled with Rate Match FIFO

Reconfigured on internal or external trigger – configured in device profile or using API



Apollo MxFE® Fast Reconfiguration & Hopping



35 GPIOs, (Channel, function, profile selections)

Low latency

4 DIFF LVDS pairs

1.6G/s read & write speed

All user registers accessible

Low latency

SYNCed time counters across multiple chips for automatic hopping with preloaded profiles

Step size: sampling clock cycle. i.e. 50ps at 20GS/s

Zero interface latency

Standard SPI up to 50Mb/s

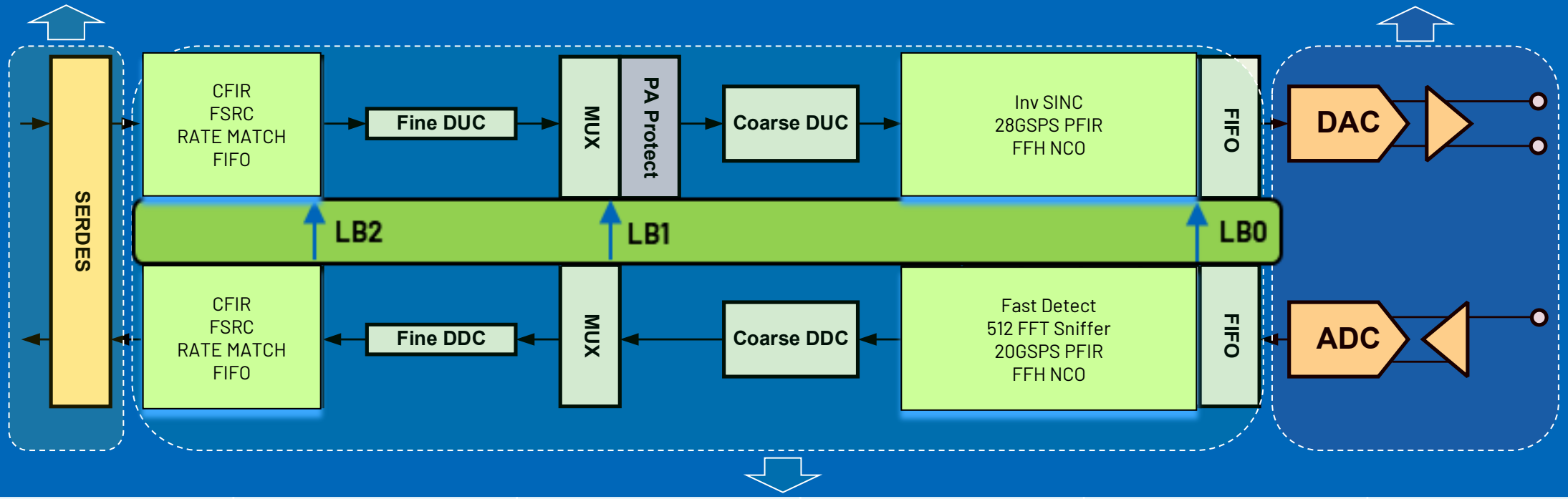
SYNCed hopping and reconfiguration across multiple chips

Programable retimed clock for ultra low latency

Apollo MxFE® – Dynamic DSP Reconfiguration

SERDES: Init at max required lane rate, will bit repeat as required after reconfiguration

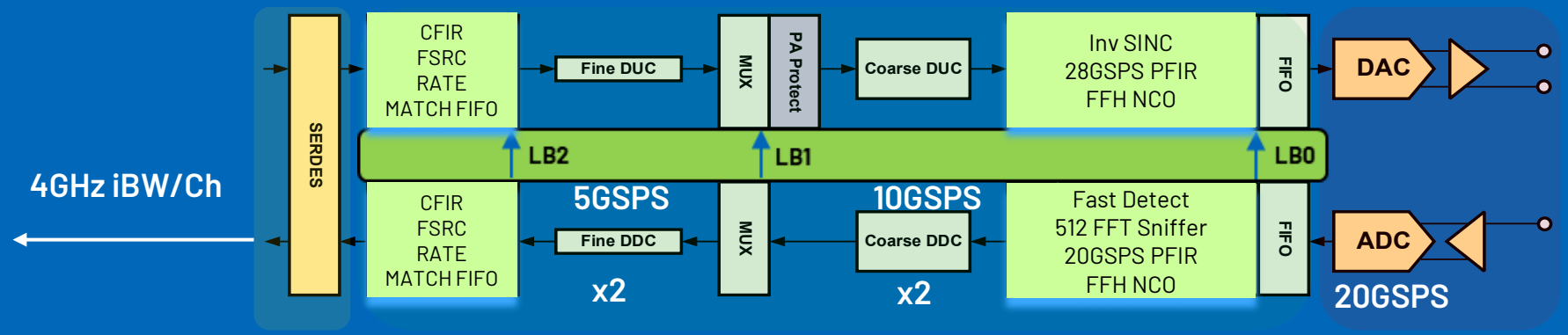
ADC / DAC Fs: Cannot be changed during operation



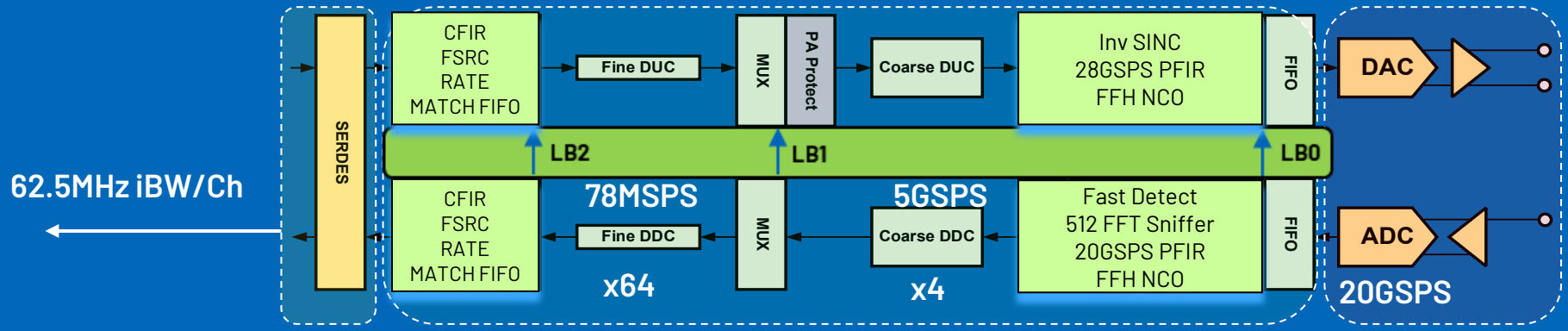
DSP Block:	FSRC	CFIR	FDUC / FDDC	CDUC / CDDC	PFILT
Dynamic Reconfig Allowed in Block	Int / Dec 1.0 – 1.99	128 Taps Two sets of coefficients	Int / Dec, NCO Freq (1,2,4,8,16,32,64)	Int / Dec, NCO Freq (1,2,3,4,6,12)	32 Taps Four sets of coefficients
Reconfig Time @ Fs = 20GSPS	<1us for reconfiguration with decimation/interpolation ≤128 <5us for reconfiguration with decimation/interpolation >128				

Apollo MxFE® – Wideband to Narrowband in 5µs

Wideband Profile: 20GSPS, CDDC = 2, FDDC = 2, iBW = 4GHz/Ch.



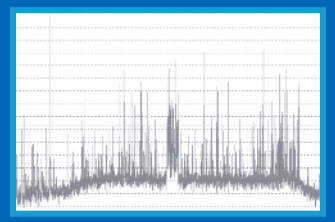
Narrowband Profile: 20GSPS, CDDC = 4, FDDC = 64, iBW = 62.5MHz/Ch.



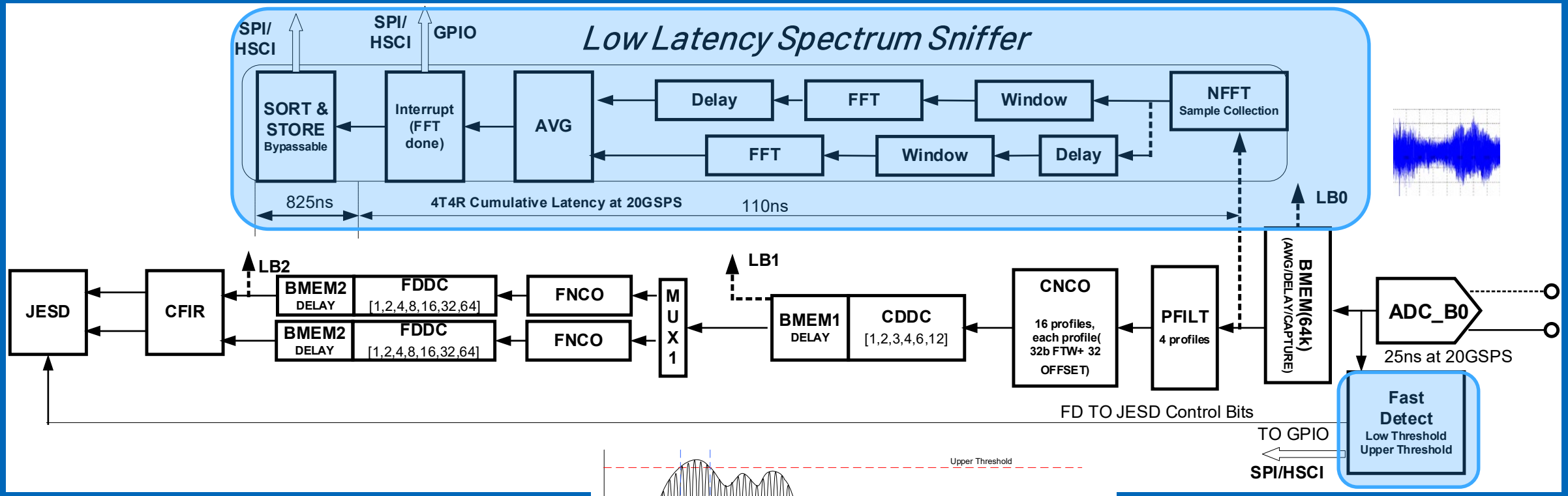
Dynamically reconfigure from 4GHz iBW/ch to 62.5MHz iBW/ch in ~ 5 µs without taking JESD link down

Background FFT Sniffer for Situational Awareness

Sort #	Bin #	RSSI
1	210	-12
2	450	-15
	...	
512	60	-40



Raw FFT



Apollo MxFE® Apollo Low Latency Loopbacks

SERDES

100-2.5k clock cycles (5n-125ns)

CFIR & FSRC

500-25k clock cycles

FDUC/FDDC

1-50k clock cycles

CDUC/CDDC

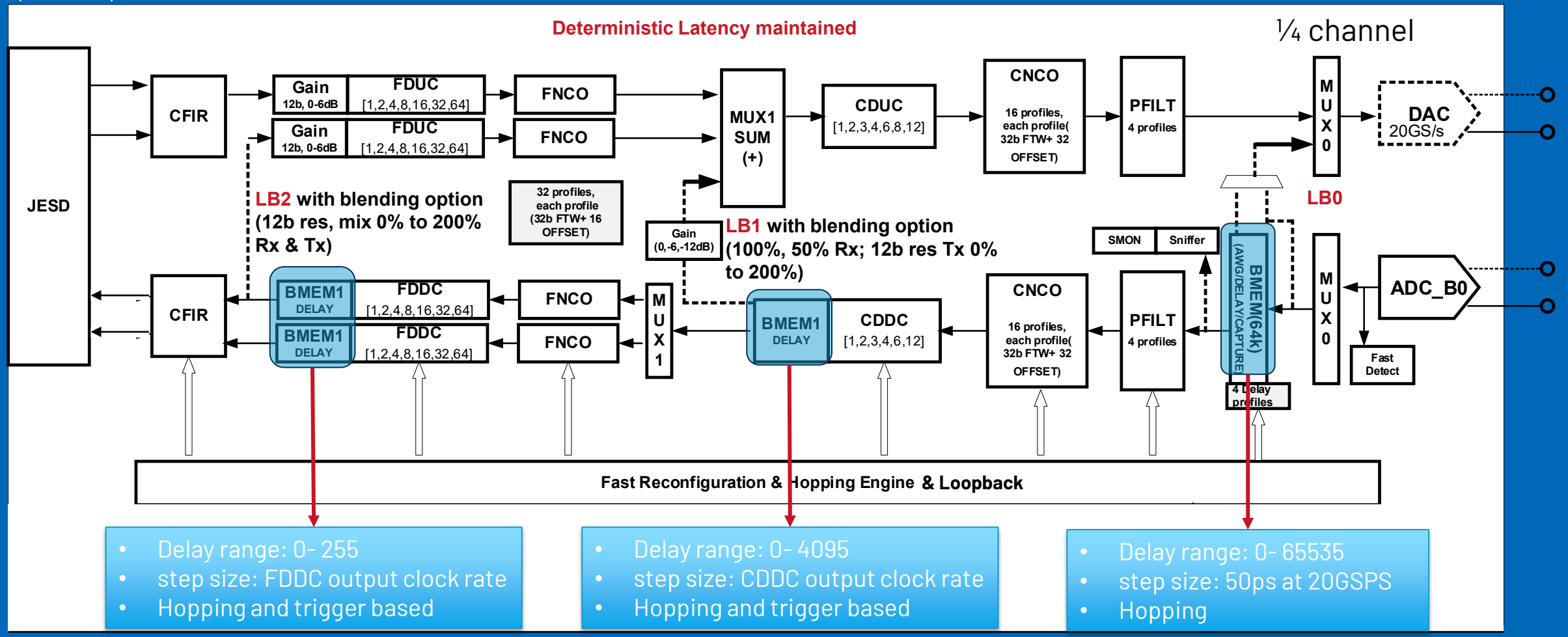
1-2k clock cycles

Full Rate DSP

1k-2k clock cycles

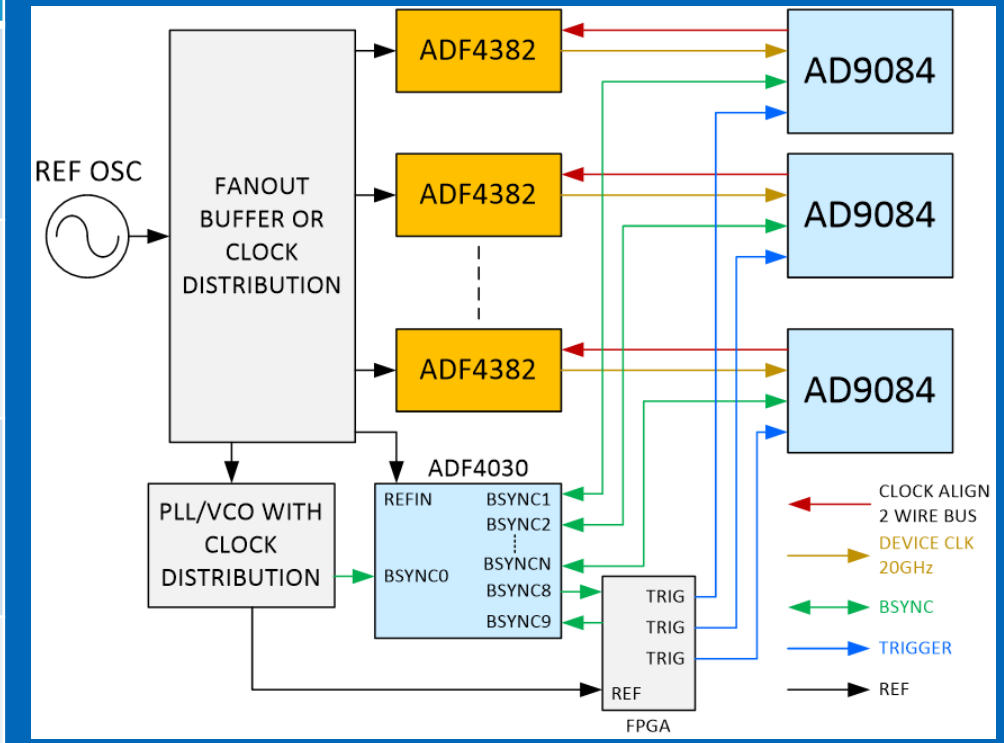
DAC/ADC

200/700 clock cycles (10ns + 40ns)

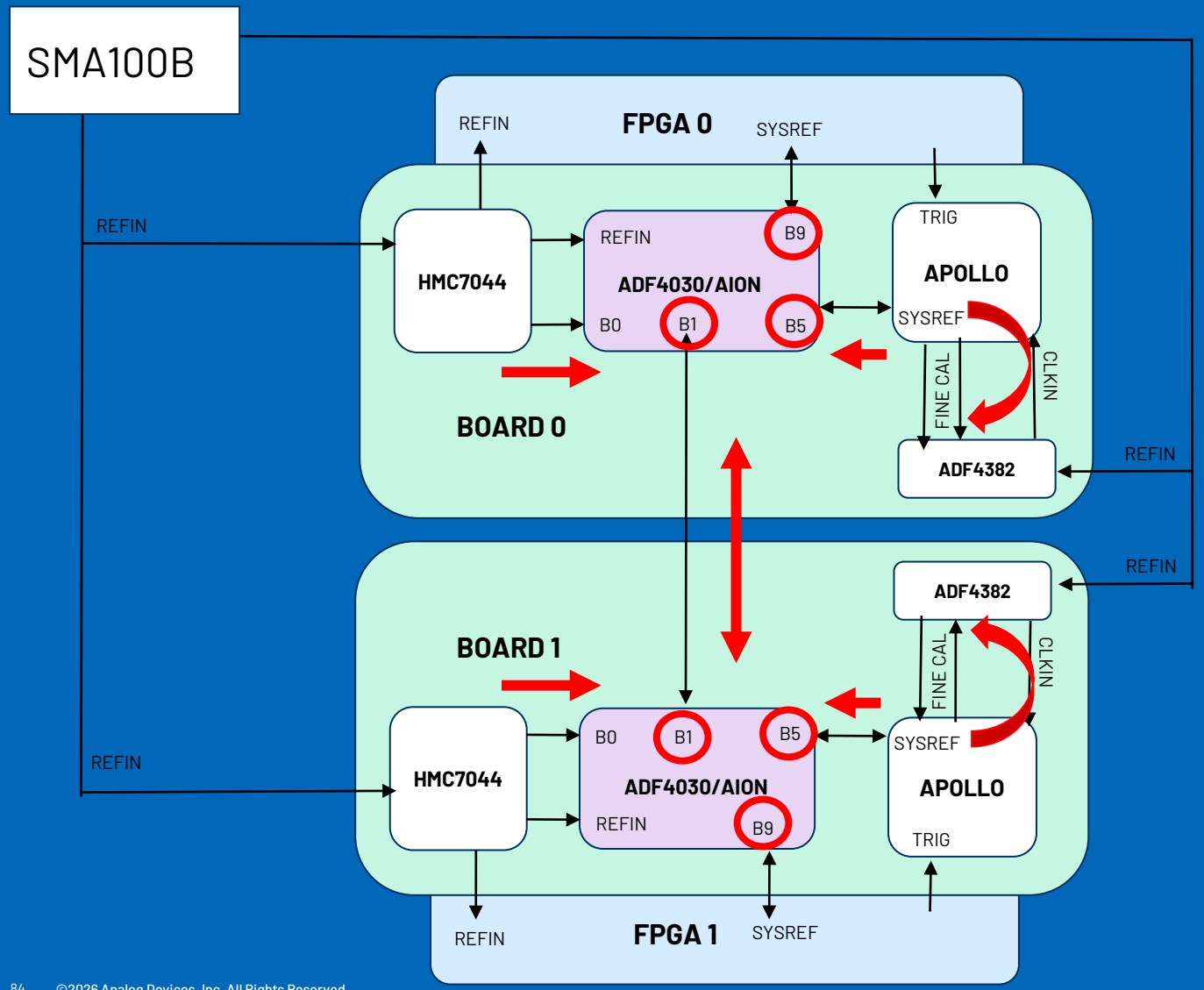


Multi-Chip Synchronization within 1ps

Component	Operation	Value
HMC7044	Fanout Buffer	➢ Ref lock Artemis, Aion, FPGA
ADF4382 (Artemis)	Provide ref clk to Apollo	➢ Receive delay information from Apollo ➢ ps delay capability to adjust Apollo clk
ADF4030 (Aion)	Provide SYSREF to Apollo(s) and FPGA	➢ Align ref BSYNC0 to BSYNCx <5ps ➢ TDCs calculate and null RT delays between chips
AD9084 (Apollo)	Internal sysref dictates JESD data release and converter transmit/capture for deterministic latency	➢ Shift internal sysref to align with ext sysref within dev clk / 2 (25ps at 20Gsps) ➢ TDC measurement strobed to Artemis to delay ref clk for <1ps int/ext sysref alignment



Multi-Chip Synchronization : <5ps alignment achieved



1. Align all Bx's with B0 per Aion
2. Determine round trip delay between the two Aions.
3. Apollos align to respective Aion through B5. Apollo sends TDC to ADF4382 to fine tune, then send tuned Sysref to B5
4. Aion determines round trip delay from Apollo. Applies any delay to specific Apollo.
5. Apollo internal Sysrefs are aligned

Wrap Up

Summary: 0.1–55 GHz Signal Chain Highlights

0.1-55 GHz is achievable – but only with hybrid architecture

- Direct Sampling + High-IF partitioning is key

System performance is SNDR/SFDR limited

- Blockers, IMD2/3, and filtering are critial

Consolidation of functions into integrated RFICs and SIPs is critical for size reduction

- Allows size reduction and optimized process selection by function (GaAs, CMOS, GaN)

Functional partitioning is critical to ensure design flexibility

- Tunable architecture enables design re-use as well as mission reconfiguration

Converters are critical part of the RF architecture

- DSP + fast reconfigure fundamentally change partitioning

Demos in action – Visit the ADI booth

See demos of these signal chains and related components on the show floor:

Title
2–18 GHz Signal Conditioning for Direct-Sampling Receivers
Seamless DC–18 GHz Coverage with Dual-Clock Direct RF
High-Density RF Digitizer SoM in a VNX+ Small Form Factor
X-Band Digital Beamforming Platform using High-Density Direct RF Sampling
Experiencing 6G Integrated Sensing & Communication with Dragonfly

AHEAD OF WHAT'S POSSIBLE

analog.com