



The Dynamic Duo – Software Defined Radio (SDR) & Software Defined Modem (SDM)

The Nevis SDR & SDM

- The Next Generation Narrowband, Software Defined Radio IC from Analog Devices.
 - Includes ADI's first ever integrated soft-modem
- Developed with engagement from leading LMR handset manufacturers
- Purpose Built to meet the needs of Critical Communications
 - *The Performance* to exceed TETRA, P25 and DMR requirements
 - *The Efficiency* to extend radio battery life
 - *The Capability* to integrate system functionality, streamline radio design and enable aggressive form factors
 - *The Flexibility* to support multi-waveform, multi-band operation and to platform an entire family of LMR handsets



The Nevis Product Family

- Supports radio platforms by offering a common package and pinout across variants
 - 196-ball, 10mm x 10mm CSP BGA pkg.
- Variants differ only in channel configuration and the availability of the Software Defined Modem
 - RF performance is equivalent across all variants
- Dual-Channel variants offer wideband Rx and Tx capabilities
- Supported by a Common Evaluation HW, GUI, SDK and API framework

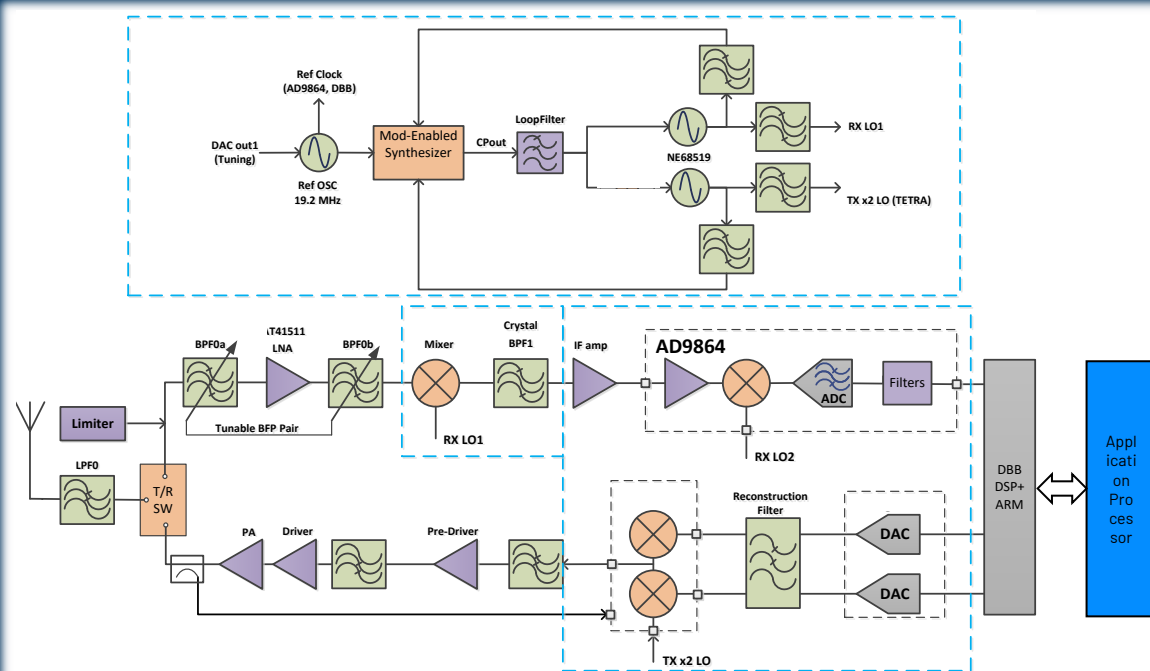


Feature	ADR9101	ADR9102	ADR9103	ADR9104
Channel Config	1T1R	1T2R	1T1R	1T2R
Tx iBW max	2 MHz	40 MHz	2 MHz	40 MHz
Rx2 iBW max	2 MHz	2 MHz	2 MHz	2 MHz
Rx1 iBW max	--	40 MHz	--	40 MHz
RF Range	70MHz ... 6GHz	70MHz ... 6GHz	70MHz ... 6GHz	70MHz ... 6GHz
Software Defined Modem	No	No	Yes	Yes
TRX Feature Set	Full	Full	Full	Full
External VCO Support	Yes	Yes	Yes	Yes
Flexible LO mapping	Yes	Yes	Yes	Yes



Nevis System Value – Integration, Size and Adaptability

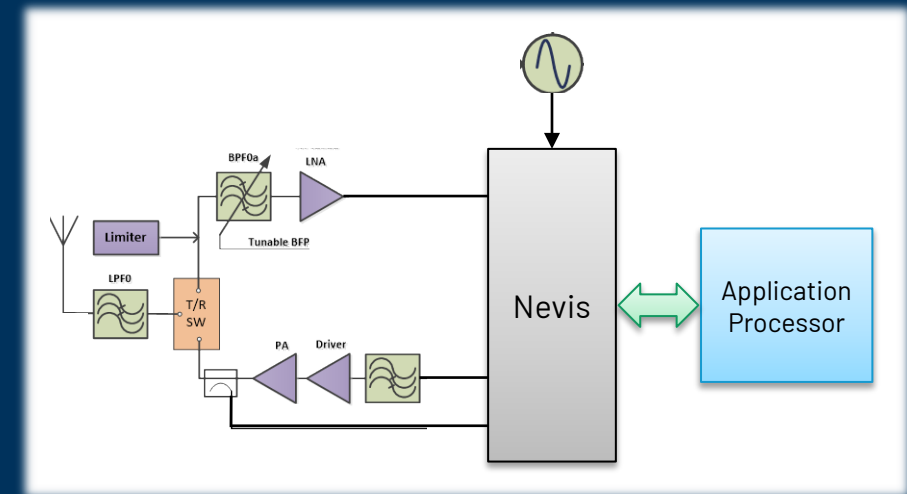
Typical TETRA System Diagram



- Traditional LMR system designs are inflexible, static and area intensive
 - Customers are exposed to greater risks of product obsolescence, due to the large component count
 - Discrete implementations require system level calibrations to maintain performance, consuming resources and time
 - Radio designs can be difficult to re-use across different waveforms and operating frequencies, increasing development effort on new products

**>1000mm²
Area
Reduction**

TETRA System Diagram with Nevis

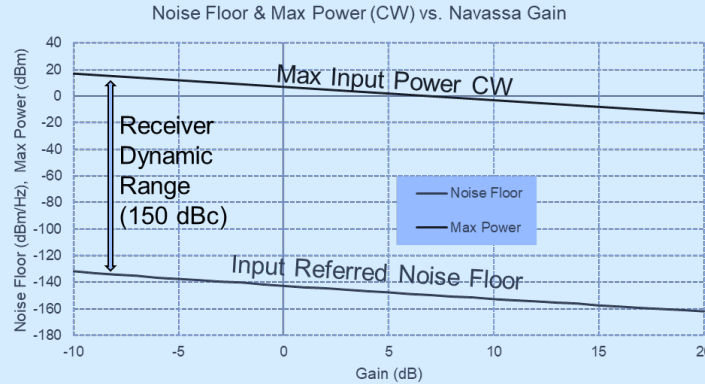


- A Nevis based approach addresses these issues:
 - Reduces BoM management and risk/exposure to obsolescence
 - ADI routinely supports products for >15yrs
 - Reduces board space
 - A single 10mm x 10mm Nevis integrates over 20 components!
 - Provided Digital Predistortion (DPD) eliminates need for Cartesian Feedback ICs
 - Integrated AuxDACs and AuxADCs can replace discretes
 - Integrated ARM subsystem (PS2) enables the use of lightweight external processors
 - Greatly increases design portability
 - New radio designs can be created for different markets/applications with minimal BoM changes and redesign effort
 - Real-time tracking calibrations maximize TRx performance across time, temperature, and operating conditions - without impacting radio operation

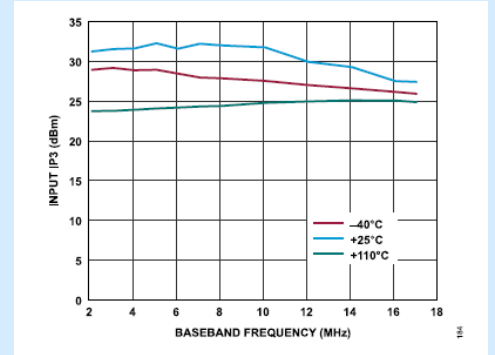
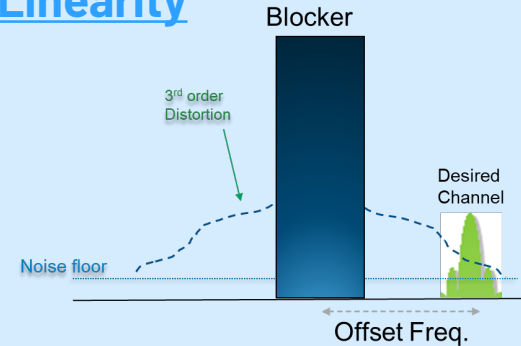
How Nevis Addresses the Blocking Challenge

Dynamic Range

- Large dynamic range (~**150dB/Hz**) enables the receiver to digitize both the blocker and desired signal
- The blocker can be filtered efficiently in the digital domain.
- Enabling flexibility by minimizing the need for external filtering.



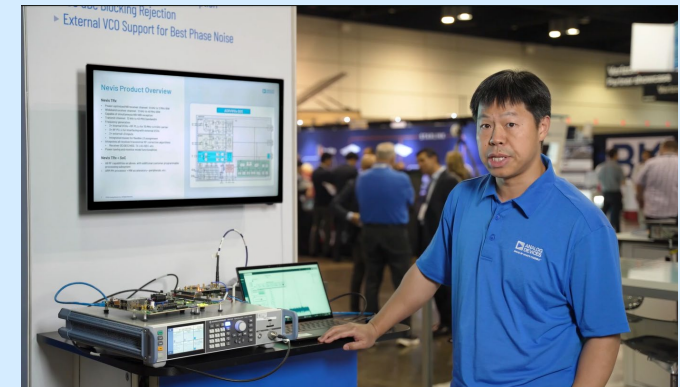
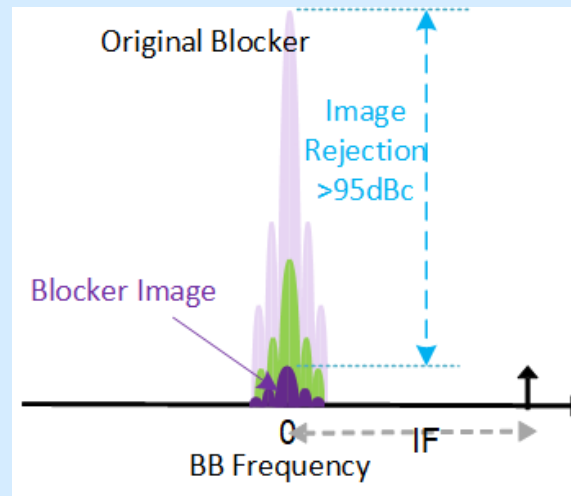
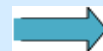
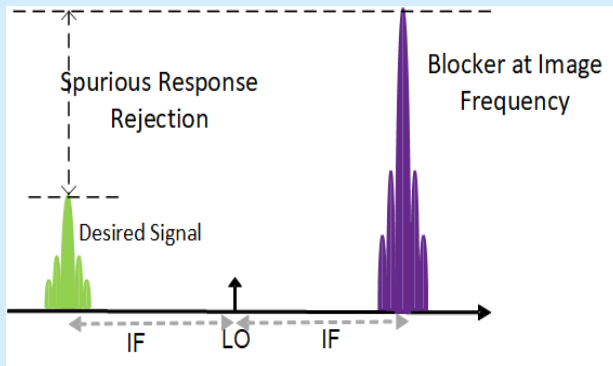
Linearity



- Intermodulation products are more than ~90 dB below large blockers

Image Rejection

- Image Rejection of ~ 95 dB ensures blocking signals do not reduce receiver sensitivity even if they land on images

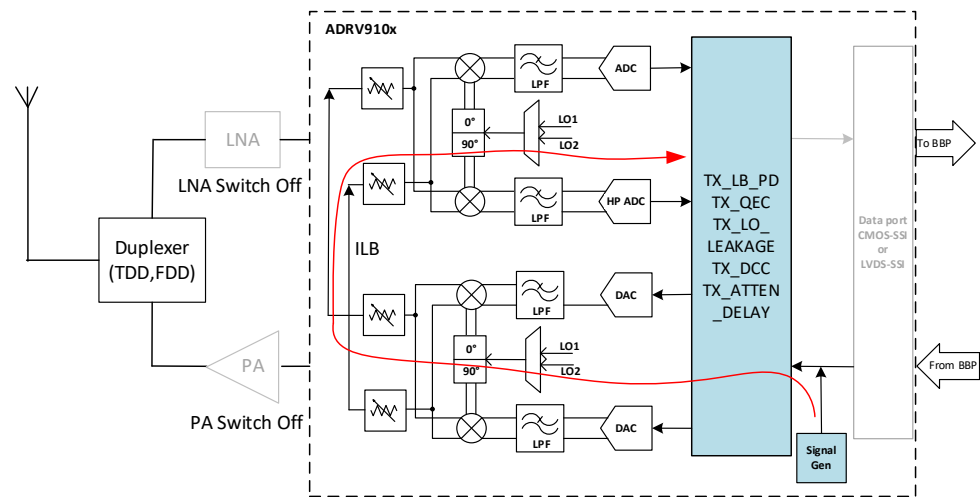


Video Demonstration of 100dBc blocker tolerance and Low Power operation

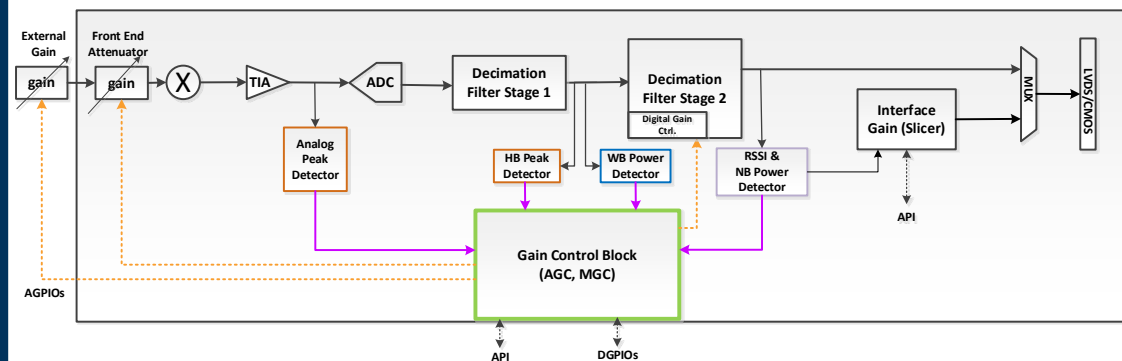
High Performance, Low Power, Narrow Band



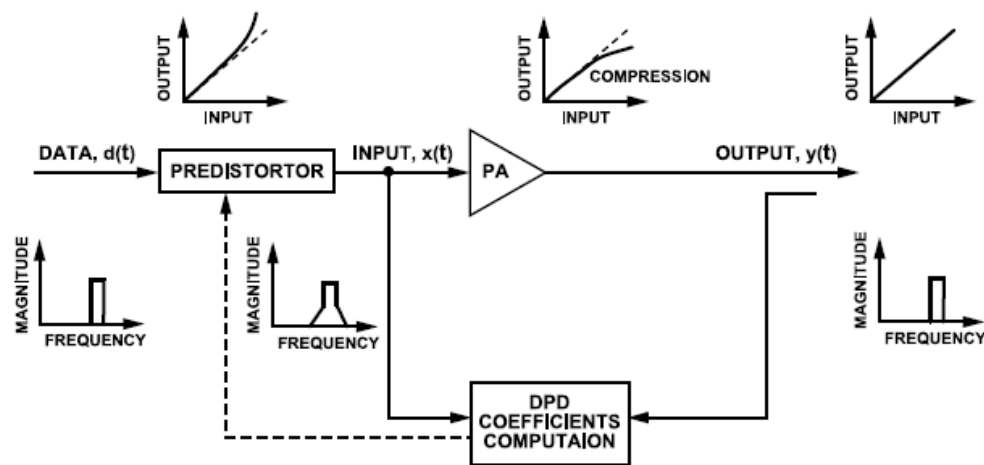
Initial + Tracking Calibrations



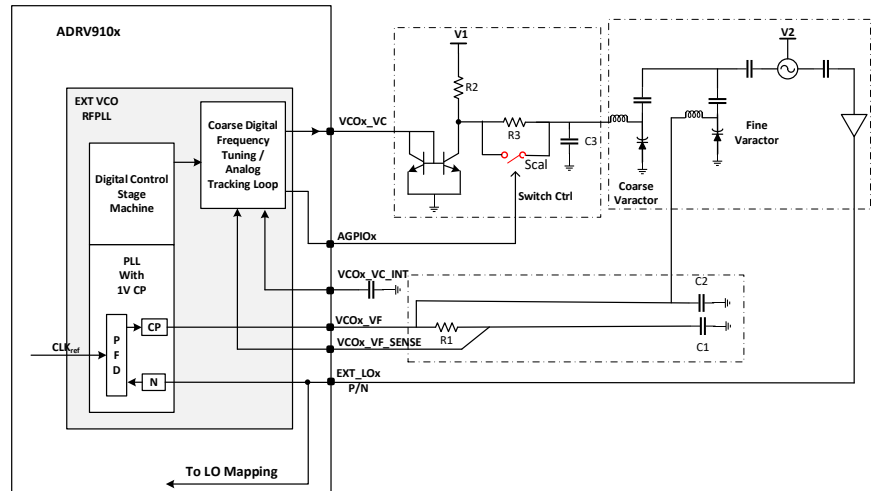
Automatic Gain Control (AGC)



Digital Pre-Distortion (DPD)



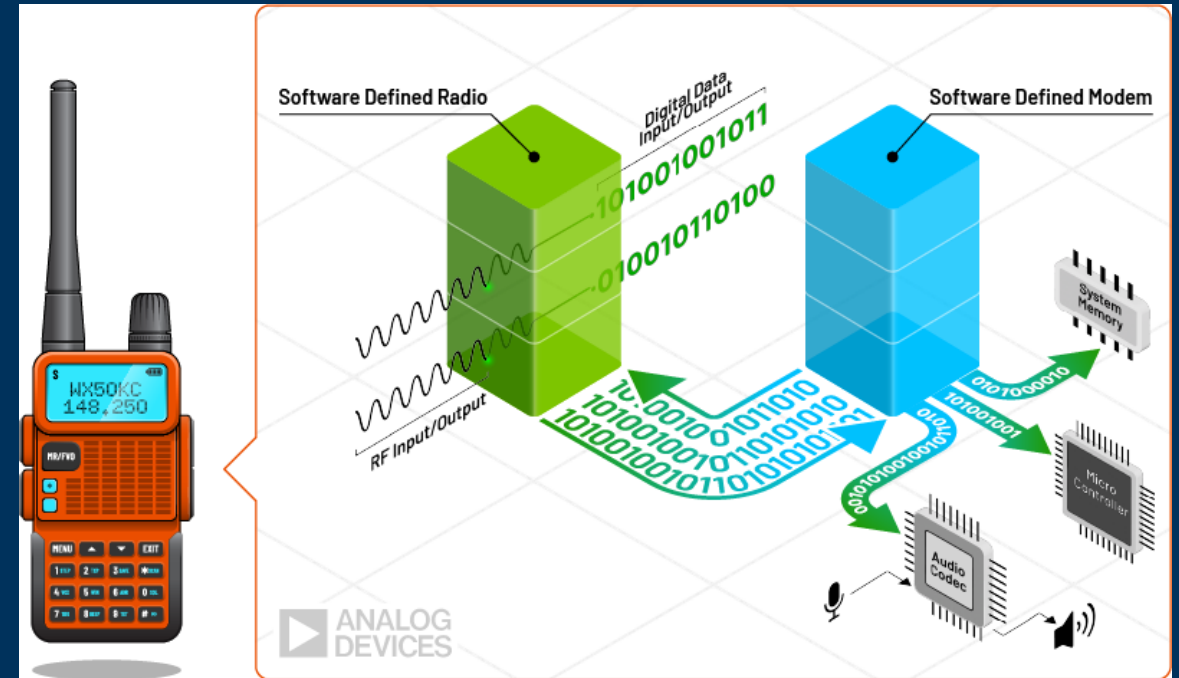
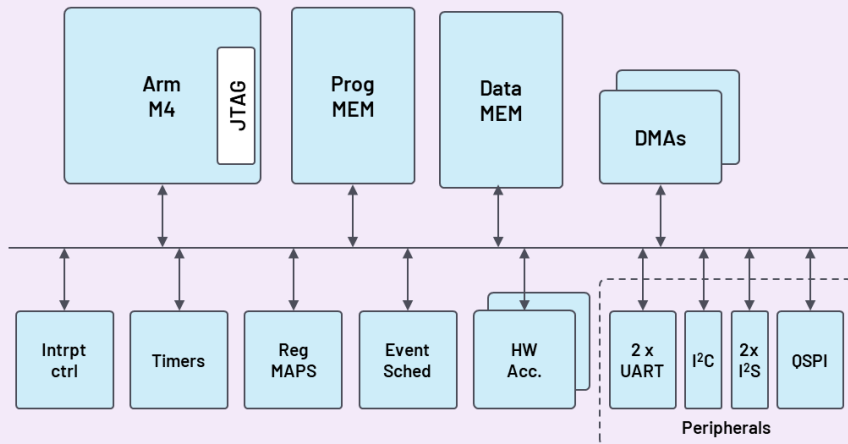
External VCO



The Nevis Software Defined Modem (SDM)

- The Nevis SDM provides a diverse set of capabilities to integrate, interface and optimize a variety of system level functionality
- SDM Advantages include:
 - Library of Hardware Accelerators perform PHY layers 1-3 functionality at reduced power consumption
 - Can self-boot the Nevis TRx, accelerating radio availability
 - Reduces external BBIC performance and interface requirements, enabling selection of lower cost components

Software Defined Modem (SDM) Architecture

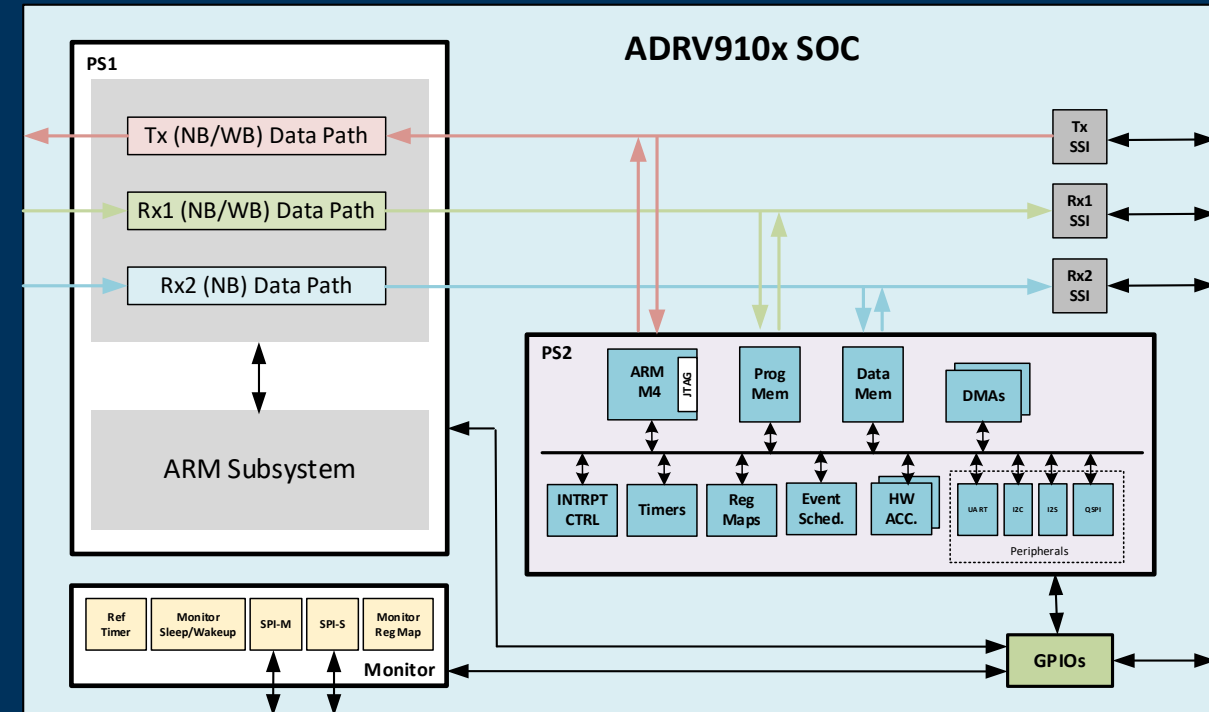


- The Nevis SDM executes user defined ARM code and can leverage any of the available functions and peripherals of the SDM
- SDM software development will be supported via:
 - CodeFusion Studio
 - Simulink Hardware Support Package
 - Provides full simulation and code generation capabilities

Nevis Processing Subsystem (PS2)

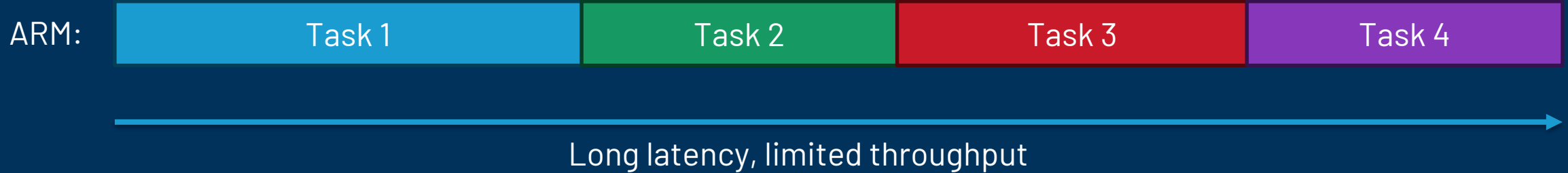
- The Nevis PS2 is a flexible, customer programmable processing subsystem that can be used for:
 - Pre-Processing Tx Data; Post-Processing Rx Data
 - Implementing the communication protocol layers
 - Timing, Interrupt and Event Scheduling operations
 - Controlling external elements through GPIO or Peripheral I/O's
 - ...and more
- The PS2 Incorporates Multiple Subsystems, such as:
 - ARM Cortex-M4 Processor
 - Up to 200MHz, 1MByte memory, JTAG interface
 - 4 x General Purpose Timers, 1 x Watchdog Timer, 1 x SysTick Timer
 - Interrupt Controller and Event Scheduler
 - Direct Memory Access (DMA) modules
 - HW Accelerators supporting signal and data processing. Examples include:
 - Arithmetic: Log, Atan
 - Signal Processing: IIR, FIR, Up Sample, Down Sample
 - Error Detection and Correction: CRC Encoder/Decoder, TCM Encoder/Decoder

PS2 capabilities can offload processing from the baseband IC

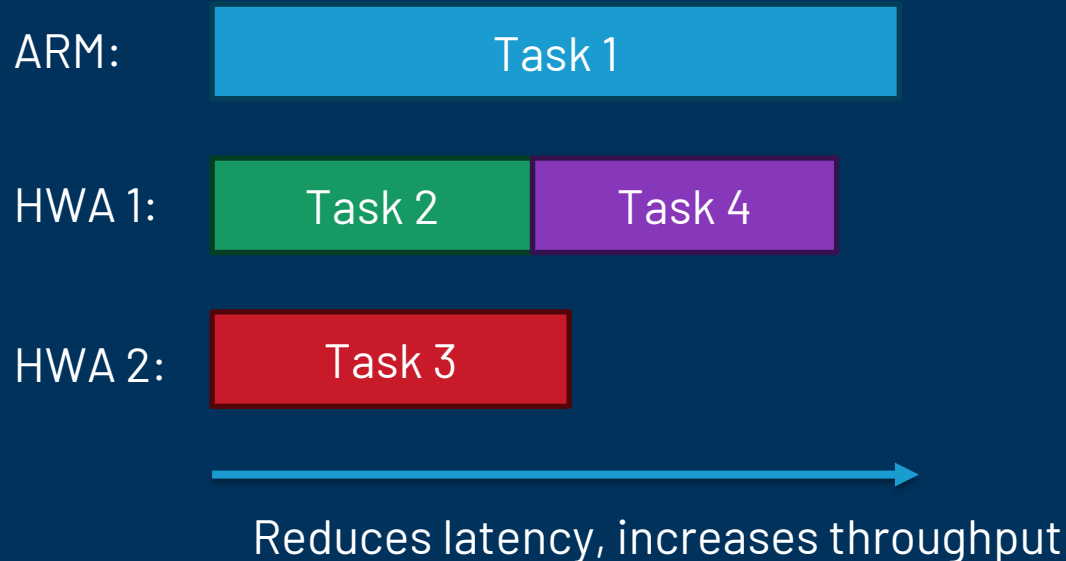


Hardware Accelerator (HWA) Value Proposition

ARM Only Processing:

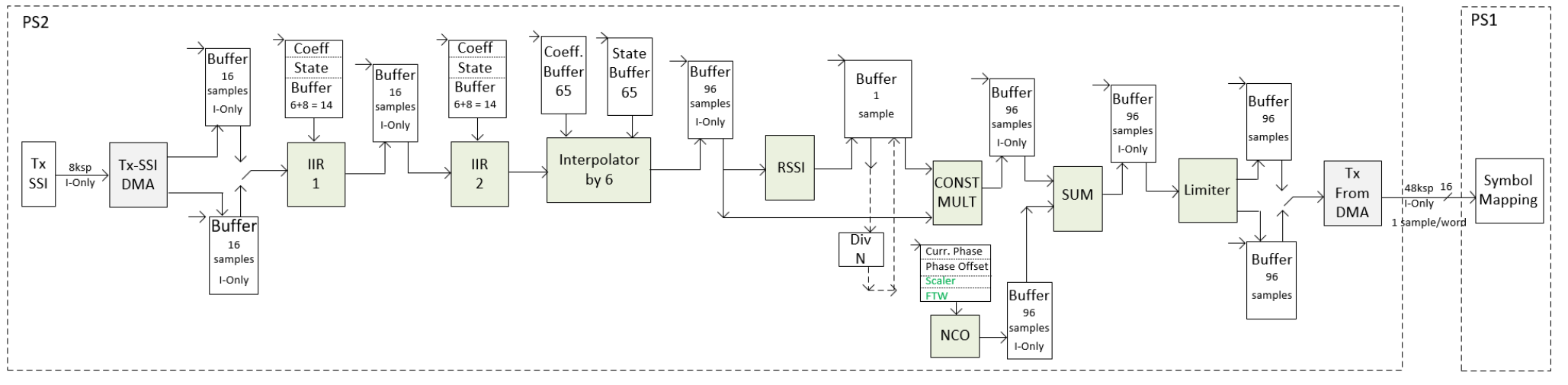


ARM + HWA Processing:

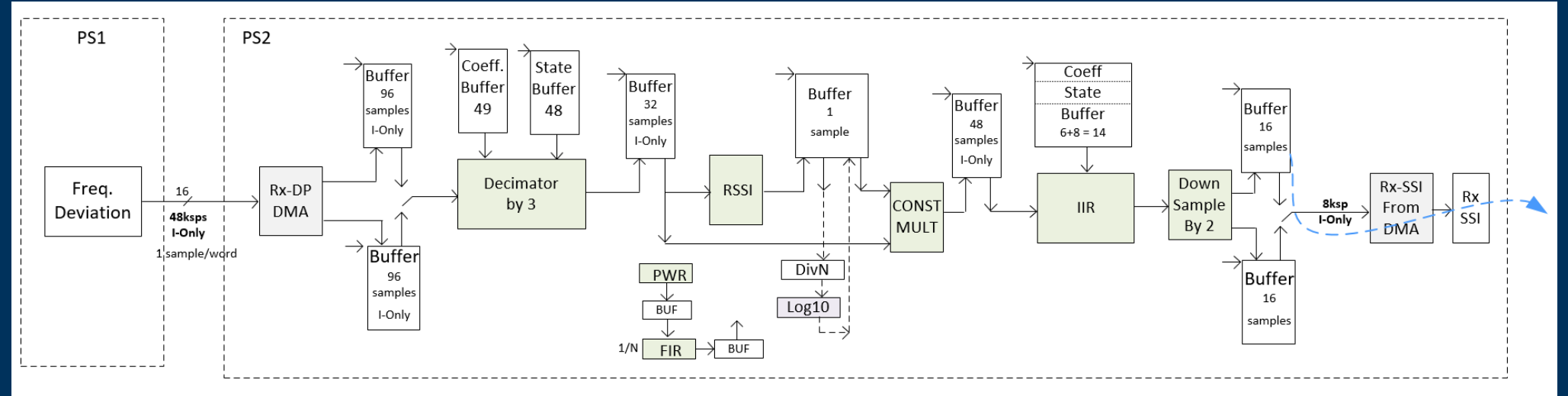


- Using ARM + HWA:
 - Reduces latency
 - Increases throughput
 - Reduces total power consumption

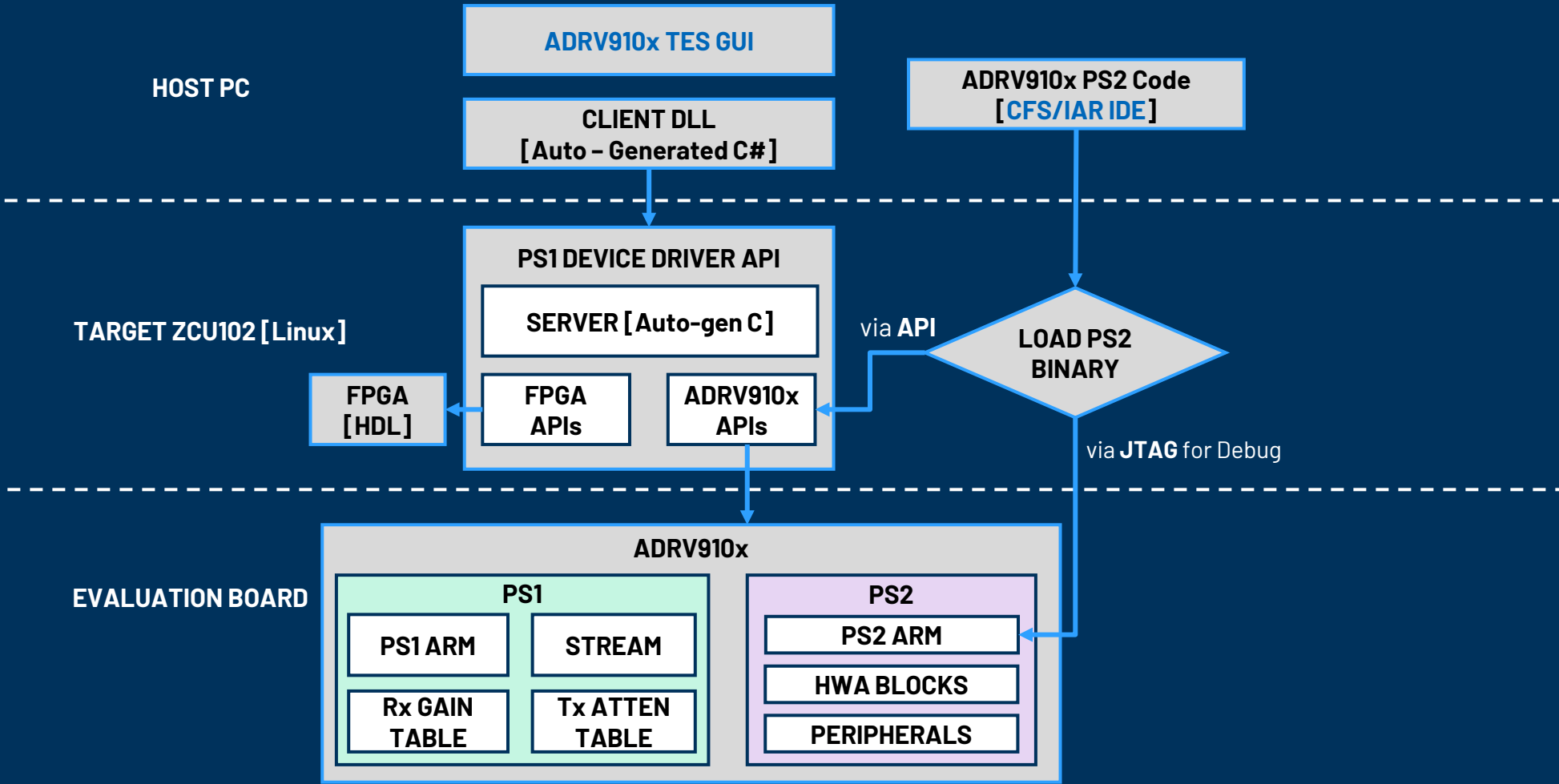
HWA: Tx Example



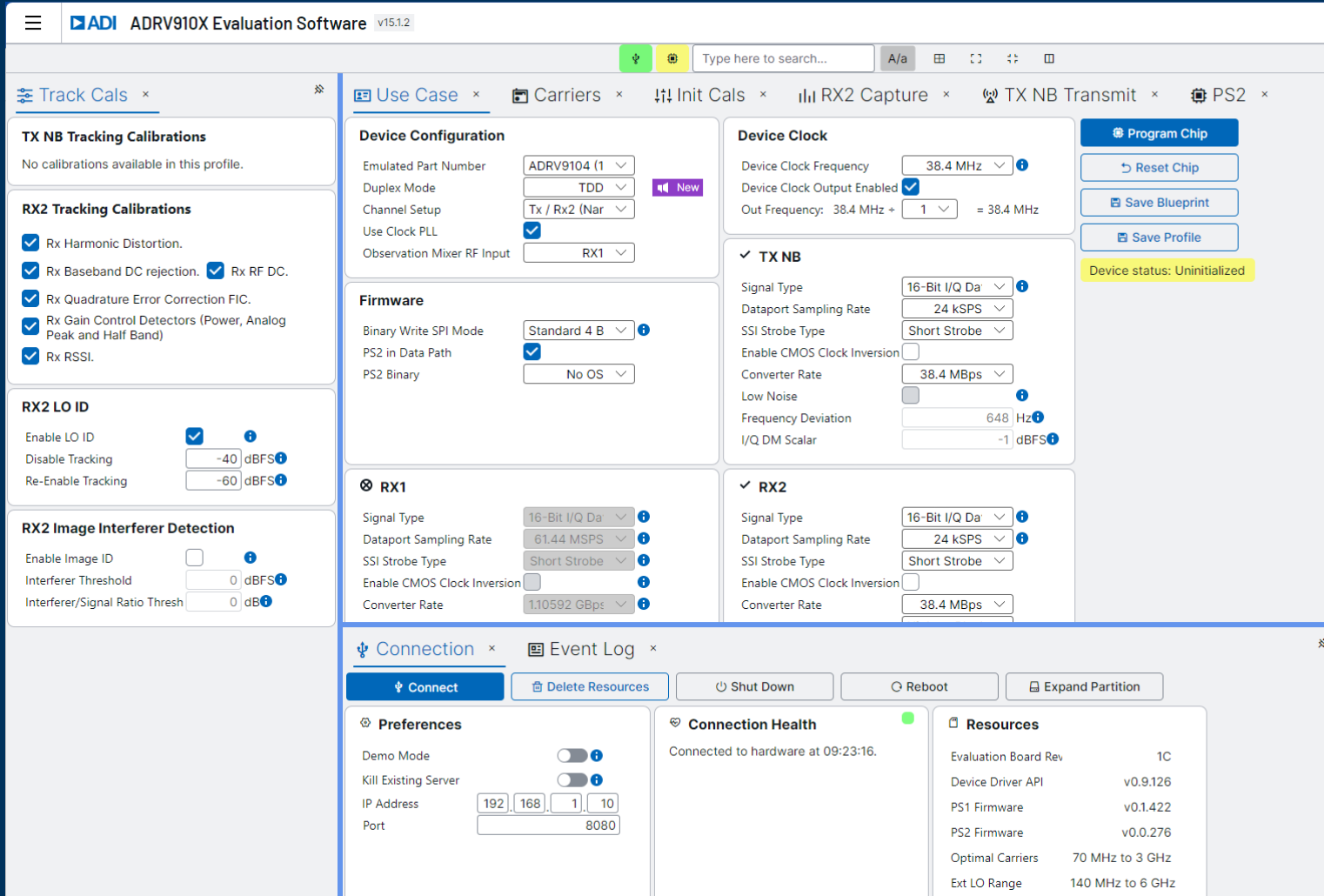
HWA: Rx Example



Nevis Software Architecture Evaluation & Development Platform



ADRV910x Transceiver Evaluation Software GUI



The screenshot displays the ADRV910x Evaluation Software v15.1.2 GUI. The interface is organized into several main sections:

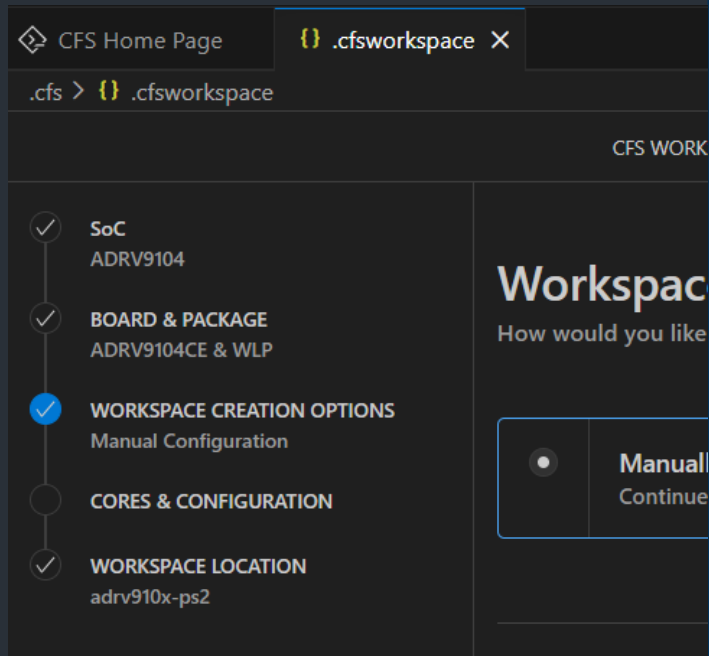
- Track Cals:** Includes TX NB Tracking Calibrations (no calibrations available), RX2 Tracking Calibrations (Rx Harmonic Distortion, Rx Baseband DC rejection, Rx RF DC, Rx Quadrature Error Correction FIC, Rx Gain Control Detectors, Rx RSSI), RX2 LO ID (Enable LO ID, Disable Tracking, Re-Enable Tracking), and RX2 Image Interferer Detection (Enable Image ID, Interferer Threshold, Interferer/Signal Ratio Thresh).
- Use Case:** Contains Device Configuration (Emulated Part Number, Duplex Mode, Channel Setup, Use Clock PLL, Observation Mixer RF Input), Device Clock (Device Clock Frequency, Device Clock Output Enabled, Out Frequency), Firmware (Binary Write SPI Mode, PS2 in Data Path, PS2 Binary), and RX1/RX2 settings (Signal Type, Dataport Sampling Rate, SSI Strobe Type, Enable CMOS Clock Inversion, Converter Rate).
- Carriers:** A tab for carrier configuration.
- Init Cals:** A tab for initialization calibrations.
- RX2 Capture:** A tab for RX2 capture settings.
- TX NB Transmit:** A tab for TX NB transmit settings.
- PS2:** A tab for PS2 settings.
- Connection:** Includes a Connect button, Delete Resources, Shut Down, Reboot, and Expand Partition buttons. It also shows Preferences (Demo Mode, Kill Existing Server, IP Address, Port), Connection Health (Connected to hardware at 09:23:16), and Resources (Evaluation Board Rev, Device Driver API, PS1 Firmware, PS2 Firmware, Optimal Carriers, Ext LO Range).

- GUI tool for configuring and controlling the ADRV910x evaluation platform
- Allows device configuration and programming with desired operating parameters
- Supports custom waveform files for transmission and signal observation on receiver ports
- Can generate initialization sequences in C99, C#, Python or MATLAB

CodeFusion Studio



A comprehensive software development environment tailored for ADI analog and digital technologies.



Software Development Kit (SDK)

Includes drivers, OS's, middleware, libraries and domain-specific reference applications



Integrated Development Environment (IDE)

Facilitates heterogeneous application development, debugging, and optimization.

Not just a Microsoft's Visual Studio Code Extension. Extensible set of Tools through a dedicated CFS Installer.



ELF File Explorer

Save hours by running SQL queries against firmware images for resource placement, memory usage, and compiler settings in a convenient graphical tool versus manually collating results from numerous command line utilities.



Pin Configuration*

Assign signals to pins, configure pin values such as input or output mode and power supply, view register details and values, and generate source code to be included in your project.

* Under Development

Nevis Development Walkthrough



PS1 (TRx)

TES:

- Configure device as desired
- Evaluate RF Performance
- Test device features
- Monitor power consumption

TES + Python/MATLAB SDKs:

- Configure device using TES and/or Python/MATLAB
- Automated testing with hardware-in-loop

TES:

- Auto generated C code based on desired configuration

Baremetal C API:

- Port C application code directly to custom host controller

Evaluate

Prototype

Production

PS2 (SDM)

TES:

- Explore PS2 demos for RF, system and peripherals

CFS:

- Analyse source code for TES PS2 demos
- Run example code for all PS2 drivers

CFS:

- Modify and debug PS2 code
- Include custom scheduling/OS

Simulink HSP:

- Simulate custom DSP with PS2 drivers
- Load Simulink code directly to PS2

CFS/Simulink:

- Develop full application code
- Compile and load PS2 application onto custom platform

AHEAD OF WHAT'S POSSIBLE

analog.com

