

TECHNICAL ARTICLE

High Fidelity PCB Design for Multichannel Beamformers –Part 1: Return Loss

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Abstract

This is Part 1 of a two-part article series. Part 1 discusses designing PCBs with highly accurate 50 Ω transmission lines and minimizing impedance discontinuities at connector transitions to reduce return loss. [Part 2](#) will discuss isolation between transmission lines, how isolation affects beamformer IC performance, and how to choose the correct line topology for a given isolation requirement.

Introduction

Modern integrated beamformer ICs (BFICs) typically have multiple parallel paths on a chip that have independent controllable gain and phase. Common BFIC configurations have two or more of these on-chip RF paths routed to pins that are either on the same edge and/or the same corner of the IC package. Figure 1 shows a 4-input, 4-output BFIC with all four inputs on the same edge of the IC package and all four outputs on the opposite edge. This device architecture is used on Analog Devices' [ADAR3000/ADAR3001/ADAR3006/ADAR3007](#) family of Ku and Ka band beamformer ICs. The BFIC must also support all the digital, power, and other miscellaneous pins that are required for operation.

The relatively close pin-to-pin placement on the BFIC is a consequence of the large number of RF inputs and outputs and their associated ground-signal-ground configuration. Routing multiple highly accurate RF lines from these closely spaced pins to different devices, to connectors, or to other printed circuit boards (PCBs) is challenging. Poor transmission line impedance accuracy and poor impedance transitions (for example, in the transition between two boards) result in signal reflections. This reduces the RF power delivered to the load and decreases gain. Lower system gain and reduced output power degrade effective

isotropic radiated power (EIRP) in transmitters. Large enough signal reflections can also cause instability, especially if the circuit design is susceptible to reflected power from its load.

This article discusses how to design and manufacture highly accurate RF PCB transmission lines and connector transitions with excellent return loss that route signals onto and off of the PCB through the transmission lines connecting to high count RF input and output BFICs. While the focus is on BFICs and phased array applications, the material applies equally to any high frequency circuit design where good impedance matching is important. While multiple design techniques will be presented, the important topic of design for manufacturing will also be covered. Note that this article provides dimensions primarily in mils (1000 mil is equal to 1 inch). To convert from mil to mm, multiply by 0.0254.

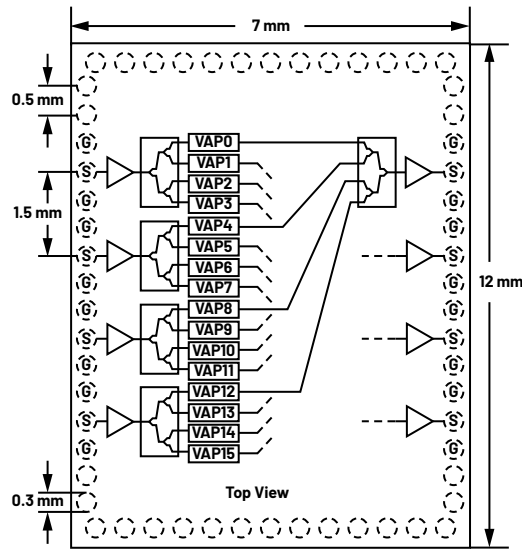


Figure 1. An anatomical block diagram of a 4-input, 4-output, 16-channel BFIC chip in BGA package; outline dimensions not to scale with ball-to-ball pitch and ball diameter.

Manufacture of Various Transmission Line Topologies

PCB fabricators support multiple popular RF transmission line topologies including microstrip, grounded coplanar waveguide (GCPW), stripline, and the less popular buried GCPW (BGCPW), which resembles a hybrid of GCPW and stripline. While microstrip is relatively easy to manufacture, for operation above 6 GHz, it is less popular because of its higher trace loss and poor mode suppression.¹ GCPW, BGCPW, and stripline operate better above 6 GHz because of lower radiation loss and better mode suppression. Buried line topologies improve isolation but are harder to fabricate and require vias to connect to them. These vias are usually blind to minimize parasitic inductance, resulting in higher board cost.

Figure 2 shows a cross-section of GCPW, buried GCPW, and stripline and the important geometries that set the nominal line impedance. These are the line width ($W1/W2/W3$), the lateral distance from the edge of the line to the adjacent ground plane ($G1/G2/G3$), the thickness of the dielectric materials ($T1/T2$), and the relative permittivity of the dielectric materials ($\epsilon_{R1}/\epsilon_{R2}$). Figure 2 does not show the thickness of the copper used for the lines or the required ground via fencing. Copper thickness does need to be considered but it is a secondary effect. The required ground via fencing will be discussed in Part 2. The choice of topology depends on acceptable trace loss, frequency, required line-to-line isolation, available space, and dielectric thickness of the PCB material.

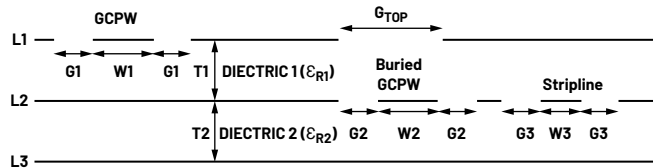


Figure 2. Cross-section of GCPW, buried GCPW, and stripline topologies.

Effects of Manufacturing Tolerances on Line Impedance

The quality of RF line topologies is affected by fabrication tolerances. Choosing the optimal geometries of the line to minimize these effects is crucial to obtaining an accurate 50 Ω line impedance. Figure 3 shows a time domain reflectometry (TDR) plot of a 3 mil wide stripline that was designed for 50 Ω but was measured to be approximately 60 Ω . An error of no more than $\pm 10\%$ was desired (45 Ω to 55 Ω) to yield a return loss of 20 dB or better.

Three of the important geometries to consider when designing the line are the line width, gap to lateral ground, and the dielectric thickness. Many PCB fabricators offer minimum conductor widths down to 3 mils (depending on the copper weight) with a tolerance of 1 to 2 mil.²⁻⁴ Manufacturers usually only provide typical dielectric thickness numbers, most likely because the final thickness is determined by the PCB fabricator during the board lamination process. The lateral gap to the ground can vary as a result of the ground plane not stopping where it should. Also, the effective lateral gap width changes if the line width varies.

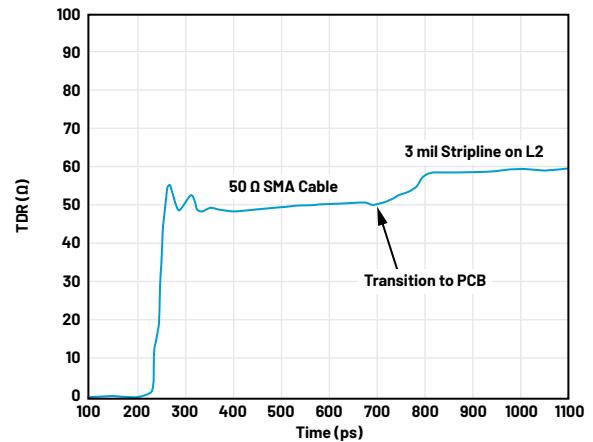


Figure 3. A TDR plot of a 3 mil wide stripline on layer 2 of a PCB.

In microstrip and stripline topologies, variations in the lateral gap width should not affect the line impedance as the lateral gap to ground distance is large by design. This results in all the field lines going to the lower ground plane in the microstrip's case and to the upper and lower ground planes for the stripline case. However, GCPW is affected more by lateral gap tolerances. By

design, the lateral gap-to-ground distance is relatively small and most of the field lines go to the lateral ground plane.

Figure 4 plots the line impedance⁵ of a stripline design vs. the line width deviation from nominal for multiple line widths. Also shown is the impedance deviation that results when the dielectric is +5% thicker than nominal (assuming a stripline copper thickness of 0.7 mils and $\epsilon_r = 3.1$). Ideally, the slope of all the lines would be 0 and there would be no intercept shift between the lines; this would indicate no fabrication variations. Notice that the wider lines have a lower slope, while the narrower lines have a steeper slope. So, in practice, where there is variance in fabrication, a wider nominal line width is preferable. Unfortunately, with a dielectric thickness increase of 5%, the impedance shift is approximately equal regardless of the nominal line widths. This means that final pressed thickness requirements must be met by the fabricator within a certain tolerance to attain the targeted line impedance tolerance. The focus is on increased dielectric thickness (vs. a decrease in thickness) because it has been observed over many board fabrication lots with different line topologies that the line impedance tends to come out greater than or equal to the design target. This leads to the rule of thumb to design the line to be a few ohms less than the target, especially when the width is thin (less than 5 mils). However, with this approach, the controlled impedance requirements that normally constrain the PCB fabricator may need to be waived depending on the impedance difference. If a thin line must be used due to other design considerations, high confidence in the chosen fabricator is paramount. Confidence can be gained organically by using a fabricator from previous designs and/or intentionally by fabricating experimental boards using the chosen line topology, with multiple lines of varying widths that would make the lines in and around 50 Ω by design. Measurements would then need to be performed to determine which line width was closest to 50 Ω .

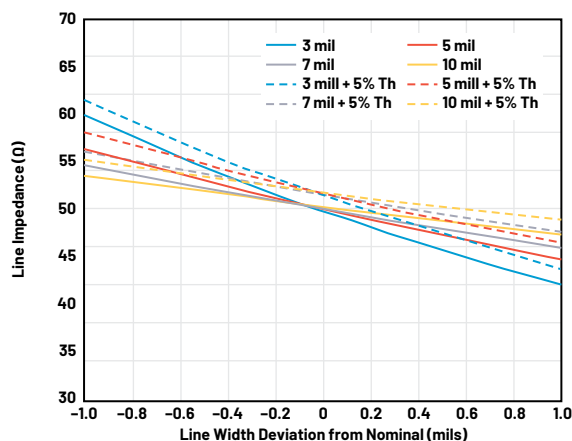


Figure 4. Impedance error (for 50 Ω) vs. fab tolerance for 3, 5, 7, and 10 mil line widths over nominal and +5% dielectric thickness.

Intra-Board Connections—Getting Signals onto and off of the PCB

RF impedance discontinuities between RF transmission lines and the RF connectors that move signals between PCBs are just as important as accurate line impedance previously discussed. When transitioning between boards, there are two physical interconnect options:

1. Edge launch connectors that mount laterally onto the edge of the PCB.
2. Vertical launch connectors that mount vertically onto the PCB.

Both types are available in SMA, SMP, SMPM, 2.92 mm, and 2.4 mm to name a few standards.

The choice of edge launch vs. vertical launch will be strongly influenced by the form factor of the end equipment. If edge-launched connectors are used, the interconnecting PCB will be arranged laterally. If the system is sitting in a single metal chassis/heat sink, this arrangement may be the best choice. If vertically launched connectors are used, it offers the possibility of stacking multiple boards sandwich style. This may result in a more compact form factor, but it also may force the use of air cooling since the individual boards are unlikely to have heat sinks. A combination of both connector types, one board having edge launch while the other having vertical launch, will have the two boards connecting orthogonally in a slotted style.

Edge Launch vs. Vertical Launch Connectors

Edge launch connectors are widely used. However, they have some potential drawbacks that stem from being attached at the board edge. Edge connectors usually require a longer trace, compared to vertical connectors, from the device to the connector. This results in increased insertion loss, parasitic capacitance, and inductance. Edge connectors also require that the top ground plane of the PCB (and preferably the bottom ground plane) extend to the edge of the board. Most PCB fabricators can only guarantee a 2 mil distance between the edge of the ground plane and the edge of the board at the connector locations when using standard edge milling/routing and etch pullback techniques. This manifests as an impedance discontinuity due to the lack of ground return in the 2 mil (or larger) gap and degrades the return loss. This discontinuity becomes more pronounced at higher frequencies.

Figure 5a shows a PCB edge connector transition with a large gap between the board edge and the ground plane, while Figure 5b shows a TDR plot showing the impedance spike

produced by a large gap at the connector. At lower frequencies, the gap may not affect the performance and could be desirable, as it keeps the end of the fragile transmission line away from the router bit that is milling the board edge. A simple fix is to end the transmission line 2 mils prior to the edge of the ground plane, which is enough distance to keep well away from the router bit (avoiding damage) while still providing a good transition for the center pin of the connector. This technique is often used in high frequency millimeter wave applications.

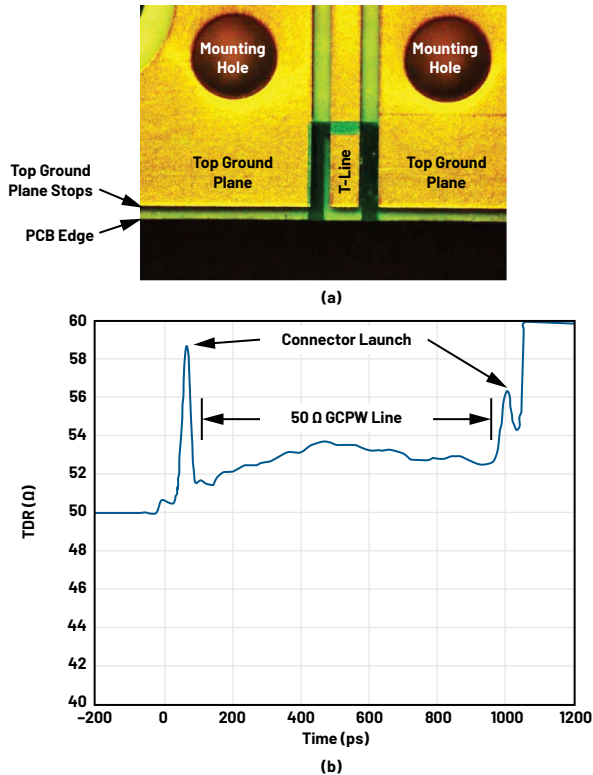


Figure 5. (a) Top view of an edge connector transition with large gap between PCB edge and top layer ground plane and (b) TDR plot of poor transition due to bad edge routing creating a large gap (second connector launch spike is due to less energy reflected).

A couple of options exist to mitigate the gap between the ground plane and board edge. The first is to use edge plating at the connector locations at the board edge. When correctly done, this effectively eliminates the gap entirely by applying metal ground plating on the vertical edge of the board. The edge plating connects to the existing top and bottom horizontal ground planes and can also connect to internal ground planes if desired. The edge plating should only be on the ground portions of the edge and thus there should be a gap between the plating at the connector locations where the transmission line is located. This is shown in Figure 6.

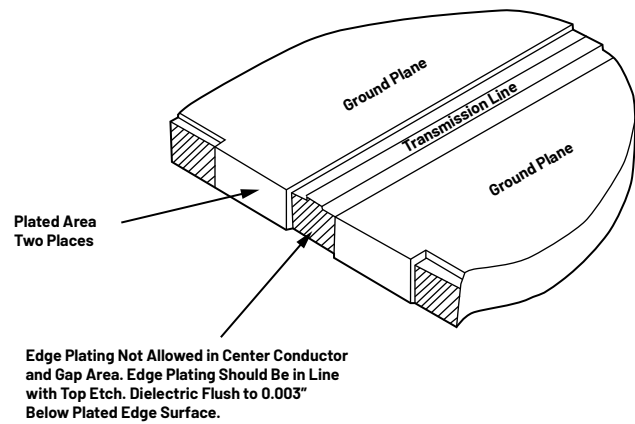


Figure 6. Cutaway of a PCB at the edge connector location showing proper edge plating.

There are some drawbacks to edge plating that stem from the quality of its fabrication. This can result in:

- A radiused cut from the circular router bit to remove the plating at the transmission line (keeping the edge of the PCB planar is desirable).
- Inconsistent routing before the edge plating occurs that leads to transmission line length matching problems (keeping the same length as the calibration traces is very important).
- Plating that extends from the ground locations on the board edge and encroaches into the transmission line area. A worst-case example is the plating being continuous over the entire connector location, including where the transmission line sits as shown in Figure 7. This can result in the transmission line shorted to ground.

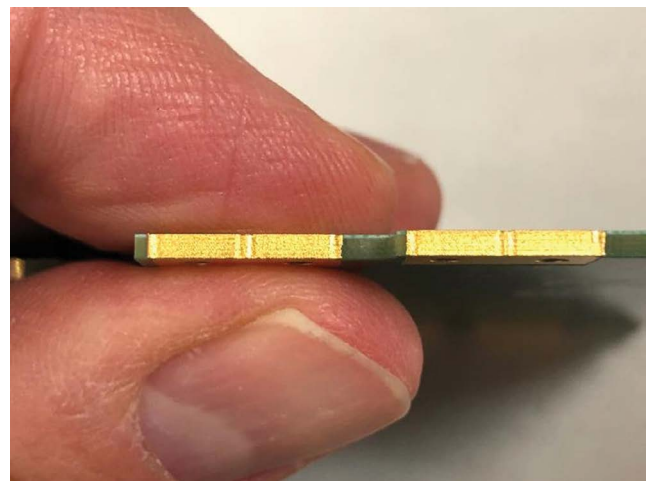


Figure 7. Example of edge plating that encroaches from the ground locations into the transmission line area (side view of PCB).

The first two quality issues are undesirable and do degrade the PCB performance. However, they are not catastrophic. The third quality issue is catastrophic and renders the PCB unusable and requires a mechanical rework to remove the edge plating in the transmission line area. The only feasible way to ensure that edge plating maintains high quality is to mandate the edge plating requirements in the PCB fabrication notes. Depending on how strict the requirements are, fabricators may have to refabricate PCB lots. Or they may decline the work.

Laser edge routing is another option. Laser edge routing involves cutting the board from its panel with a laser. This can be done along the entire edge of the board, but only needs to be done at the connector locations, with mechanical routing on the rest of the board edge. Not all PCB fabricators offer laser edge routing. Vendors that do typically only guarantee the gap to 1 mil and that is generally only achievable if the PCB is relatively thin. Some PCB fabricators require the board to be less than 14 mils thick, while others can offer this accuracy on boards that are up to 40 mils thick. That is still relatively thin and brings the possibility of board warpage into play, especially with larger boards, and is usually not thick enough for boards with a high layer count.

Edge plating and laser edge routing can increase cost, complexity, and fabrication time. If the form factor of the end equipment permits boards to be sandwiched together (vs. being laterally connected), vertical launch interconnects can be a viable option.

Vertical Launch Interconnects

Because they are not bound to the board edge, vertical launch connectors are not susceptible to the edge routing issues described above. On simple, single device boards, the connector(s) can be placed close to the device being tested, resulting in minimal insertion loss.

In addition, the transition onto the board can be RF matched so that the impedance discontinuity is minimized. Connector vendors such as SVMicrowave will create a custom footprint for a given line design and stack-up. A footprint for an SVMicrowave vertical launch connector that interfaces to a stripline design is shown in Figure 8. Four PCB layers are shown with the via fencing. The 30 mil diameter void on layer 3 (L3) is the matching for the connector and is shown in Figure 8c.

One disadvantage of vertical launch connectors is that it can be difficult to achieve good alignment between the connector and the PCB footprint. Ideally, the circular center pin of the connector connects to its circular pad on the PCB and their centers would be aligned. However, when looking down at the connector when mounting on the 2D ground plane, left-to-right and forward-to-back movement is possible and can cause the center pin to be not centered with the PCB pad. Connectors that are intended for lines running on the top layer do have a mouse hole at the front of the connector that can be useful for alignment, especially of the left-to-right movement (these mouse hole

connectors have been successfully used with striplines as well). Mounting hole size tolerance should be tight so there is minimal excess movement of the connector. If exact alignment is needed, which is the case at frequencies >35 GHz, Rosenberger offers connectors that launch at 45° to the board (vs. the 90° vertical connectors) and can be manually aligned much easier than the vertical connectors. However, these 45° launch connectors are more expensive than their vertical and edge launch counterparts and require a much larger footprint on the PCB.

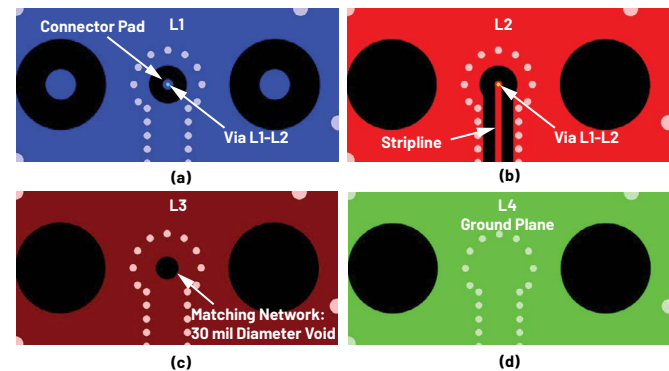


Figure 8. Layout of custom vertical connector footprint: (a) the top ground on layer 1, (b) stripline on layer 2, (c) 30 mil void on layer 3 for matching, and (d) solid ground plane on layer 4.

Conclusion

The advent of high frequency beamformer ICs and other high frequency multichannel RF ICs is making PCB design more challenging. When approaching these challenging designs, PCB designers need to preempt potential manufacturing problems by avoiding the use of very thin RF traces and generally design for characteristic impedance that is slightly below the target value of 50 Ω . When designing board-to-board interconnects, top launch or edge launched interconnects will most likely be chosen based on the form factor of the end equipment. Top launched interconnects are less susceptible to manufacturing limitations that can happen at the edge of the board.

Part 2 of this article series will discuss how transmission line isolation can affect the performance of high frequency beamformer ICs, differences in isolation between transmission line topologies, and how to choose the best transmission line for the given application and BFIC geometry.

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- ⁵"Stripline." Microwaves101.

About the Author

Joel Dobler is a principal product applications engineer in the Aerospace and Defense and Communications Group, focusing on beamformer products, but also supporting vector modulators and programmable low-pass filters. He has worked for Analog Devices since 2006, supporting a wide range of RF products including logarithmic and rms detectors, digital and analog variable gain amplifiers, mixers, and I/Q demodulators. He received his B.S.E.E. degree from Washington State University in 2005 and his M.E.E. degree from Portland State University in 2007.

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