

TECHNICAL ARTICLE

High Fidelity PCB Design for Multichannel Beamformers –Part 2: Isolation

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Abstract

This is Part 2 of a two-part article series. Part 1 discussed designing PCBs with highly accurate 50 Ω transmission lines and minimizing impedance discontinuities at connector transitions to minimize return loss. Part 2 discusses isolation between transmission lines, how isolation affects beamformer IC performance, and how to choose a correct line topology for a given isolation requirement.

Introduction

Good channel-to-channel isolation is critical for maintaining performance in beamformer integrated circuits (BFICs). Channel-to-channel gain settings in phased array applications can vary significantly to achieve the desired element tapering for sidelobe reduction and muting (a 30 dB difference is not unusual). As shown in [Part 1](#), modern BFICs typically have multiple parallel RF paths on chip that are routed to pins that are either on the same edge and/or same corner of the IC package, often with all inputs (or outputs) also on the same edge. As a result, the challenge is in routing the multiple RF lines to and from these closely spaced pins on printed circuit boards (PCBs) while maintaining sufficient isolation between the lines.

Part 2 of this article series discusses how the amount of isolation between transmission lines affects the performance of BFICs, general guidelines on how to choose the best transmission line topology based on the application's isolation requirement and BFIC geometries, and how best to fanout closely spaced transmission lines near the BFIC. This article provides dimensions primarily in mils (1000 mils is equal to 1 inch). To convert from mil to mm, multiply by 0.0254.

Isolation: From Transmission Line to Transmission Line

On any PCB, two adjacent transmission lines will have some amount of coupling between them, either electrically and/or through the electric and magnetic (EM) fields, resulting in noninfinite isolation. There are large differences in isolation performance between the line topologies discussed in Part 1. Top layer routing generally has worse isolation than buried lines due to field coupling. Beyond the chosen line topology, the dominant factors that affect isolation are operating frequency, the distance between the lines, and the parallel routing distance of the lines. Also, if using a buried topology such as stripline, any transitions to the top layer must be designed carefully to maintain good isolation.

Figure 1 shows a Keysight RFPro EM simulation of isolation vs. frequency for two pairs of transmission line topologies: grounded coplanar waveguide (GCPW) and buried GCPW. Center-to-center distance between each pair of lines was set at 60 mils, with a parallel routing distance of 200 mils. Six mil ground vias spaced 25 mils center-on-center were used for fencing on either side of each line. GCPW has worse simulated isolation than

buried GCPW. Clearly a buried topology should be chosen where isolation is critical.

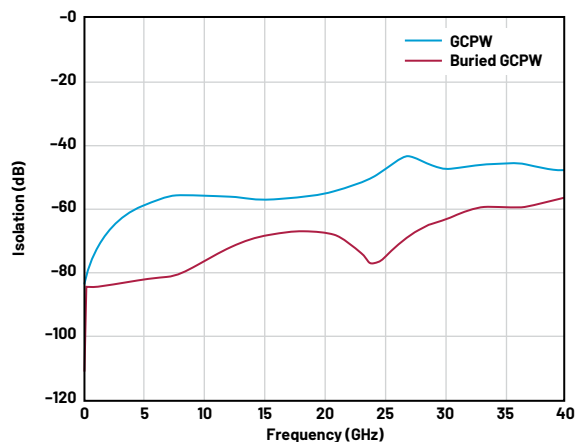


Figure 1. Simulated isolation of GCPW and buried GCPW.

GCPW vs. Buried GCPW: What a Difference 15 dB of Isolation Can Make

Poor isolation between transmission lines on a PCB can be especially problematic in applications where there is a large difference between the signal levels in the respective traces. In a phased array system, if two adjacent variable amplitude and phase (VAP) blocks are operating at minimum and maximum attenuation, parasitic signal coupling will degrade the linearity of the VAP's gain control function in the more attenuated path. This behavior was observed on the [ADAR3001](#), a 4-input, 4-output BFIC (similar to what is shown in Figure 1 in Part 1), on a PCB with GCPW transmission lines. The PCB was redesigned with buried GCPW to increase the isolation between lines.

The rms gain error is an abstracted figure of merit that is an indicator of gain control nonlinearity. In this case, rms gain error was measured on both versions of the PCB. Figure 2a shows the rms gain error of the original PCB with GCPW, while Figure 2b shows the rms gain error of the redesigned PCB with buried GCPW. In Figure 2a, the rms gain error is significantly worse when the VAP's digital stepped attenuator (DSA) is exercised over its full range. This is to be expected because the application is most susceptible to poor isolation when the delta between a DSA's attenuations is at its largest.

The higher line-to-line isolation of the buried GCPW board improved rms gain errors significantly, aligning with simulations and displaying the actual performance of the BFIC. These results show that even a moderate improvement in isolation of 15 dB at 30 GHz can affect the measured performance dramatically.

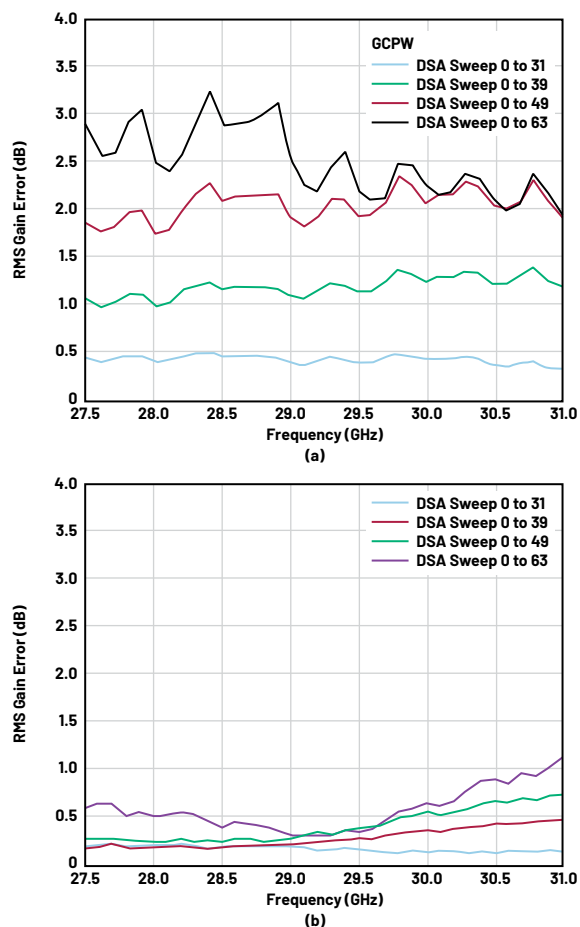


Figure 2. BFIC rms errors on a PCB with (a) GCPW lines vs. a PCB with (b) buried GCPW.

Isolation of Two Parallel Striplines

It is generally assumed that stripline topology gives the best isolation of the topologies mentioned. To test this assumption, an experimental board was fabricated to see how much isolation over frequency could be achieved with a stripline topology. An 8 mil wide stripline design routed on layer 2 was used on 8 mil Rogers 4003C (layer 1 to layer 2) and 8 mil 4450T (layer 2 to layer 3) dielectrics. The center-to-center distance of the line pair was 76 mils and the parallel run length was 300 mils. These distances were chosen to approximately emulate the average pitch between RF pins of many BFICs and the subsequent routing the lines must take before fanout to coaxial connectors or other devices. Each line had its own via fencing with 10 mil vias and 18 mil center-on-center pitch. Figure 3a shows the stripline layout on layer 2 (not shown are the layer 1 and layer 3 ground planes that sandwich the stripline on either side of the Rogers dielectrics). The isolation measurement is shown in Figure 3b and clearly proves that uninterrupted stripline with tight via fencing yields optimum performance and should be used where isolation requirements are very high.

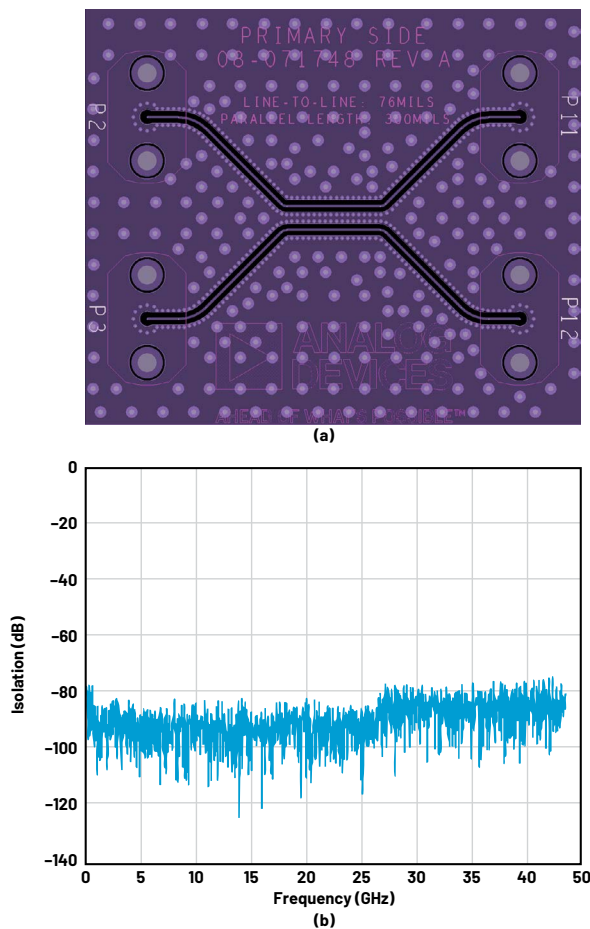


Figure 3. Layout of an experimental board with stripline design (layer 2 shown) and (b) the isolation results of the board.

The isolation plot is noisy due to the isolation of the line pair being on the edge of the measurement capabilities of the vector network analyzer (VNA). The average isolation at all frequencies is better than -80 dB. The decrease in isolation that occurs at roughly 26 GHz is due to the VNA.

Isolation of Two Parallel Striplines with Back-to-Back L1-to-L2 Vias

On the same experimental board introduced in the previous section, another pair of striplines was designed with all the same attributes as before (line geometry, via placement, line-to-line spacing, and parallel run length) but a pair of transition vias (or back-to-back layer 1 to layer 2) were added to each line to see how isolation degrades when transitioning to the top layer, as shown on the left side in Figure 4a. Top layer routing was kept short at 14 mils between via centers as shown in the zoomed in image on the right side of Figure 4a.

Isolation was measured on these striplines with back-to-back transition vias (back-to-back layer 1 to layer 2 vias) and found to be degraded compared with lines that have no transition vias, as shown in Figure 4b. This experiment highlights the importance of

careful via design when transitioning to the top layer for device interfacing.

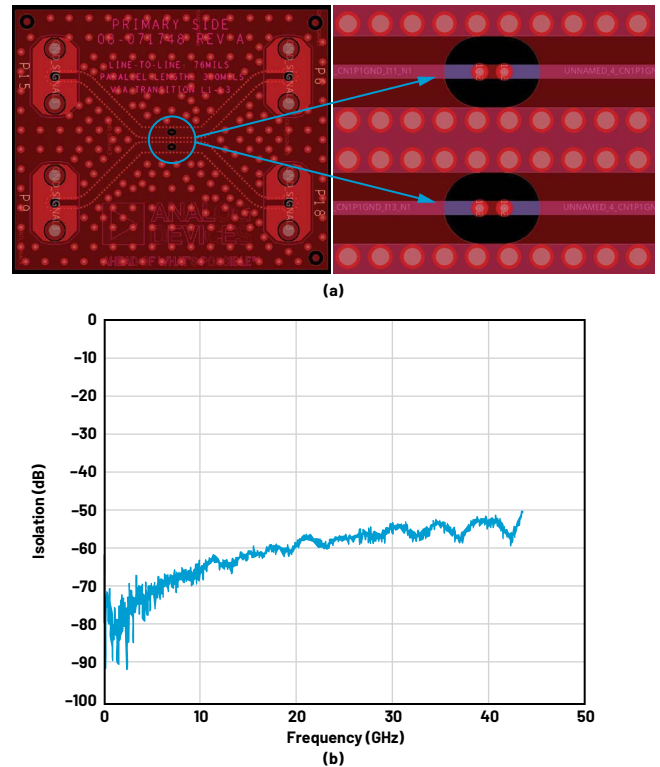


Figure 4. (a) A layout of experiment board zoomed out view (left) and zoomed in view (right) of a stripline pair with back-to-back transition vias and (b) a measured isolation of experimental board with transition vias.

Guidelines on Routing Multiple RF I/Os

Many ICs, RF beamformers in particular, have a high RF I/O count, which is difficult to route while maintaining good RF performance. Along with careful choice and design of the transmission line topology, correct ground via fencing all the way into the device is key to maintaining RF performance— isolation in particular.

Which Transmission Line to Use

The decision on which transmission line to use should be primarily based on the isolation requirement and the geometries of the BFIC. For example, if the isolation only needs to be around -40 dB, then a GCPW can be safely used. If the isolation needs to be around -65 dB, that requires the use of stripline. The geometry of the BFIC should be considered next, primarily the size of each pin, the pin-to-pin pitch, and the distance between RF pins. For example, if the BFIC is a BGA with a solder ball diameter of 5.5 mils/0.22 mm, 10 mils/0.4 mm pin-to-pin pitch, and 30 mils/1.2 mm of distance between the closest RF pins, and if the isolation requirement is -65 dB or better, the BFIC geometries could support a symmetrical stripline with approximate dimensions of: 6 mil line width, 6 mil thick dielectric (above and below the line), and a 10 mil lateral gap to ground assuming a dielectric constant in the low threes. The rule of

thumb for stripline is to have a lateral gap to ground distance that is approximately $2\times$ that of the line width; smaller gap distances start to affect line impedance. Smaller distances between RF pins would require a thinner width, whereas a larger distance between RF pins would accommodate a wider line. As seen in Part 1, the latter is preferable as there is a higher chance of attaining $50\ \Omega$ in manufacturing.

Routing near the Device

When using a stripline, care must be taken when transitioning to the device pin on the top layer as this transition can degrade the isolation significantly if appropriate grounding vias are not used. To attain the highest isolation, the ground wall of vias should extend around the end of the stripline at the device transition as shown in Figure 5. Doing this extends the critical ground wall required for best isolation performance. The device should also have ground pins, bumps, and/or ground paddle that surround the signal pin and should roughly coincide with the extended ground wall vias.

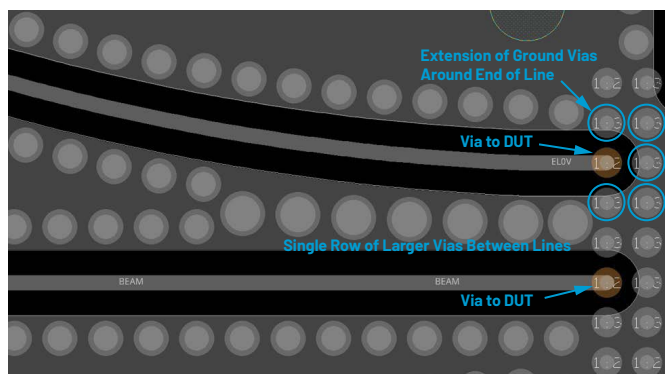


Figure 5. Vias extending around transmission line at device and going to a single row of vias between lines.

RF I/O pins that are located a short distance from each other may not provide enough area for each transmission line to maintain its same via fencing all the way into the device. Depending on available area, the typical options for the via fencing are:

1. Use smaller vias if they do not violate the fabricator's aspect ratio rules for the dielectric thickness.
2. Stagger the vias in a sawtooth pattern where there is a moderate amount of area if the absence of a via on one of the lines at the device interface will not degrade isolation.
3. As shown in Figure 5, go to a single row of vias between the lines using a larger via size, while keeping the same distance between the edges of the vias holes as was on the smaller vias; this maintains the isolation performance.
4. Go to a single row of vias between the lines using the same via size, when space is very limited between the lines.

The decision of when and how to fanout largely depends on where the RF I/O pins are in relation to each other on the device.

The general rule of thumb is that fanout should happen as soon as it is feasible to reduce parallel runs and thereby keep isolation as high as possible. As seen in Figure 5, the fanout can happen immediately due to the relative positions of the shown RF I/O pins (and pins that are not shown). However, Figure 6 shows the fanout of a 2-channel, 8-output device where each channel has a 1:4 switch as an output stage, which drives four transmission lines of different parallel run lengths. In this case, the fanout was also constrained by the non-RF I/O routing and associated circuitry on the north and south side of the device, which limited where and how the eight transmission lines could be routed.

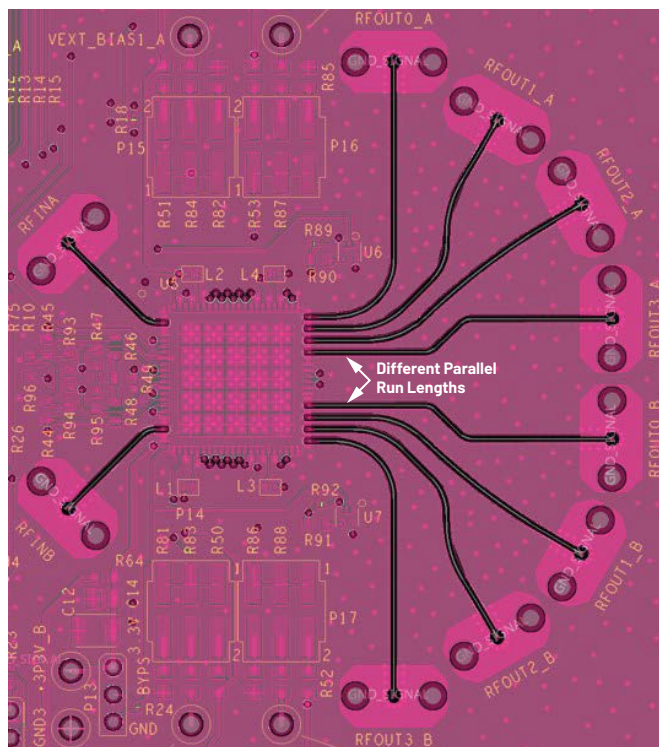


Figure 6. Fanout of eight RF outputs from a 2-channel device.

Conclusion

The advent of high frequency multichannel beamformer and other RF ICs is making PCB design more challenging both in terms of transmission line and transition accuracy (discussed in Part 1) as well as maintaining the high channel-to-channel isolation required to sustain device performance (discussed in Part 2). RF transmission line designs are going through a forced migration from surface level grounded coplanar waveguide to buried stripline, but even with buried stripline designs, care must be taken to maintain isolation between adjacent traces using closely spaced via fencing that fully encircles the device's pins. Additionally, quick fanout of closely spaced traces from the device, creating separation of the traces, is helpful in maintaining high isolation.

About the Author

Joel Dobler is a principal product applications engineer in the Aerospace and Defense and Communications Group, focusing on beamformer products, but also supporting vector modulators and programmable low-pass filters. He has worked for Analog Devices since 2006, supporting a wide range of RF products including logarithmic and rms detectors, digital and analog variable gain amplifiers, mixers, and I/Q demodulators. He received his B.S.E.E. degree from Washington State University in 2005 and his M.E.E degree from Portland State University in 2007.

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