Simple Steps to EMI Compliance

ADM2582E and ADM2587E
Signal and Power Isolated RS–485

Passing Your EMC Certification Is a Time-to-Revenue Differentiator

Design in Time
Choose Systems Radiated Emissions Limits
Set PCB Layers
Implement Design Guidelines
Test for Success

Design for EMI Compliance
► Easily reduce emissions
► Verified component choices
► Proven PCB layout

Emissions Increase
Class A
Nonresidential
Class B
Residential
USA
EU+
Industrial
Residential, Commercial, Light Industrial

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1. Choose a 2- or 4-Layer PCB

Emissions Limits: Class A vs. Class B

- Depending on your radiated emissions requirements (Class A or Class B), it is important to select the correct number of layers for your PCB. Typically with the ADM2587E, Class A can be met with a margin on a 2-layer PCB.
- For the more stringent Class B requirements, a stitching capacitance is required in order to meet the required limits. On a 2-layer PCB, this requires the use of a discrete high voltage capacitor. On a 4-layer PCB, use of an embedded interplane capacitor provides better radiated emissions performance.
- Please see Table 1 for more detail on the device setup, load, and measured margin on the required emissions class. Select the number of layers for your design and continue with the layout guide.

<table>
<thead>
<tr>
<th>Layer Count</th>
<th>CISPR 32 Pass Margin (dB)</th>
<th>Supply (V)</th>
<th>Data Rate</th>
<th>Stitching Capacitor Technique</th>
<th>Load (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ADM2587E</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>B 8.5 5.5 3.3</td>
<td>5</td>
<td>500 kbps</td>
<td>Embedded</td>
<td>54</td>
</tr>
<tr>
<td>2</td>
<td>A 3.9</td>
<td>3.3</td>
<td>500 kbps</td>
<td>None</td>
<td>54</td>
</tr>
<tr>
<td><strong>ADM2582E</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>B 8.5 5.5 3.3</td>
<td>5</td>
<td>16 mbps</td>
<td>Embedded</td>
<td>54</td>
</tr>
<tr>
<td>2</td>
<td>A 3.9</td>
<td>3.3</td>
<td>16 mbps</td>
<td>None</td>
<td>54</td>
</tr>
</tbody>
</table>

2. Follow Recommended Decoupling

2-Layer PCB

- Figure 1 shows the components and connections required to meet the desired radiated emissions limits.
- Device decoupling requirements are as follows:
  - 100 nF and 10 nF ceramic caps from \( V_{CC} \) to GND1 (C4/C3) and \( V_{ISOIN} \) to GND2 (C5/C6).
  - 100 nF and 10 μF from \( V_{CC} \) to GND1 (C9/C7) and \( V_{ISOOUT} \) to GND2 (C1/C8).
- Placement of ceramic caps as shown in Figure 2 and Figure 3 for 2- and 4-layer boards, respectively. Ensure the lower value cap is nearest the DUT.
- Capacitor form factors are as follows:
  - C4, C6, C8, and C9 are 0805 footprint.
  - C1, C3, C5, and C7 are 0603 footprint.

4-Layer PCB

- Placement of ceramic caps as shown in Figure 2 and Figure 3 for 2- and 4-layer boards, respectively. Ensure the lower value cap is nearest the DUT.
- Capacitor form factors are as follows:
  - C4, C6, C8, and C9 are 0805 footprint.
  - C1, C3, C5, and C7 are 0603 footprint.
2. Follow Recommended Decoupling (Continued)

<table>
<thead>
<tr>
<th>2-Layer PCB</th>
<th>4-Layer PCB</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="2-layer PCB" /></td>
<td><img src="image2.png" alt="4-layer PCB" /></td>
</tr>
</tbody>
</table>

3. \( V_{\text{ISO}} \) and GND2 Connections

<table>
<thead>
<tr>
<th>2-Layer PCB</th>
<th>4-Layer PCB</th>
</tr>
</thead>
<tbody>
<tr>
<td>- The selection of the ferrite bead for L3 and L2 is critical in order to meet the required emissions limits. This ferrite bead is required to be high impedance over a broad frequency range and it is recommended to use the BLM15HD182SN1 ferrite bead. Figure 4 shows the impedance curve for the ferrite bead.</td>
<td></td>
</tr>
<tr>
<td>- To reduce the capacitive coupling of high frequency noise, ensure there is a minimum 4 mm separation between the isolated ground copper pour at Pin 11 and the GND2 plane, as shown in Figure 2 and Figure 3. Provide cutouts around and below L2 and L3 on all layers.</td>
<td></td>
</tr>
<tr>
<td>- Do not connect the ( V_{\text{ISOOUT}} ) pin to a power plane. Ensure that the ( V_{\text{ISOIN}} ) (Pin 19) is connected through the L3 ferrite bead to the ( V_{\text{ISOOUT}} ) (Pin 12) connect between ( V_{\text{ISOOUT}} ) and ( V_{\text{ISOIN}} ) using a PCB trace, as shown in Figure 2 and Figure 3.</td>
<td></td>
</tr>
<tr>
<td>- Similarly do not connect the GND2 (Pin 11 and Pin 14) directly to the GND2 plane. Connect Pin 14 and Pin 11 using a PCB trace. Ensure that the these pins are connected through the L2 ferrite bead to the GND2 plane.</td>
<td></td>
</tr>
</tbody>
</table>

![Figure 4. BLM15HD182SN1 impedance curve.](image3.png)
4. Provide a Return Path for High Frequency (Common-Mode) Noise

<table>
<thead>
<tr>
<th>2-Layer PCB</th>
<th>4-Layer PCB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Follow the implementation of the stitching capacitor depending on your PCB layer requirements.</td>
<td>Class B can be achieved by placing an embedded stitching capacitor between GND_ISO and GND1 on layers 2 and 3. The capacitance required to meet Class B is 35 pF.</td>
</tr>
<tr>
<td>► For a 2-layer PCB, place a high voltage decoupling capacitor as shown.</td>
<td>► Adjust W, L, and D of overlapping planes to required capacitance. On Layer 3, connect the floating overlapping plane to GND_ISO (Pin 11 and Pin 14) only.</td>
</tr>
<tr>
<td>► Suggested capacitor:</td>
<td>► Note: IEC 61010 third edition requires D to be a minimum of 0.4 mm. Therefore, adjust W and L accordingly.</td>
</tr>
<tr>
<td>■ Value: 100 pF</td>
<td></td>
</tr>
<tr>
<td>■ Case: 1812</td>
<td></td>
</tr>
<tr>
<td>■ Manufacturer: TDK</td>
<td></td>
</tr>
<tr>
<td>■ Manu. No: C4532C0G3F101K160KA</td>
<td></td>
</tr>
</tbody>
</table>

![Figure 5. Placement of high voltage stitching capacitor.](image5)

![Figure 6. PCB stitching capacitance.](image6)

![Figure 7. Embedded stitching capacitor.](image7)

<table>
<thead>
<tr>
<th>Table 2. PCB Stack-up</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>3</td>
</tr>
<tr>
<td>4</td>
</tr>
</tbody>
</table>

Capacitance \( = \frac{\varepsilon_0 \times \varepsilon_r \times W \times L}{D} \)

![Capacitance formula](image8)

For further information on the 2-layer ADM2582E/ADM2587E, please visit [analog.com/UG-916](http://analog.com/UG-916).

For further information on the 4-layer ADM2582E/ADM2587E, please visit [analog.com/UG-044](http://analog.com/UG-044).