SCHEMATIC AND WAVEFORM EDITING SHORTCUTS

Place Components*

W	wire	W
G	ground	G
Alt G	com	⌥ G
V	*voltage*	V
R	resistor	R
C	capacitor	C
L	inductor	L
D	diode	D
P	component	P
N	label net	N
T	text/comment	T
.	spice directive *right-click text field to open "Help me Edit" dialog*	.
B	bus tap	B
⇧ left-click	toggle directive/comment	⇧ left-click

Press Esc or right-click to exit mode.

Schematic Options

hold Ctrl	place angled wires	hold ⌘
hold Ctrl	draw shapes off grid	hold ⌘
Ctrl Alt ⇧ H	show hidden text, e.g. parallel or series resistance	⌘ ⌥ ⇧ H
Ctrl U	show/hide unconn pin marks	⌘ U
Ctrl A	show/hide text anchor marks	⌘ A

most options available in Settings

Probe Schematic*

click	**Probe Wire** plot voltage **Probe Component** plot current	click
Alt click	**Probe Wire** plot current **Probe Component** plot instantaneous power	⌥ click
drag net-to-net	plot differential voltage	drag net-to-net

Probes available once simulation is running.

General Editing

Ctrl X or ⌦ or backspace	delete	⌘ X or ⌦ or backspace
Ctrl C	copy/duplicate*	⌘ C
M	move* *select components to move*	M
S	stretch* *select anchor points to move*	S
Ctrl R	rotate	⌘ R
Ctrl E	mirror	⌘ E
Z	**Schematic** zoom area (drag over area) zoom in (click on scheme) **Waveform** zoom area is default mode	Z
⇧ Z	zoom out	⇧ Z
Space	zoom to fit. zoom extents	Space
Ctrl G	toggle grid	⌘ G
Ctrl Z	undo	⌘ Z
Ctrl ⇧ Z	redo	⌘ ⇧ Z

Choose mode first, then select component or waveform title.
Press Esc or right-click to exit mode.

Edit Text & Component Parameters

right-click >	**text**	**component body**
	edit with helper if available	edit limited parameters
Ctrl	edit directly	edit all parameters

Text preceded by an underscore, e.g. "_FAULT" is displayed with an overbar, "FAULT".

Simulator

A	configure analysis	A
Alt R	run/pause	⌥ R
Alt S	stop	⌥ S
Ctrl L	view SPICE log	⌘ L
0	reset sim waveform T = 0	0

Schematics can be edited even as a simulation runs.
Edits affect subsequent simulations.

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Waveform Viewing

click or C	add cursor and see measure	click
L	label current cursor position	L
⇧ C or Esc	clear all cursors	⇧ C or Esc
Alt click	highlight corresponding net in schematic	⌘ click
Ctrl click	integrate	⌘ click
drag	move trace (to another pane)	drag
drag, hold Ctrl	copy trace (to another pane)	drag, hold ⌘
A	add trace	A
P	add pane above	P
B	add pane below	B
U	move active pane up	U
D	move active pane down	D
⇧ S	select steps	⇧ S
	recenter	

Mouse actions are on label of waveform trace

Waveform Pan & Cursor

↑ ← ↓ →	**No Cursors**	↑ ← ↓ →
← →	**Cursor Present** snap cursor to next time data point	← →
↑ ↓	**Cursor Present** cycle cursors through traces at current time data point	↑ ↓
⇧ + ← →	**Cursor Present** snap cursor to next data point **No Cursors** pan ~50%	⇧ + ← →
Ctrl or ⇧ + ← →	**Cursor Present** bump cursor 10 data points	⌘ or ⇧ + ← →
Ctrl ⇧ + ← →	**Cursor Present** bump cursor 100 data points	⌘ ⇧ + ← →
Ctrl	pan with mouse	⌘
Ctrl ⇧	pan left and right with mouse	⌘ ⇧
Ctrl Alt	pan up and down with mouse	⌘ Alt

Click in waveform pane to apply keyboard functions to active frame.

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ANALOG DEVICES

SPICE QUICK REFERENCE

SPICE Analysis (requires exactly one*)

or A	.ac	perform small signal AC analysis
	.dc	perform DC source sweep analysis
	.fra	perform a specialized transient simulation to analyze the frequency response of a feedback loop.
	.noise	perform noise analysis
	.op	find the DC operating point
	.tf	find the DC small-signal transfer function
	.tran	perform nonlinear transient analysis

** Simulation requires exactly one active spice anlalysis directive.*
Tip: Open Configure Analysis to activate one directive and comment the others.

SPICE Directives

.backanno	annotate subcircuit pin names on port currents; automatically added by netlister
.end	end of netlist; required; added by netlister
.ends	end of subcircuit definition; use with .subckt
.four	compute fourier component
.func	user defined functions
.global	declare global nodes
.ic	set initial conditions
.include	include text from file
.lib	include library
.loadbias*	load a nodeset
.loadstate**	load a previously solved DC solution
.machine	arbitrary state machine
.measure	evaluate user-defined electrical quantities
.model	define a SPICE model
.net	compute network parameters in .AC analysis
.nodeset	supply hints for initial DC solution
.options	set simulator options
.param	user-defined parameters
.save	limit the quantity of saved data
.savebias*	save a nodeset to file
.savestate**	save comprehensive snapshot of state at time in a proprietary file format
.step	parameter sweeps
.subckt	define a subcircuit
.temp	temperature sweeps
.wave	write selected nodes to a .WAV file

** superceded by .savestate/.loadstate, **versions 24.1 and later*

Spice Netlist Lines/Components

Leading Character	*Type of Line*
*	comment
A	special function device
B	arbitrary behavioral source
C	capacitor
D	diode
E	voltage dependent voltage source
F	current dependent current source
G	voltage dependent current source
H	current dependent voltage source
I	independent current source
J	JFET transistor
K	mutual inductance
L	inductor
M	MOSFET transistor
O	lossy transmission line
Q	bipolar transistor
R	resistor
S	voltage controlled switch
T	lossless transmission line
U	uniform RC-line
V	independent voltage source
W	current controlled switch
X	subcircuit invocation
Z	MESFET or IGBT transistor
@	frequency response analyzer
&	frequency response analysis probe
.	simulation directive; for example: .options reltol=1e-4
+	continuation of the previous line
NA	jumper, schematic only, not netlisted

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COMMAND LINE FLAGS

-alt	set solver to Alternate
-ascii	use ASCII .raw files, degrading performance
-b <command>	batch mode of -run -netlist, or -sync, eg. ...-b -run
-big or -max	start LTspice as a maximized window
-ini <path>	use non-default .ini file
-I<path>	path to insert in the symbol and file search paths; no space after I (cap "i"); eg. -IC:\Users\...
-norm	set solver to Normal
-run	open the schematic and simulate
-encrypt	encrypt a model library
-FastAccess	convert a binary .raw file to Fast Access format
-FixUpSchematicFonts -FixUpSymbolFonts	convert the font size field of very old user-authored schematic/symbol text to the modern default
-netlist	batch conversion of a schematic to a netlist
-PCBnetlist	convert schematic to a PCB format netlist
-sync	update component libraries
-uninstall	uninstall LTspice

Syntax: LTspice.exe -I<path> <schematic.asc> -b -run -ini <path>
Path required for files not in same directory as LTspice.exe.
Can be stated as a full file path or defined using I<path>.

NUMBERS

Value Multipliers

LTspice		*Means*	*Value*
T or t	e12	tera	10^{12}
G or g	e9	giga	10^{9}
meg	e6	mega	10^{6}
K or k	e3	kilo	10^{3}
M or m	e–3	milli	10^{-3}
mil		mil	25.4×10^{-6}
U or u or µ	e–6	micro	10^{-6}
N or n	e–9	nano	10^{-9}
P or p	e–12	pico	10^{-12}
F or f	e–15	femto	10^{-15}

case insensitive
6K34 = 6.34K = 6.34k = 6.34e3
units not required, but allowed
kΩ = kohm = K = k

Constants

LTspice	*Means*
e	Euler's number
pi	π
k	Boltzmann constant
q	charge constant
true	1
false	0

Used in waveform math

DRAWING

editor >			
text	T	T	T
line		I	L
rectangle		R	R
ellipse			C
arc			A

draw arrow available for waveform

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SIMULATION COMMANDS

Key

Description	*Key*	*Replace Key with...*	*Examples*
required literal	foo	foo	Replace V(<node>) with V(out) or V(n001)
<required value>	<foo>	a value	Replace <freq> with 1000 for freq = 1kHz Replace <Tstop> with 2 for stop time = 2s
[optional literal]	[foo]	foo, or leave out	Replace [startup] with startup
[<optional value>]	[<foo>]	a value, or leave out	Replace [I(<source>)] with I(R1)
<required choice, mutually exclusive, list, of, values>	<foo, bar>	foo or bar	Replace <oct, dec, lin> with oct or leave unspecified for lin
[<optional, mutually exclusive, list, of, values>]	[<foo, bar>]	foo or bar, or leave out for default value, bar	Replace [<oct, dec, lin>] with dec
'<filename>' "<filename>"	<filename>	filename or path to save/retrieve a file	Replace filename with "my path\my file". If no path is specified, the file is saved in the same directory as the netlist or schematic. Enclose the file name or path in single or double quotes.
[...][more]	[...]	optionally more versions of preceding item(s)	Replace V(<node>)[...] with V(n001) V(n002) V(in) V(out)
[parameter=<value>]	[foo=<bar>]	foo=value	Replace [Tstart=<val>] with Tstart=1ms
I(<source>)			<source> can be discrete component, Vsource name or pin. I(R1), I(V1), Ib(Q1)

parentheses () are always literal

SPICE Analysis (requires exactly one*)

.ac or A	.ac	perform small signal AC analysis	.ac <oct, dec, lin> <Npoints> <startfreq> <endfreq> .ac <list> <freq> [...]
	.dc	perform DC source sweep analysis for up to three V or I sources; overrides named source settings with DC sweep of source	.dc <sourcename> <oct, dec, lin> <startvalue> <stopvalue> <incr> [more sources] .dc <sourcename> list <value> [...] [more sources]
	.fra	perform a transient simulation to analyze the frequency response of a feedback loop land produce a Bode plot	.fra [Tstart=<time>] [dTmax=<time>] [Tstep=<time>] + [Tstop=<time>] [uic] [startup]
	.noise	perform noise analysis	.noise V(<node>[,<refnode>]) <src> + <oct, dec, lin> <Npoints > <startfreq> <endfreq> .noise V(<node>[,<refnode>]) <src> list <freq> [...]
	.op	find the DC operating point	.op
	.tf	find the DC small-signal transfer function	.tf V(<node> [, <refnode>]) <source> .tf I(<Vsource>) <source>
	.tran	perform nonlinear transient analysis	.tran <Tstep> <Tstop> + [Tstart [dTmax]] + [uic]** [steady] [nodiscard] [startup] [step] + [loadstate=[<filename>]] + [savestate=[<filename>]] [savestatetime=[<time>]] .tran <Tstop> + [uic]** [steady] [nodiscard] [startup] [step] + [loadstate=[<filename>]] + [savestate=[<filename>]] [savestatetime=[<time>]]

** Simulation requires exactly one active spice anlalysis directive.*
Tip: Opening Configure Analysis comments out all but one anlalysis command.
*** Use of this modifier is highly discouraged. In particular, it is not a viable workaround for DC operating point convergence problems.*

SPICE Directives

.backanno	annotate subcircuit pin names on port currents; automatically added by netlister	.backanno
.end	end of netlist; required; added by netlister	.end
.ends	end of subcircuit definition	.ends (used with .subckt)
.four	compute fourier component	.four <freq> [Nharmonics] [Nperiods] + <datatrace> [...]
.func	user defined functions	.func <name> ([arguments]) {<expression>}
.global	declare global nodes	.global <node> [...]
.ic	set initial conditions	.ic [V(<node>)=<voltage>] [...] + [I(<inductor>)=<current>] [...]
.include	include text from file	.include <filename.ext>
.lib	include library	.lib <filename> [<entryname>]
.loadbias*	load a nodeset from a file	.loadbias <filename>
.loadstate**	load a previously solved DC solution	.loadstate <statefilename> [reset]
.machine	arbitrary state machine	.mach[ine] [<tripdt>] .state <name> <value> .rule <old state> <new state> <condition> .output (<posnode> [, <negnode>]) <expression> .endmach[ine]
.measure	evaluate user-defined electrical quantities at a point on the abscissa or over a range	.meas[sure] [ac, dc, op, tran, tf, noise] <name> + [<find, deriv, param> <expr> [when <expr>, at=<expr>]] + [td=<val1>] [<rise, fall, cross>=[<count1>, last]]
.model	define a SPICE model	.model <name> <type> [(<parameter list>)]
.net	compute network parameters in .AC analysis	.net [V(out[,ref]), I(Rout)] < Vin, lin> +[Rin=<val>] [Rout=<val>]
.nodeset	supply hints for initial DC solution	.nodeset V(<node>)=<voltage> [...]
.options	set simulator options	.options
.param	user-defined parameters	.param
.save	limit the quantity of saved data	.save V(<node>) [...] [V(n2) [I(L1) [I(S2)]]]
.savebias*	save a nodeset to file	.savebias <filename> [internal] + [temp=<temp>] [time=<time> [repeat]] + [step=<step#>] + [DC1=<value>] [DC2=<value>] [DC3=<value>]
.savestate**	save comprehensive snapshot of state	.savestate <filename> [time=<time>]
.step	parameter sweeps	.step [<oct, dec, lin>] <item> <startval> <endval> <incr> .step <item> list <value> [...]
.subckt	begin a subcircuit definition	.subckt <name> [<node>] [...]
.temp	temperature sweep; same as .step temp list	.temp <temp> [...]
.wave	write selected nodes to a .WAV file	.wave <filename.wav> <Nbits> <SampleRate> + V(<node>) [...] [I(<source>)] [...]

** superceded by .savestate/.loadstate, **versions 24.1 and later*

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.OPTIONS FLAGS/MODIFIERS AND PARAMETERS

Keyword	Type	Default	Description
abstol	=	1pA	Absolute current error tolerance
allow_ambiguous_models	flag		Each model used in simulation can have exactly one definition. This option tells LTspice to ignore the error, choose a model with no indication of which, and continue simulating.
baudrate	=	(none)	In eye diagrams, tells the waveform viewer how to wrap the abscissa time to overlay the bit transitions.
chgtol	=	10fC	Absolute charge tolerance
cshunt	=	0	Optional capacitance added from every node to ground
cshuntintern	=	cshunt	Optional capacitance added from every device internal node to ground
debugtran	flag		Add device and node convergence difficulty scores to the log file. Slows down the simulation. Results are relative, but generally, values below 1 are negligible, while values above ~50 are problematic.
defad	=	0	Default MOS drain diffusion area
defas	=	0	Default MOS source diffusion area
defl	=	100µm	Default MOS channel length
defw	=	100µm	Default MOS channel width
delay	=	0	Used for eye diagrams. Shifts the bit transitions in the diagram.
fastaccess	flag		Convert to fastaccess file format at end of simulation
flagloads	flag		Flags external current sources as loads
gfarad	=	1e-12	Conductivity leakage per farad of every capacitor element
gfloat	=	1e-12	Conductivity added to from every floating node to ground if topology checking is enabled
gmin	=	1e-12	Conductivity added to every PN junction to aid convergence
gminsteps	=	25	Set to zero to prevent gminstepping for the initial DC solution
gshunt	=	0	Optional conductance added from every node to ground
itl1	=	100	DC iteration count limit
itl2	=	50	DC transfer curve iteration count limi
itl4	=	10	Transient analysis time point iteration count limit
itl6	=	25	Set to zero to prevent source stepping for the initial DC solution
srcsteps	=	25	Alternative name for itl6
list	flag		Put expanded netlist into log file. This has priority over the corresponding choice in the Settings window.
logparams	flag		Puts all parameters into the log file. Useful as a diagnostic.
logopinfo	flag		Puts operating point information of semiconductor devices into log file
maxclocks	=	∞	maximum number of clock cycles to save
maxstep	=	∞	Maximum step size for transient analysis
meascplxfmt	=	bode	Complex number format of .meas statement results. One of "polar", "cartesian", or "bode".
measdgt	=	6	Number of significant figures used for .measure statement output
method	=	trap	Numerical integration method, either "trap", "modtrap", or "gear". This has priority over the corresponding choice in the Settings window.
minclocks	=	10	Minimum number of clock cycles to save
mindeltagmin	=	1e-4	Limit for termination of adaptive gmin stepping

Keyword	Type	Default	Description
no_caret_warning	flag		Suppresses all caret operator warnings.
nomarch	flag		Do not plot marching waveforms
noopiter	flag		Go directly to gmin stepping
numdgt	=	6	Historically "numdgt" was used to set the number of significant figures used for output data. In LTspice, if "numdgt" is set to be > 6, double precision is used for dependent variable data.
pivrel	=	.001	Relative ratio between the largest column entry and an acceptable pivot value
pivtol	=	1e-13	Absolute minimum value for a matrix entry to be accepted as a pivot
plotreltol	=	0.0025	Relative error tolerance for waveform compression
plotvntol	=	10µV	Absolute voltage error tolerance for waveform compression
plotabstol	=	1nA	Absolute current error tolerance for waveform compression
plotwinsize	=	300	Number of data points in each compression window. With compression, each compression window is reduced to fitted polynomials. Smaller numbers mean less compression. Set to zero to disable compression.
ptrantau	=	0.1	Characteristic source start-up time for a damped pseudo transient analysis to find the operating point. Set to zero to disable pseudo transient.
ptranmax	=	0	If set non-zero, that time of the damped pseudo transient analysis is used as the operating point whether the circuit has settled or not
reject_number_tails	flag		Report any numeric literal with additional text following the number as syntax error
reltol	=	.001	Relative error tolerance
solver	=	(none)	Solver to use. Values are either "norm" or "alt". This setting overrides solver choice in Settings, and/or "-alt" and "-norm" command line flags.
srcstepmethod	=	0	Which source stepping algorithm to start with
sstol	=	.001	Relative error for steady-state detection
ststclocks	=	10	Number of clock cycles to process in continuous switching mode after steady state detection
ststdelay	=	0	Time to wait before trying to detect steady state
temp	=	27°C	Default temperature for circuit element instances that don't specify temperature
tnom	=	27°C	Default temperature at which device parameters were measured for models that don't specify this temperature
topologycheck	=	1	Set to zero to skip check for floating nodes, loops of voltage sources, and non-physical transformer winding topology
trtol	=	2.0	Transient error tolerance. This parameter is an estimate of the factor by which the actual truncation error is overestimated
trytocompact	=	1	When non-zero, the simulator tries to condense LTRA transmission lines' history of input voltages and currents
vntol	=	1µV	Absolute voltage error tolerance

Flags have no value; either the flag is present or it is not. Syntax is .options [flag][...][<keyword> = <value>][...]

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