**READY FOR PRIME TIME**

**THE EVOLUTION OF THE JESD204B HIGH SPEED CONVERTER INTERFACE STANDARD**

This infographic shows the evolution of the JEDEC® JESD204B standard, the high speed, high resolution converter interface technology of choice for today's high performance applications. Defining high speed serial link standards for data converters and logic devices, JESD204B enables smaller and lower cost device packages, reduces system test efforts and development costs, and accelerates product development. JESD204B has become the default interface for high speed analog I/O components.

**JESD204 original release**

- Designed to address the demand for a repeatable interface between converters and a receiver, such as an FPGA or ASIC.
- Problems:
  - Data rates in excess of 3.125 Gbps were limiting and additional lanes were needed.
  - Faster sampling rates and higher resolution made converter footprints awkward.

**Revision A (JESD204A)**

- Increased allowable converter speed, decreased noise and cross-talk, and utilization of both serial lanes for jitter mitigation.
- Problems:
  - Data rates increased to 12.5 Gbps (Double lane).
  - The device clock can be utilized instead of the frame clock.
  - Three subclasses divide devices into three speed grades.

**Revision B (JESD204B)**

- Increased available converter speed, decreased noise and cross-talk, and utilization of both serial lanes for jitter mitigation.
- Problems:
  - Lane data rates, the frame clock and the electrical interface stayed the same.
  - Converter speeds and resolutions kept increasing and more capability was needed.
  - ADI releases its first ADC with the JESD204 interface standard.

**Revision C (JESD204C)**

- Increased available converter speed, decreased noise and cross-talk, and utilization of both serial lanes for jitter mitigation.
- Problems:
  -Lane data rates, the frame clock and the electrical interface stayed the same.
  -Converter speeds and resolutions kept increasing and more capability was needed.

**ADI takes the evolution of JESD204B to the next level with:**

- Higher level system integration.
- Easier multichannel system synchronization.
- Smaller and lower cost device packages.
- Fewer interconnects.
- Deterministic latency.

**JESD204B makes it possible to convert many high speed, high resolution ADCs and DACs to an FPGA or ASIC with a small number of copper conductors, smaller device footprints, and simpler routing on the circuit board.**

**ADI releases first four ADCs with JESD204B to industry acclaim**

**ADI achieves JESD204B interoperability between the ADI ADS9250 analog-to-digital and ADCS to 12.5 Gbps, enabling greater integration for high speed analog I/O.**

**The JESD204B standard is rapidly adopted in high resolution converter and ADC applications including:**

- Wireless infrastructure transceivers.
- Software-defined radios.
- Medical imaging systems.
- Defence and aerospace.
- Radar and remote sensing.
- Electronic countermeasures and signal monitoring.
- Secure communications.
- Instrumentation and automated test equipment.
- Spectrum analysis and data acquisition.
- Digital video capture.
- Manufacturing.

**The JESD204 interface becomes the default interface for high speed analog I/O components.**

**Evolution of JESD204B to JESD204C to increase speed and efficiency.**

Learn more about ADI's JESD204B serial interface and JEDEC standard data converters.